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4736B/4736BX

1024-BIT RANDOM ACCESS MEMORY WITH 3-STATE OUTPUTS

DESCRIPTION – The 4736B/4736BX is a 1024-Bit, Random Access Memory, organized 1024 words x 1 bit, with 3-state outputs. It has a Data Input (D), ten Address Inputs (A_0-A_9), an active LOW Write Enable Input ($\overline{WE}$), an active LOW Chip Select Input ($\overline{CS}$), and one 3-State Data Output (Q).

Information on the Data Input (D) is written into the memory location selected by the Address Inputs (A_0-A_9) when the Chip Select Input ($\overline{CS}$) and the Write Enable Input ($\overline{WE}$) are LOW. Under these conditions the Data Output (Q) is held in a high impedance OFF state. Information is read from the memory location selected by the Address Inputs (A_0-A_9) while $\overline{CS}$ is LOW and $\overline{WE}$ is HIGH. When $\overline{CS}$ is HIGH the Data Output (Q) is held in a high impedance OFF state. This allows other 3-state outputs to be wired together in a bus arrangement. The 4736B/4736BX offers fully static operation. The 4736B is specified to operate over a Power Supply Voltage Range of 5 ± 0.5 V. The 4736BX is specified to operate over a Power Supply Voltage Range of 4.5 V to 12.5 V.

- **TYPICAL HOLDING VOLTAGE OF 1.5 V**
- **3-STATE OUTPUTS**
- **ORGANIZATION – 1024 WORDS x 1 BIT**
- **ON-CHIP DECODING**
- **FULLY STATIC OPERATION**
- **LOW POWER DISSIPATION**
- **HIGH SPEED**
- **CHIP SELECT INPUT FOR EASY MEMORY EXPANSION**

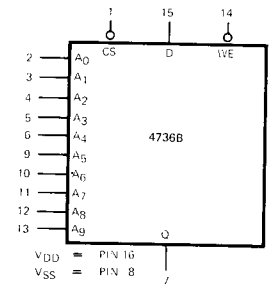
PIN NAMES

$\overline{CS}$	Chip Select (Active LOW) Input
A_0-A_9	Address Inputs
$\overline{WE}$	Write Enable (Active LOW) Input
D	Data Input
Q	Data Output

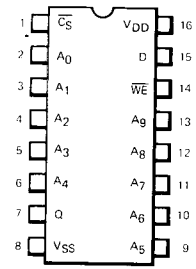
MODE SELECTION

	INPUTS		OUTPUT	MODE
	$\overline{CS}$	$\overline{WE}$	Q	
H = HIGH Level	H	X	High Impedance	Inhibit
L = LOW Level	L	L	High Impedance	Write
X = Don't Care	L	H	Data Written Into Memory	Read

LOGIC SYMBOL

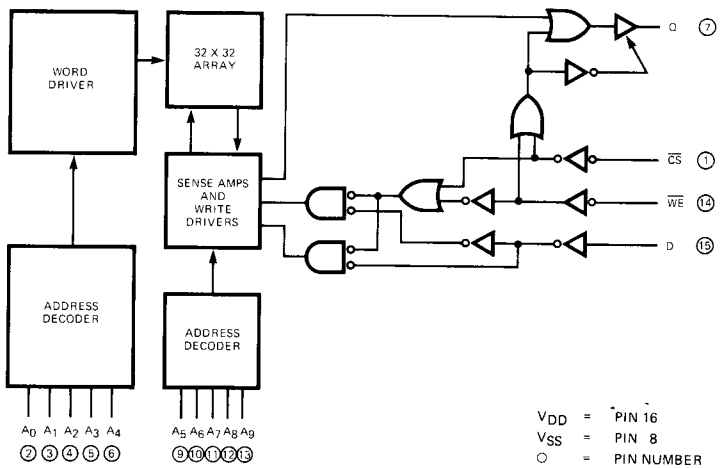


CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

BLOCK DIAGRAM



DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 12.5 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{OZH}	Output OFF Current HIGH	XC									1.6	μA	MIN, 25°C	Output Returned to V_{DD}, $\overline{CS}$ = V_{DD}
											12		MAX	
		XM									0.4		MIN, 25°C	
											12		MAX	
I_{OZL}	Output OFF Current LOW	XC									-1.6	μA	MIN, 25°C	Output Returned to V_{SS}, $\overline{CS}$ = V_{DD}
											- 12		MAX	
		XM									-0.4		MIN, 25°C	
											- 12		MAX	
I_{DD}	Quiescent Power Supply Current	XC			32.5			65			130	μA	MIN, 25°C	$\overline{CS}$ = V_{DD} All inputs at 0 V or V_{DD}
					250			500			1000		MAX	
		XM			8.75			17.5			35		MIN, 25°C	
					250			500			1000		MAX	

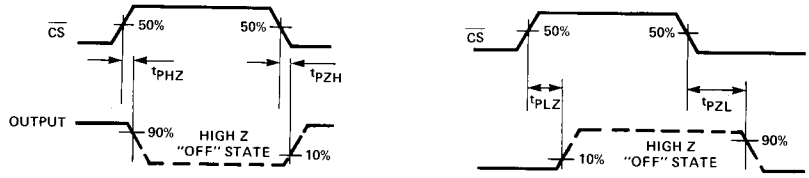
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 12.5 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
	READ MODE											C_L = 50 pF, R_L = 200 kΩ Input Transition Times ⩽ 20 ns
t_{PLH}	Propagation Delay, Address to Output		500			320			260		ns	
t_{PHL}			500			320			260			
t_{PZH}	Enable Time, $\overline{CS}$ to Output		150			70			50		ns	(R_L = 1 kΩ to V_{SS})
t_{PZL}			150			70			50			(R_L = 1 kΩ to V_{DD})
t_{PHZ}	Disable Time, $\overline{CS}$ to Output		150			70			50		ns	(R_L = 1 kΩ to V_{SS})
t_{PLZ}			150			70			50			(R_L = 1 kΩ to V_{DD})
t_{TLH}	Output Transition Time		75			35			25		ns	
t_{THL}			75			35			25			
	WRITE MODE											
t_{PZH}	Enable Time, $\overline{WE}$ to Output		150			70			50		ns	(R_L = 1 kΩ to V_{SS})
t_{PZL}			150			70			50			(R_L = 1 kΩ to V_{DD})
t_{PHZ}	Disable Time, $\overline{WE}$ to Output		150			70			50		ns	(R_L = 1 kΩ to V_{SS})
t_{PLZ}			150			70			50			(R_L = 1 kΩ to V_{DD})
$t_{W\overline{WE}}$	Minimum $\overline{WE}$ Pulse Width		180			100			80		ns	
t_s	Set-Up Time, D_n to $\overline{WE}$		150			120			115		ns	
t_h	Hold Time, D_n to $\overline{WE}$		40			20			15			
t_s	Set-Up Time, Address to $\overline{WE}$		150			120			115		ns	
t_h	Hold Time, Address to $\overline{WE}$		40			20			15			
t_s	Set-Up Time, $\overline{CS}$ to $\overline{WE}$		150			120			115		ns	
t_h	Hold Time, $\overline{CS}$ to $\overline{WE}$		40			20			15			

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

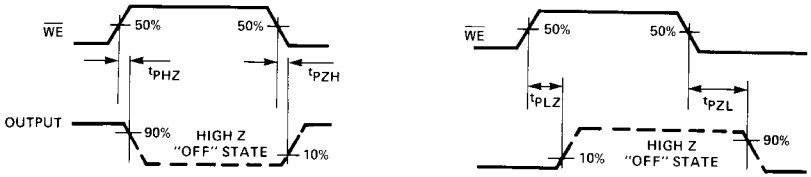
AC WAVEFORMS

READ MODE

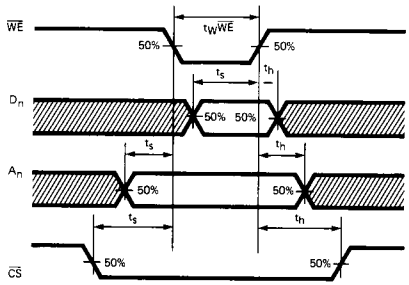


$\overline{CS}$ TO OUTPUT ENABLE AND DISABLE TIMES

WRITE MODE



$\overline{WE}$ TO OUTPUT ENABLE AND DISABLE TIMES



MINIMUM $\overline{WE}$ PULSE WIDTH AND SET-UP AND HOLD TIMES, D_n TO $\overline{WE}$, A_n TO $\overline{WE}$, AND $\overline{CS}$ TO $\overline{WE}$

Note: Set-up and Hold Times are shown as positive values but may be specified as negative values.