NEC microcomputers, inc. OBSOLETE

PRELIMINARY

μPD414-E
μPD414
μPD414-1
μPD414-2

FULLY DECODED RANDOM ACCESS 4096 BIT DYNAMIC MEMORY

DESCRIPTION

The NEC μPD414 is a 4096 words by 1 bit Dynamic N channel MOS RAM. It was designed for memory applications where very low cost and large bit storage are important design objectives. The μPD414 uses a single transistor dynamic storage cell and dynamic circuitry to achieve high speed and low power dissipation.

The μPD414 is packaged in the standard 16 pin dual-in-line package. The 16 pin package provides the highest system bit densities and is available in either cerdip or plastic.

Single Copy
Handle With Care

The use of the 16 pin package is made possible by multiplexing the 12 address bits (required to address 1 of 4096 bits) into the μPD414 on 6 address input pins. The two 6 bit address words are latched into the μPD414 by the two TTL clocks, Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). Noncritical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

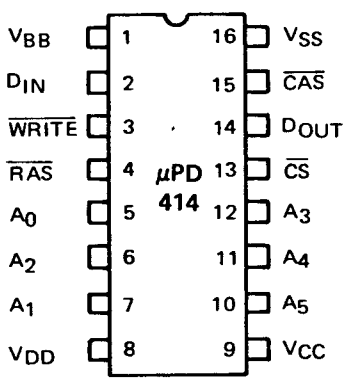
The single transistor dynamic storage cell provides high speed along with low power dissipation. The memory cell requires refreshing for data retention. Refreshing is most easily accomplished by performing a read cycle at each of the 64 row addresses every 2 milliseconds.

FEATURES

- 4096 Words x 1 Bit Organization
- Refresh Period 2 ms
- Standard 16 Pin Cerdip and Plastic Packages
- Low Standby Power
- All Inputs Including Clocks TTL Compatible
- Standard Power Supplies +12V, +5V, −5V
- Gated $\overline{CAS}$ Characteristic
- On-Chip Latches for Addresses, Chip Select and Data In
- Simple Memory Expansion Chip Select
- Output is Three State, TTL Compatible; Data is Latched and Valid into Next Cycle
- 4 Performance Ranges:

	ACCESS TIME	R/W CYCLE	RMW CYCLE
μPD414-E	350 ns	500 ns	700 ns
μPD414	300 ns	425 ns	590 ns
μPD414-1	250 ns	375 ns	480 ns
μPD414-2	200 ns	375 ns	420 ns

PIN CONFIGURATION



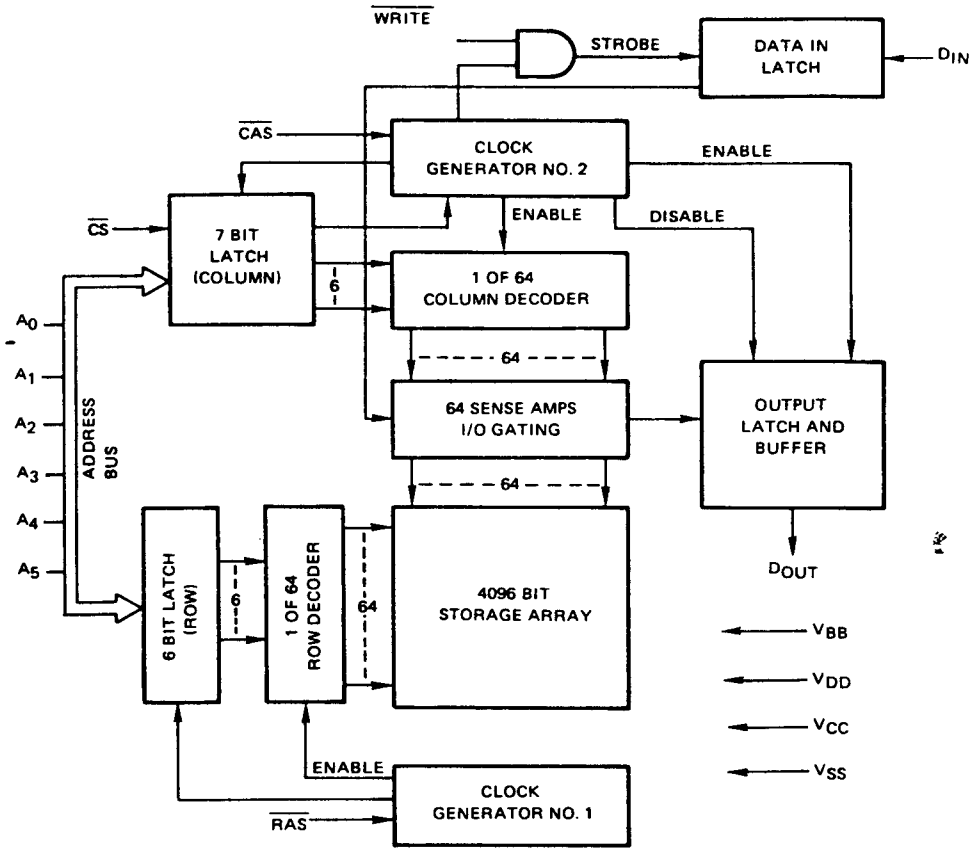
PIN NAMES

A_0-A_5	Address Inputs
$\overline{CAS}$	Column Address Strobe
$\overline{CS}$	Chip Select
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write
V_{BB}	Power (−5V)
V_{CC}	Power (+5V)
V_{DD}	Power (+12V)
V_{SS}	Ground

0816 NEC
RAS
003550
65
3550

Five Militia Drive/Lexington, Massachusetts 02173 Telephone 617/862-6410 Telex 92-3434

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +150°C
All Output Voltages ①	−0.5 to +25 Volts
All Input Voltages ①	−0.5 to +25 Volts
Supply Voltages V_{DD}, V_{CC}, V_{SS} ①	−0.5 to +25 Volts
Power Dissipation	1.0W

Note: ① Relative to V_{BB}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

CAPACITANCE

T_a = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V, unless otherwise noted. ①②

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Address Capacitance	C_{AD}			10	pF	V_{IN} = V_{SS}
$\overline{CAS}$, $\overline{RAS}$, $\overline{CS}$ Capacitance	C_C			7	pF	V_{IN} = V_{SS}
Data Output Capacitance	C_{OUT}			8	pF	V_{OUT} = 0V
D_{IN} and $\overline{WRITE}$ Capacitance	C_{IN}			7	pF	V_{IN} = V_{SS}

Notes: ① All voltages referenced to V_{SS}. The only requirement for the sequence of applying voltages to the device is that V_{DD}, V_{CC}, and V_{SS} should never be 0.5V or more negative than V_{BB}.

② Capacitance measured with Boonton Meter.

DC CHARACTERISTICS

T_a = 0°C to +70°C, V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = −5V ± 10%, ① V_{SS} = 0V, unless otherwise noted.

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP ②	MAX		
Input Load Current (any input)	I_{LI}			10	µA	⑤
Output Leakage Current for High Impedance State	I_{LO}			10	µA	Chip deselected ⑥⑦
V_{DD} Supply Current	I_{DD}OFF ③			2.0	mA	$\overline{CAS}$ and $\overline{RAS}$ at V_{IH}. Chip deselected. ⑥
Average V_{DD} Current	I_{DD}AV ③			35	mA	Cycle time = Min ④ t_{RP} = 150 ns, T_a = 25°C
V_{CC} Supply Current when deselected	I_{CC}OFF			10	µA	⑧
Average V_{BB} Current	I_{BB} ③			75	µA	
Average V_{DD} Power Supply Current During "$\overline{RAS}$ only" cycles	I_{DD3}			28	mA	④
Input Low Voltage (any input)	V_{IL}	−1.0		0.8	V	①⑨
Input High Voltage except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IH}	2.4		7.0	V	①⑨
Output Low Voltage	V_{OL}	0		0.4	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH}	2.4		7.0	V	I_{OH} = −5.0 mA
Supply Voltage	V_{DD}	10.8	12.0	13.2	V	①
Supply Voltage	V_{CC}	V_{SS}	5.0	V_{DD}	V	① ⑩
Supply Voltage	V_{SS}	0	0	0	V	①
Supply Voltage	V_{BB}	−4.5	−5.0	−5.5	V	①
Logic 1 Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.7		7.0	V	⑨

Notes:
① All voltages referenced to V_{SS}. V_{BB} must be applied before and removed after other supply voltages.
② Typical values are for T_a = 25°C and nominal power supply voltages.
③ The I_{DD} current flows to V_{SS}. The I_{BB} current is the sum of all leakage currents.
④ Current is proportional to cycle rate; maximum current is measured at the fastest cycle rate.
⑤ All device pins at 0 volts except V_{BB} which is at −5 volts and the pin under test which is at +10 volts.
⑥ Output is disabled (open-circuit) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1.
⑦ $0V < V_{OUT} < +10V$.
⑧ When chip is selected V_{CC} supply current is dependent on output loading; V_{CC} is connected to output buffer only.
⑨ Device speed is not guaranteed at input voltages greater than TTL levels (0 to +5V).
⑩ Output voltage will swing from V_{SS} to V_{CC} if $V_{CC} \leq V_{DD} - 4$ volts. If $V_{CC} \geq V_{DD} - 4$ volts, the output will swing from V_{SS} to a voltage somewhat less than V_{DD}.

AC CHARACTERISTICS

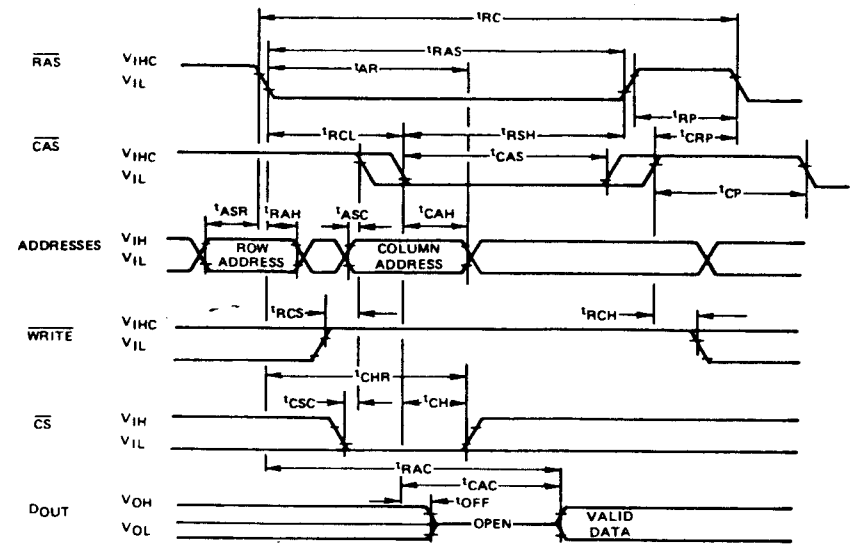
T_a = 0°C to 70°C, V_{DD} = 12V ± 10%, V_{CC} = 5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V, unless otherwise noted.

PARAMETER	SYMBOL	LIMITS												SYMBOL	TEST CONDITIONS
		414-E			414			414-1			414-2				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
Random read or write cycle time	tRC	500			425			375			375			ns	②
Read write cycle time	tRWC	700			590			480			420			ns	
Access time from row address strobe	tRAC			350			300			250			200	ns	③ ⑤
Access time from column address strobe	tCAC			200			165			140			135	ns	④ ⑤
Output buffer turn-off delay	tOFF			100			80			60			50	ns	⑥
Row address strobe precharge time	tRP	150			125			120			120			ns	
Row address strobe pulse width	tRAS	350		32,000	300		32,000	250		32,000	200		32,000	ns	
Row address strobe hold time	tRSH	200			165			140			135			ns	
Column address strobe pulse width	tCAS	200		3,000	165		3,000	140		3,000	135		3,000	ns	
Row to column strobe lead time	tRCL	110		150	90		135	35		110	25		65	ns	⑦
Row address set-up time	tASR	0			0			0			0			ns	
Row address hold time	tRAH	100			80			35			25			ns	
Column address set-up time	tASC	0			0			0			0			ns	
Column address hold time	tCAH	100			80			60			40			ns	
Column address hold time referenced to $\overline{RAS}$	tAR	210			170			160			120			ns	
Chip select set-up time	tCSC	0			0			0			0			ns	
Chip select hold time	tCH	100			80			60			40			ns	
Chip select hold time referenced to $\overline{RAS}$	tCHR	210			170			160			120			ns	
Transition time (rise and fall)	tT	5		50	5		50	3		50	3		50	ns	⑧
Read command set-up time	tRCS	0			0			0			0			ns	
Read command hold time	tRCH	0			0			0			0			ns	
Write command hold time	tWCH	150			130			75			55			ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	260			220			160			120			ns	
Write command pulse width	tWP	200			165			75			55			ns	
Write command to row strobe lead time	tRWL	200			165			140			135			ns	
Write command to column strobe lead time	tCWL	200			165			140			135			ns	
Data in set-up time	tDS	0			0			0			0			ns	⑨
Data in hold time	tDH	150			130			110			110			ns	⑨
Data in hold time referenced to $\overline{RAS}$	tDHR	260			220			195			175			ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	0			0			0			0			ns	
Column precharge time	tCP	150			125			120			120			ns	
Refresh period	tRFSH			2			2			2			2	ms	
$\overline{CAS}$ to $\overline{WRITE}$ delay	tCWD	200			165			90			80			ns	⑩
$\overline{RAS}$ to $\overline{WRITE}$ delay	tRWD	350			300			175			145			ns	⑩

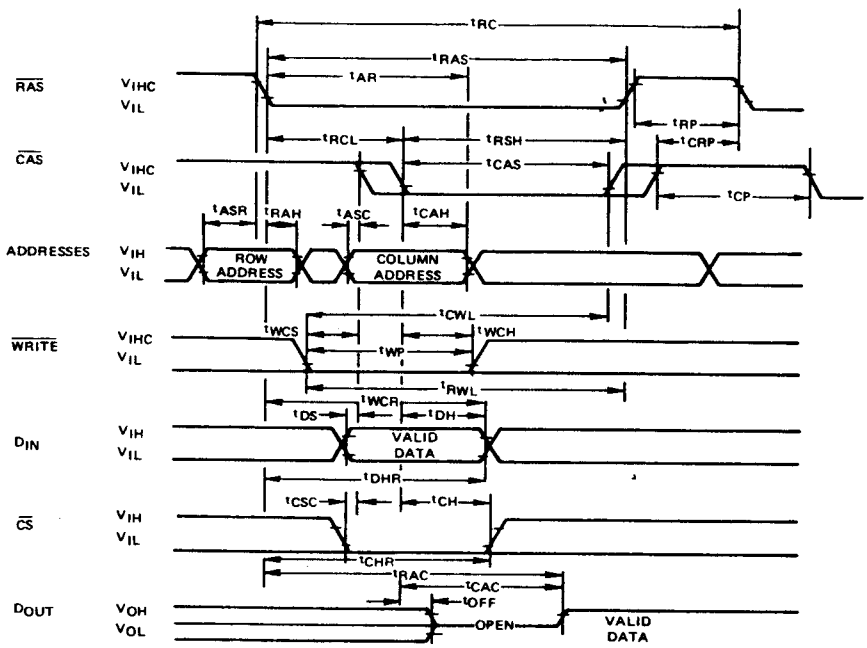
Notes:
① A.C. measurements assume t_T = 5 ns.
② Minimum cylce time (t_{RC}) is greater than $t_{RAS} + t_{RP} + 2t_T$ in order to limit power dissipation.
③ Assumes that $t_{RCL} + t_T \leq t_{RCL}$ (max).
④ Assumes that $t_{RCL} + t_T \geq t_{RCL}$ (max).
⑤ Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
⑥ Assumes that $t_{RCL} + t_T \geq t_{RCL}$ (max). If $t_{RCL} + t_T < t_{RCL}$ (max), 60 + t_{RCL} (max) − t_{RCL} − t_T ns min.
⑦ Operation within the t_{RCL} (max) limit insures that t_{RAC} (max) can be met. t_{RCL} (max) is specified as a reference point only; if t_{RCL} is greater than the specified t_{RCL} (max) limit, then access time is controlled exclusively by t_{CAC}.
⑧ V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
⑨ These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
⑩ t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only:
If $t_{CWD} + t_T \leq t_{CWD}$ (min), the data out latch will contain high level data.
If $t_{CWD} \geq t_{CWD}$ (max) + t_T and $t_{RWD} \geq t_{RWD}$ (max) + t_T, the data out latch will contain the data read from the selected cell.
If t_{CWD} does not meet the above constraints, then data out latch will contain indeterminate data.

TIMING WAVEFORMS

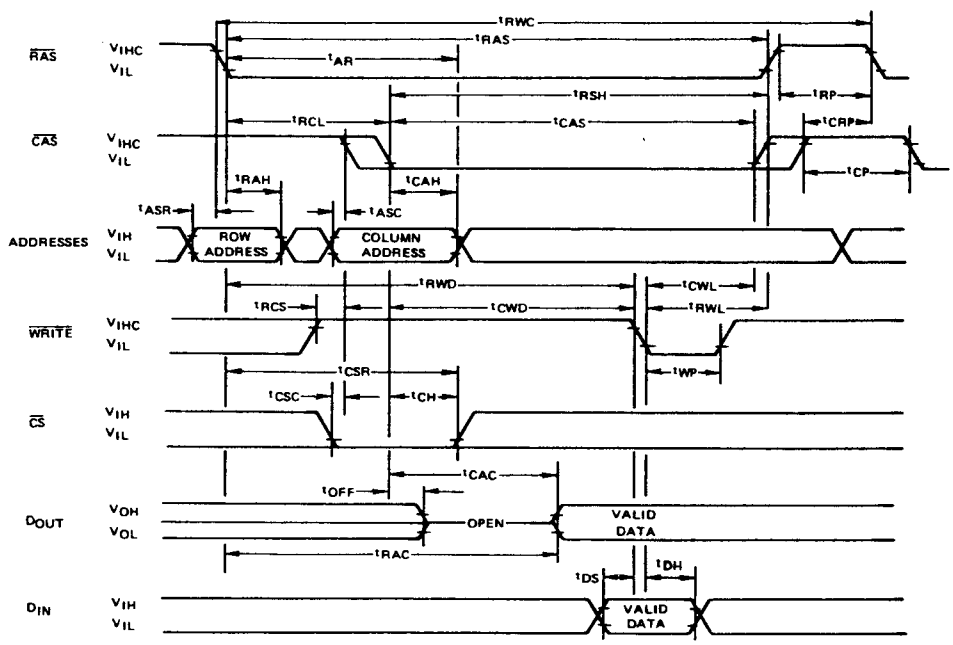
READ CYCLE



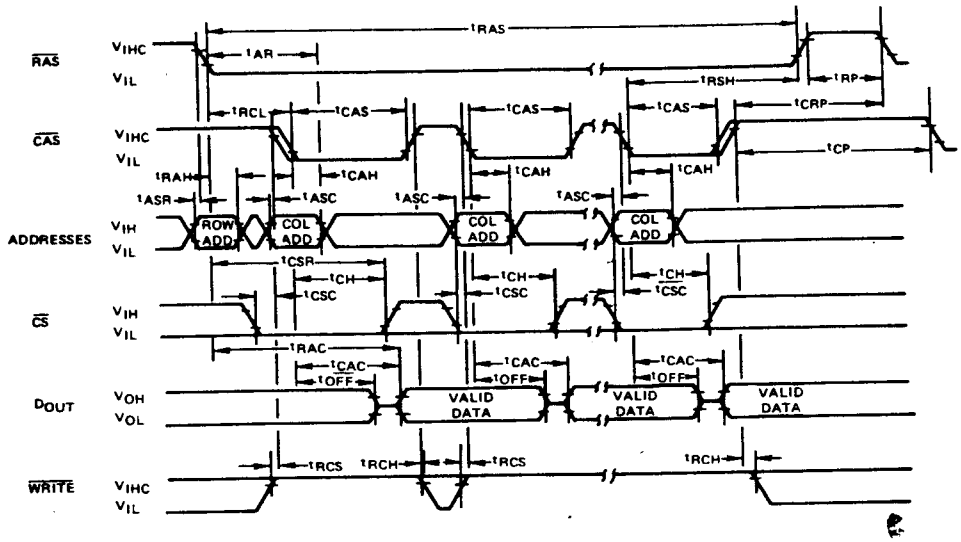
WRITE CYCLE



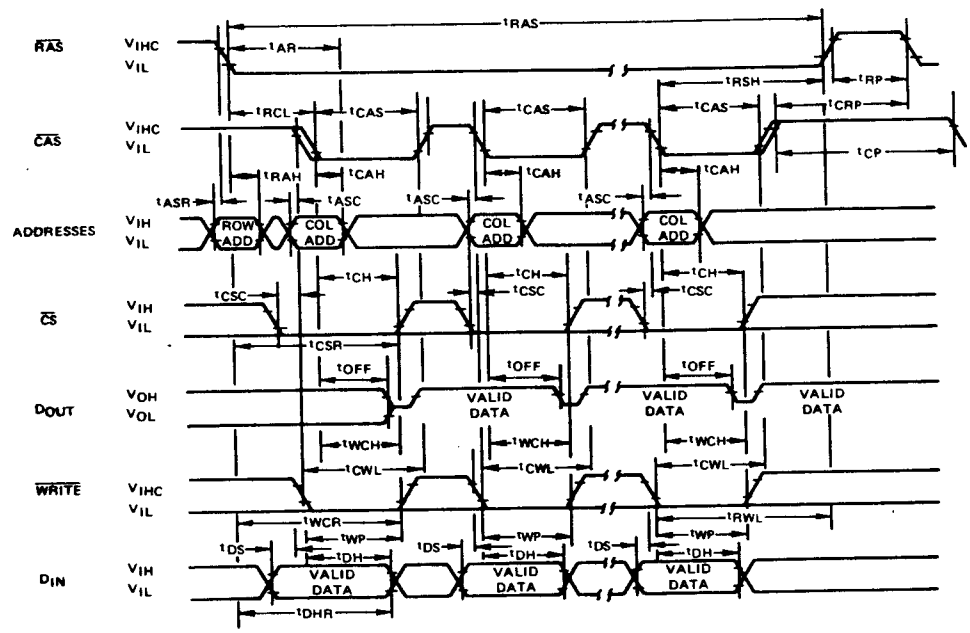
READ-MODIFY-WRITE CYCLE



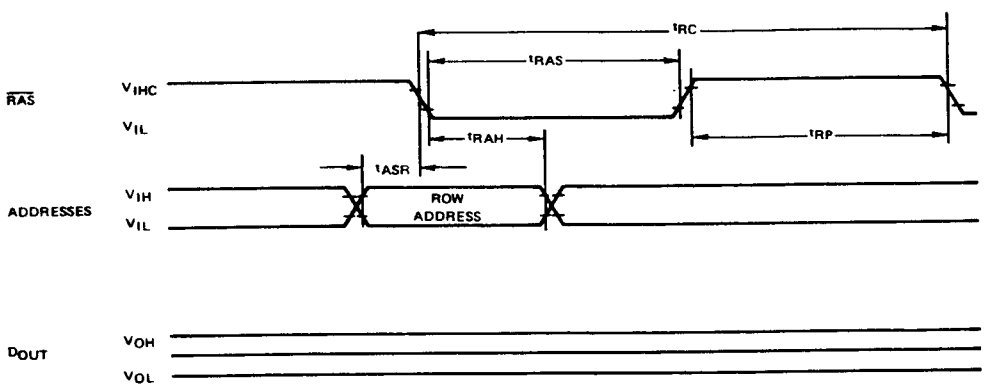
PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



"RAS ONLY" REFRESH CYCLE



Note: DOUT remains unchanged from previous cycle.

ADDRESSING

The 12 address bits required to decode 1 of 4096 bit locations are multiplexed onto the 6 address pins and then latched on the chip with the use of the Row Address Strobe ($\overline{RAS}$), and the Column Address Strobe ($\overline{CAS}$). The 6 bit row address is first applied and $\overline{RAS}$ is then brought low. After the $\overline{RAS}$ hold time has elapsed, the column address and chip select signals are applied and $\overline{CAS}$ is brought low. Since the column address and chip select are not needed internally until a time of t_{RCL} MAX after the row address, this multiplexing operation imposes no penalty on access time as long as $\overline{CAS}$ is applied no later than t_{RCL} MAX. If this time is exceeded, access time will be defined from $\overline{CAS}$ instead of $\overline{RAS}$.

DATA I/O

For a write operation, the input data is latched on the chip by the negative going edge of $\overline{WRITE}$ or $\overline{CAS}$, whichever occurs later. If $\overline{WRITE}$ is active before $\overline{CAS}$, Data out will unconditionally assume a logic "1" state. If $\overline{WRITE}$ is mode active after the access time, as in a read/write cycle, the output will reflect the data read. The output data is latched and will remain in its proper state until the next negative transition of $\overline{CAS}$.

PAGE MODE

The μPD414 may also be operated in page mode for either reading or writing by keeping $\overline{RAS}$ low after strobing in the row address, and cycling $\overline{CAS}$ for each new column address.

REFRESH

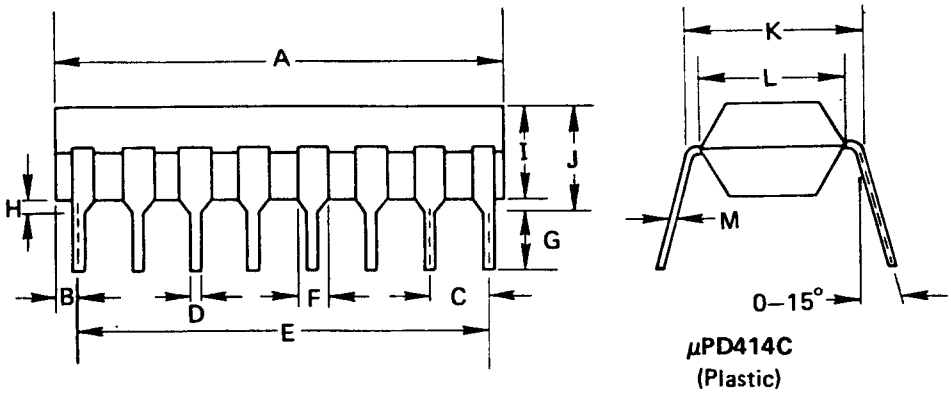
Refresh of the memory matrix is accomplished by performing a memory cycle at each of the 64 row addresses every 2 milliseconds or less. Any memory cycle will refresh the chip regardless of the state of chip select although the chip must be deselected if a write cycle is used to avoid altering data. The data output will go to the high impedance state if chip select is high when $\overline{CAS}$ is brought low.

Refresh may also be achieved by cycling $\overline{RAS}$ only and strobing in each of the 64 row addresses. The data output will remain unaffected by this "$\overline{RAS}$-only" refresh.

$\overline{CAS}$ ONLY OPERATION

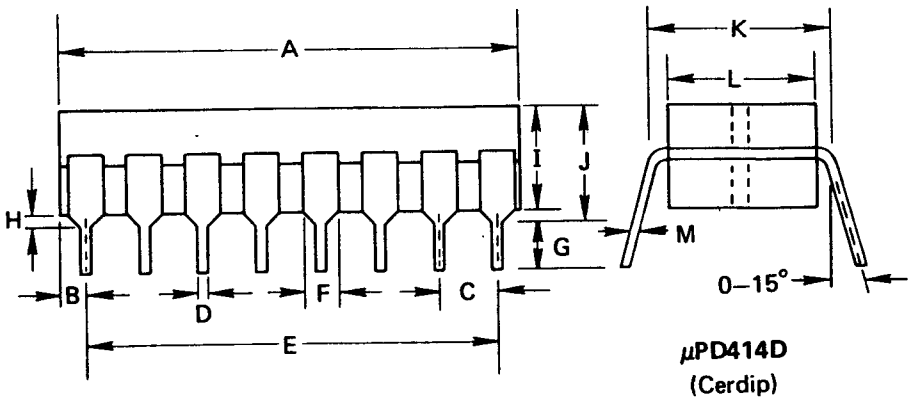
If $\overline{RAS}$ is decoded and applied only to the desired chips, the remaining chips will dissipate no power on the $\overline{CAS}$ edges. In addition, the outputs will assume the high impedance state regardless of chip select.

PACKAGE OUTLINE
μPD414C/D



μPD414C
(Plastic)

ITEM	MILLIMETERS	INCHES
A	19.4 MAX.	0.76 MAX.
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.05 MAX.	0.16 MAX.
J	4.55 MAX.	0.18 MAX.
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	0.01



μPD414D
(Cerdip)

ITEM	MILLIMETERS	INCHES
A	19.9 MAX	0.784 MAX
B	1.06	0.042
C	2.54	0.10
D	0.46 ± 0.10	0.018 ± 0.004
E	17.78	0.70
F	1.5	0.059
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	4.58 MAX	0.181 MAX
J	5.08 MAX	0.20 MAX
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	$0.0098^{+0.0039}_{-0.0019}$