Description

The GM71C(S)18163B/BL is the new generation dynamic RAM organized 1,048,576 words x 16 bit. GM71C(S)18163B/BL has realized higher density, higher performance and various functions by utilizing advanced CMOS process technology. The GM71C(S)18163B/BL offers Extended Data Out (EDO) Mode as a high speed access mode. Multiplexed address inputs permit the GM71C(S)18163B/BL to be packaged in standard 400 mil 42pin plastic SOJ, and standard 400mil 44(50)pin plastic TSOP II. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply 5V ± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

Features

- 1,048,576 Words x 16 Bit Organization
- Extended Data Out Mode Capability
- Single Power Supply (5V ± 10%)
- Fast Access Time & Cycle Time

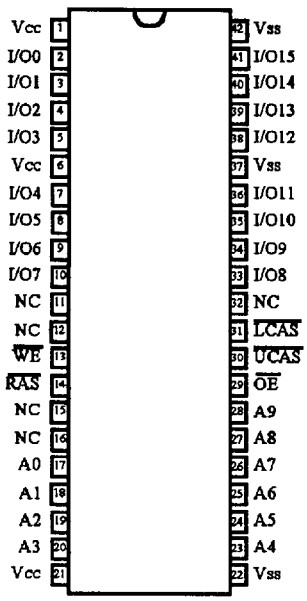
(Unit: ns)

	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
GM71C(S)18163B/BL-6	60	15	104	25
GM71C(S)18163B/BL-7	70	18	124	30
GM71C(S)18163B/BL-8	80	20	144	35

- Low Power
  Active : 935 / 825 / 715mW (MAX)
  Standby : 5.5mW (CMOS level : MAX)
  0.83mW (L-version : MAX)
- $\overline{RAS}$ Only Refresh, $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh Capability
- Self Refresh Operation (L-version)
- All inputs and outputs TTL Compatible
- 1024 Refresh Cycles/16ms
- 1024 Refresh Cycles/128ms (L-version)
- Battery Back Up Operation (L-version)
- 2 $\overline{CAS}$ byte Control

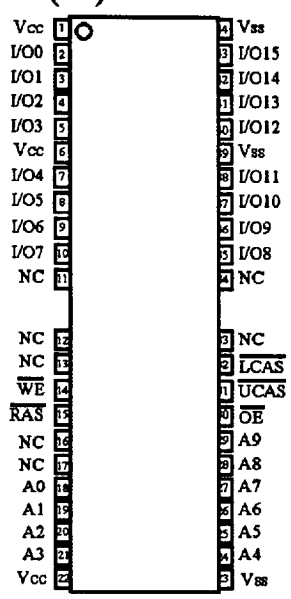
Pin Configuration

42 SOJ



(Top View)

44 (50) TSOP II



Pin Description

Pin	Function	Pin	Function
A0-A9	Address Inputs	$\overline{WE}$	Read/Write Enable
A0-A9	Refresh Address Inputs	$\overline{OE}$	Output Enable
I/O0-I/O15	Data Input / Data Output	Vcc	Power (+5V)
$\overline{RAS}$	Row Address Strobe	Vss	Ground
$\overline{UCAS}$, $\overline{LCAS}$	Column Address Strobe	NC	No Connection

Ordering Information

Type No.	Access Time	Package
GM71C18163AJ-6 GM71C18163AJ-7 GM71C18163AJ-8	60ns 70ns 80ns	400 Mil 42 Pin Plastic SOJ
GM71C18163AT-6 GM71C18163AT-7 GM71C18163AT-8	60ns 70ns 80ns	400 Mil 44 (50) Pin Plastic TSOP II
GM71CS18163ALJ-6 GM71CS18163ALJ-7 GM71CS18163ALJ-8	60ns 70ns 80ns	400 Mil 42 Pin Plastic SOJ
GM71CS18163ALT-6 GM71CS18163ALT-7 GM71CS18163ALT-8	60ns 70ns 80ns	400 Mil 44 (50) Pin Plastic TSOP II

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0 ~ 70	℃
T_{STG}	Storage Temperature (Plastic)	-55 ~ 125	℃
V_{IN}/V_{OUT}	Voltage on any Pin Relative to Vss	-1.0 ~ +7.0	V
Vcc	Voltage on Vcc Relative to Vss	-1.0 ~ +7.0	V
I_{OUT}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	1.0	W

*Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

Recommended DC Operating Conditions ($T_A = 0 \sim 70℃$)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	-	6.5	V
V_{IL}	Input Low Voltage	-1.0	-	0.8	V

*Note: All voltage referred to Vss.
The supply voltage with all Vcc pins must be on the same level. The supply voltage with all Vss pins must be on the same level.

Truth Table

$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	Output	Operation		Notes
H	D	D	D	D	Open	Standby		1,3
L	L	H	H	L	Valid	Lower byte	Read cycle	1,3
L	H	L	H	L	Valid	Upper byte		
L	L	L	H	L	Valid	Word		
L	L	H	L	D	Open	Lower byte	Early write cycle	1,2,3
L	H	L	L	D	Open	Upper byte		
L	L	L	L	D	Open	Word		
L	L	H	L	H	Undefined	Lower byte	Delayed Write cycle	1,2,3
L	H	L	L	H	Undefined	Upper byte		
L	L	L	L	H	Undefined	Word		
L	L	H	H to L	L to H	Valid	Lower byte	Read-modify -write cycle	1,3
L	H	L	H to L	L to H	Valid	Upper byte		
L	L	L	H to L	L to H	Valid	Word		
H to L	H	L	D	D	Open	Word	CBR Refresh or Self Refresh (L-version)	1,3
H to L	L	H	D	D	Open	Word		
H to L	L	L	D	D	Open	Word		
L	H	H	D	D	Open	Word	$\overline{RAS}$-only Refresh cycle	1,3
L	L	L	H	H	Open	Read cycle (Output disabled)		1,3

*Note : 1. H : High(inactive), L : Low(active), D : H or L
2. $t_{WCS} \geq 0ns$: Early write cycle, $t_{WCS} \leq 0ns$: Delayed write cycle
3. Mode is determined by the OR function of the $\overline{UCAS}$ and $\overline{LCAS}$. (Mode is set by the earliest of $\overline{UCAS}$ and $\overline{LCAS}$ active edge and reset by the latest of $\overline{UCAS}$ and $\overline{LCAS}$ inactive edge.)
However write OPERATION and output High-Z control are done independently by each $\overline{UCAS}$, $\overline{LCAS}$.
ex) if $\overline{RAS}$=H to L, $\overline{LCAS}$=L, $\overline{UCAS}$=H, then $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle is selected.

DC Electrical Characteristics (V_{CC} = 3.3V ± 0.3V, T_A = 0 ~ 70℃)

Symbol	Parameter		Min	Max	Unit	Note
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = -2mA)		2.4	Vcc	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 2mA)		0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ Cycling: t_{RC} = t_{RC} min)	60ns	-	170	mA	1, 2
		70ns	-	150		
		80ns	-	130		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ = V_{IH}, D_{OUT} = High-Z)		-	2	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Refresh Mode (t_{RC} = t_{RC} min)	60ns	-	170	mA	2
		70ns	-	150		
		80ns	-	130		
I_{CC4}	Extended Data Out Mode Current Average Power Supply Current EDO Page Mode (t_{HPC} = t_{HPC} min)	60ns	-	185	mA	1, 3
		70ns	-	165		
		80ns	-	150		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ ≥ Vcc - 0.2V, D_{OUT} = High-Z)		-	1	mA	
			-	150	μA	
I_{CC6}	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Current (t_{RC} = t_{RC} min)	60ns	-	170	mA	
		70ns	-	150		
		80ns	-	130		
I_{CC7}	Battery Back Up Operating Current (Standby with CBR Refresh) (t_{RC}=125μs, t_{RAS}≤0.3μs, D_{OUT}=High-Z)		-	0.5	mA	4,5
I_{CC8}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{UCAS}$, $\overline{LCAS}$ = V_{IL} D_{OUT} = Enable		-	5	mA	1
I_{CC9}	Self-Refresh Mode Current ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$≤0.2V, D_{OUT}=High-Z)		-	300	μA	5
$I_{I(L)}$	Input Leakage Current Any Input (0V≤V_{IN}≤7V)		-10	10	μA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, 0V≤V_{OUT}≤7V)		-10	10	μA	

Note: 1. Icc depends on output load condition when the device is selected. Icc(max) is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.

3. Address can be changed once or less while $\overline{LCAS}$ and $\overline{UCAS}$ = V_{IH}.

4. V_{IH} ≥ Vcc - 0.2V, 0V≤V_{IL}≤0.2V .

5. L-version.

Capacitance ($V_{CC} = 5V \pm 10\%$, $T_A = 25℃$)

Symbol	Parameter	Min	Max	Unit	Note
C_{I1}	Input Capacitance (Address)	-	5	pF	1
C_{I2}	Input Capacitance (Clocks)	-	7	pF	1
$C_{I/O}$	Output Capacitance (Data-In/Out)	-	7	pF	1, 2

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{LCAS}$ and $\overline{UCAS}$ = V_{IH} to disable D_{OUT}.

AC Characteristics ($V_{CC} = 5V \pm 10\%$, $T_A = 0 \sim 70℃$, Notes 1, 2, 18, 19, 20)

Test Conditions

Input rise and fall times : 2 ns
Input levels : V_{IL} = 0V, V_{IH} = 3V
Input timing reference levels : 0.8V, 2.4V
Output timing reference levels : 0.8V, 2.0V
Output load : 1TTL gate + CL (100 pF)
(Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	GM71C(S)18163 B/BL-6		GM71C(S)18163 B/BL-7		GM71C(S)18163 B/BL-8		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	104	-	124	-	144	-	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	-	50	-	60	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	13	-	15	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	10	10,000	13	10,000	15	10,000	ns	
t_{ASR}	Row Address Set up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	10	-	ns	
t_{ASC}	Column Address Set-up Time	0	-	0	-	0	-	ns	21
t_{CAH}	Column Address Hold Time	10	-	13	-	15	-	ns	21
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	52	20	60	ns	3
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	4
t_{RSH}	$\overline{RAS}$ Hold Time	15	-	18	-	20	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	48	-	58	-	68	-	ns	23
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	22
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	15	-	18	-	20	-	ns	5
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	0	-	0	-	0	-	ns	6
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	-	0	-	0	-	ns	6
t_T	Transition Time (Rise and Fall)	2	50	2	50	2	50	ns	7
t_{REF}	Refresh Period	-	16	-	16	-	16	ms	
	Refresh Period (L-version)	-	128	-	128	-	128	ms	

Read Cycle

Symbol	Parameter	GM71C(S)18163 B/BL-6		GM71C(S)18163 B/BL-7		GM71C(S)18163 B/BL-8		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	-	60	-	70	-	80	ns	8,9
t_{CAC}	Access Time from $\overline{CAS}$	-	15	-	18	-	20	ns	9,10,17
t_{AA}	Access Time from Address	-	30	-	35	-	40	ns	9,11,17
t_{OAC}	Access Time from $\overline{OE}$	-	15	-	18	-	20	ns	9
t_{RCS}	Read Command Setup Time	0	-	0	-	0	-	ns	21
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	-	0	-	0	-	ns	12,22
t_{RCHR}	Read Command Hold Time to from $\overline{RAS}$	60	-	70	-	80	-	ns	
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	-	5	-	5	-	ns	12
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	-	35	-	40	-	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	18	-	23	-	28	-	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	0	-	ns	
t_{OH}	Output Data Hold Time	3	-	3	-	3	-	ns	27
t_{OHO}	Output Data Hold Time from $\overline{OE}$	3	-	3	-	3	-	ns	
t_{OFF}	Output Buffer Turn-off Time	-	15	-	15	-	15	ns	13,27
t_{OEZ}	Output Buffer Turn-off Time to $\overline{OE}$	-	15	-	15	-	15	ns	13
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	-	18	-	20	-	ns	5
t_{OHR}	Output Data Hold Time from $\overline{RAS}$	3	-	3	-	3	-	ns	27
t_{OFR}	Output Buffer Turn-off Time to $\overline{RAS}$	-	15	-	15	-	15	ns	27
t_{WEZ}	Output Buffer Turn- off to $\overline{WE}$	-	15	-	15	-	15	ns	
t_{WDD}	$\overline{WE}$ to Din Delay Time	15	-	18	-	20	-	ns	
t_{RDD}	$\overline{RAS}$ to Din Delay Time	15	-	18	-	20	-	ns	

Write Cycle

Symbol	Parameter	GM71C(S)18163 B/BL-6		GM71C(S)18163 B/BL-7		GM71C(S)18163 B/BL-8		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{WCS}	Write Command Setup Time	0	-	0	-	0	-	ns	14,21
t_{WCH}	Write Command Hold Time	10	-	13	-	15	-	ns	21
t_{WP}	Write Command Pulse Width	10	-	10	-	10	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	10	-	13	-	15	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	10	-	13	-	15	-	ns	23
t_{DS}	Data-in Setup Time	0	-	0	-	0	-	ns	15,23
t_{DH}	Data-in Hold Time	10	-	13	-	15	-	ns	15,23

Read- Modify-Write Cycle

Symbol	Parameter	GM71C(S)18163 B/BL-6		GM71C(S)18163 B/BL-7		GM71C(S)18163 B/BL-8		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	136	-	161	-	185	-	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	79	-	92	-	104	-	ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	34	-	40	-	44	-	ns	14
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	49	-	57	-	64	-	ns	14
t_{OEH}	$\overline{OE}$ Hold Time from $\overline{WE}$	15	-	18	-	20	-	ns	

Refresh Cycle

Symbol	Parameter	GM71C(S)18163 B/BL-6		GM71C(S)18163 B/BL-7		GM71C(S)18163 B/BL-8		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	5	-	5	-	5	-	ns	21
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	-	10	-	10	-	ns	22
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	0	-	0	-	0	-	ns	21

EDO Mode Cycle

Symbol	Parameter	GM71C(S)18163 B/BL-6		GM71C(S)18163 B/BL-7		GM71C(S)18163 B/BL-8		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{HPC}	EDO Mode Cycle Time	25	-	30	-	35	-	ns	25
t_{RASP}	EDO Mode $\overline{RAS}$ Pulse Width	-	100,000	-	100,000	-	100,000	ns	16
t_{ACP}	Access Time from $\overline{CAS}$ Precharge	-	35	-	40	-	45	ns	9,17,22
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	-	40	-	45	-	ns	
t_{DOH}	Output Data Hold Time from $\overline{CAS}$ Low	3	-	3	-	3	-	ns	9
t_{COL}	$\overline{CAS}$ Hold Time Referred $\overline{OE}$	10	-	13	-	15	-	ns	
t_{COP}	$\overline{CAS}$ to $\overline{OE}$ Setup time	5	-	5	-	5	-	ns	
t_{RCHP}	Read command hold time from $\overline{CAS}$ precharge	35	-	40	-	45	-	ns	

EDO Read-Modify-Write Cycle

Symbol	Parameter	GM71C(S)18163 B/BL-6		GM71C(S)18163 B/BL-7		GM71C(S)18163 B/BL-8		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{HPRWC}	EDO Mode Read-Modify-Write Cycle Time	68	-	79	-	88	-	ns	
t_{CPW}	$\overline{WE}$ Delay Time from $\overline{CAS}$ Precharge	54	-	62	-	69	-	ns	14,22

Self Refresh Mode

Symbol	Parameter	GM71CS18163 AL-6		GM71CS18163 AL-7		GM71CS18163 AL-8		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RASS}	$\overline{RAS}$ Pulse Width (Self-Refresh)	100	-	100	-	100	-	us	29
t_{RPS}	$\overline{RAS}$ Precharge Time (Self-Refresh)	110	-	130	-	150	-	ns	
t_{CHS}	$\overline{CAS}$ Hold Time (Self-Refresh)	-50	-	-50	-	-50	-	ns	

Notes :

1. AC measurements assume t_T = 2 ns.
2. An initial pause of 200 μs is required after power followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh).
3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
5. Either t_{ODD} or t_{CDD} must be satisfied.
6. Either t_{DZO} or t_{DZC} must be satisfied.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
9. Measured with a load circuit equivalent to 1TTL loads and 100pF.
10. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
11. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
13. t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit(high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), and $t_{AWD} \geq t_{AWD}$(min), or $t_{CWD} \geq t_{CWD}$(min) $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. These parameters are referred to $\overline{UCAS}$ and $\overline{LCAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{RASP} defines $\overline{RAS}$ pulse width in EDO mode cycles.
17. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
18. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device. After $\overline{RAS}$ is reset, if $t_{OEH} \geq t_{CWL}$, the I/O pin will remain open circuit (high impedance): if $t_{OEH} \leq t_{CWL}$, invalid data will be out at each I/O.
19. When both $\overline{LCAS}$ and $\overline{UCAS}$ go low at the same time, all 16-bits data are written into the device. $\overline{LCAS}$ and $\overline{UCAS}$ cannot be staggered within the same write/read cycles.
20. All the Vcc and Vss pins shall be supplied with the same voltages.
21. t_{ASC}, t_{CAH}, t_{RCS}, t_{WCS}, t_{WCH}, t_{CSR} and t_{RPC} are determined by the earlier falling edge of $\overline{UCAS}$ or $\overline{LCAS}$.
22. t_{CRP}, t_{CHR}, t_{RCH}, t_{ACP} and t_{CPW} are determined by the later rising edge of $\overline{UCAS}$ or $\overline{LCAS}$.
23. t_{CWL}, t_{DH}, t_{DS} and t_{CHS} should be satisfied by both $\overline{UCAS}$ and $\overline{LCAS}$.
24. t_{CP} is determined by the time that both $\overline{UCAS}$ and $\overline{LCAS}$ are high.

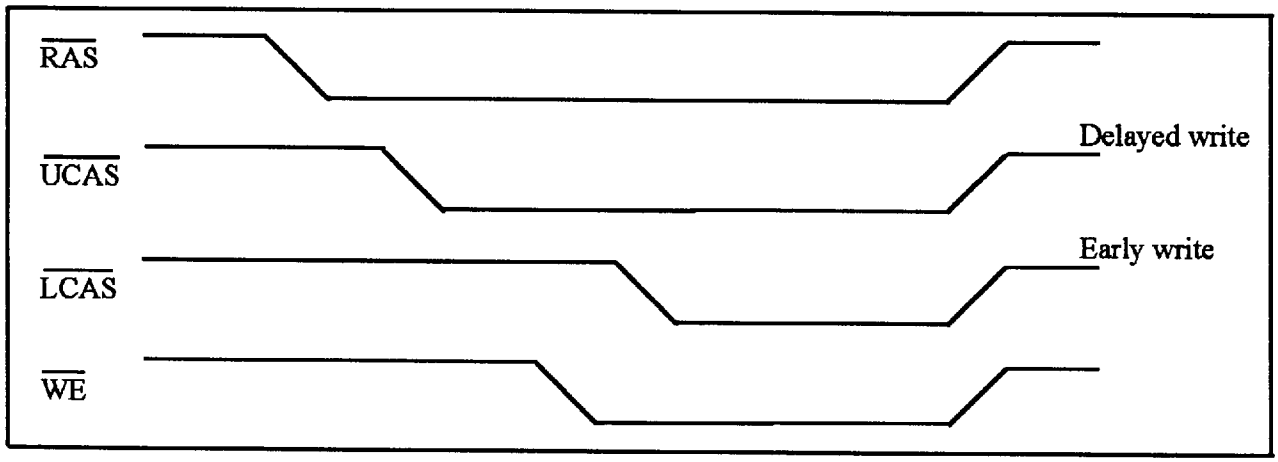
25. t_{HPC}(min) can be achieved during a series of EDO page made write cycles or EDO mode write cycles. It both write and read operation are mixed in a EDO mode $\overline{RAS}$ cycle(EDO mode mix cycle (1),(2)) minimum Value of $\overline{CAS}$ cycle ($t_{CAS}+t_{CP}+2tT$) becomes greater than the specified t_{HPC} (min) value. The value of $\overline{CAS}$ cycle time of mixed EDO mode is shown in EDO mode mix cycle (1) and (2).
26. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time , generally it causes large Vcc/Vss line noise, which causes to degrade V_{IH} min/V_{IL} max level.
27. Data output turns off and becomes high impedance from later rising edge of $\overline{RAS}$ and $\overline{CAS}$. Hold time and turn off time are specified by the timing specification of later rising edge of $\overline{RAS}$ and $\overline{CAS}$ between t_{OHR} and t_{OH}, and between t_{OFR} and t_{OFF}.
28. EDO Hi-Z control by $\overline{OE}$ or $\overline{WE}$. $\overline{OE}$ rising edge disables data outputs. When $\overline{OE}$ goes high during $\overline{CAS}$ high, the data will not come out until next $\overline{CAS}$ access. When $\overline{WE}$ goes low during $\overline{CAS}$ high, the data will not come out until next $\overline{CAS}$ access.
29. Please do not use t_{RASS} timing, $10\mu s \leq t_{RASS} \leq 100\mu s$. During this period, the device is in transition state from normal operation mode to self refresh mode. If $t_{RASS} \geq 100\mu s$, then RAS precharge time should use t_{RPS} instead of t_{RP}.
30. ⊠ H or L (H : V_{IH}(min) ≤ V_{IN} ≤ V_{IH}(max), L : V_{IL}(min) ≤ V_{IN} ≤ V_{IL}(max))

Notes concerning 2$\overline{CAS}$ control

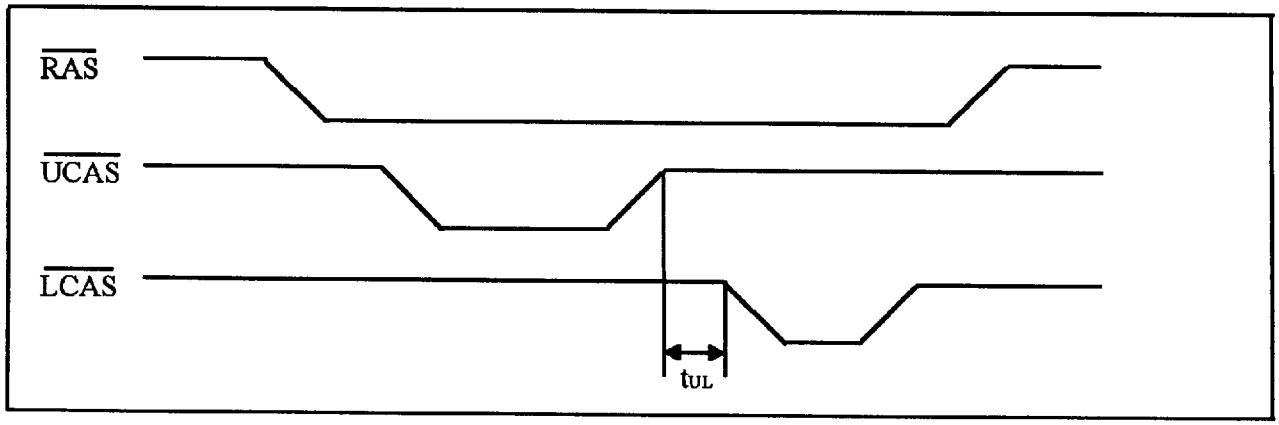
Please do not separate the $\overline{UCAS}$/$\overline{LCAS}$ operation timing intentionally. However skew between $\overline{UCAS}$/$\overline{LCAS}$ are allowed under the following conditions.

(1) Each of the $\overline{UCAS}$/$\overline{LCAS}$ should satisfy the timing specifications individually.

(2) Different operation mode for upper/lower byte is not allowed; such as following.



(3) Closely separated upper/lower byte control is not allowed. However when the condition($t_{CP} \leq t_{UL}$) is satisfied, EDO page mode can be performed.



(4) Byte control operation by remaining $\overline{LCAS}$ or $\overline{UCAS}$ high is guaranteed.

Timing Waveforms *30

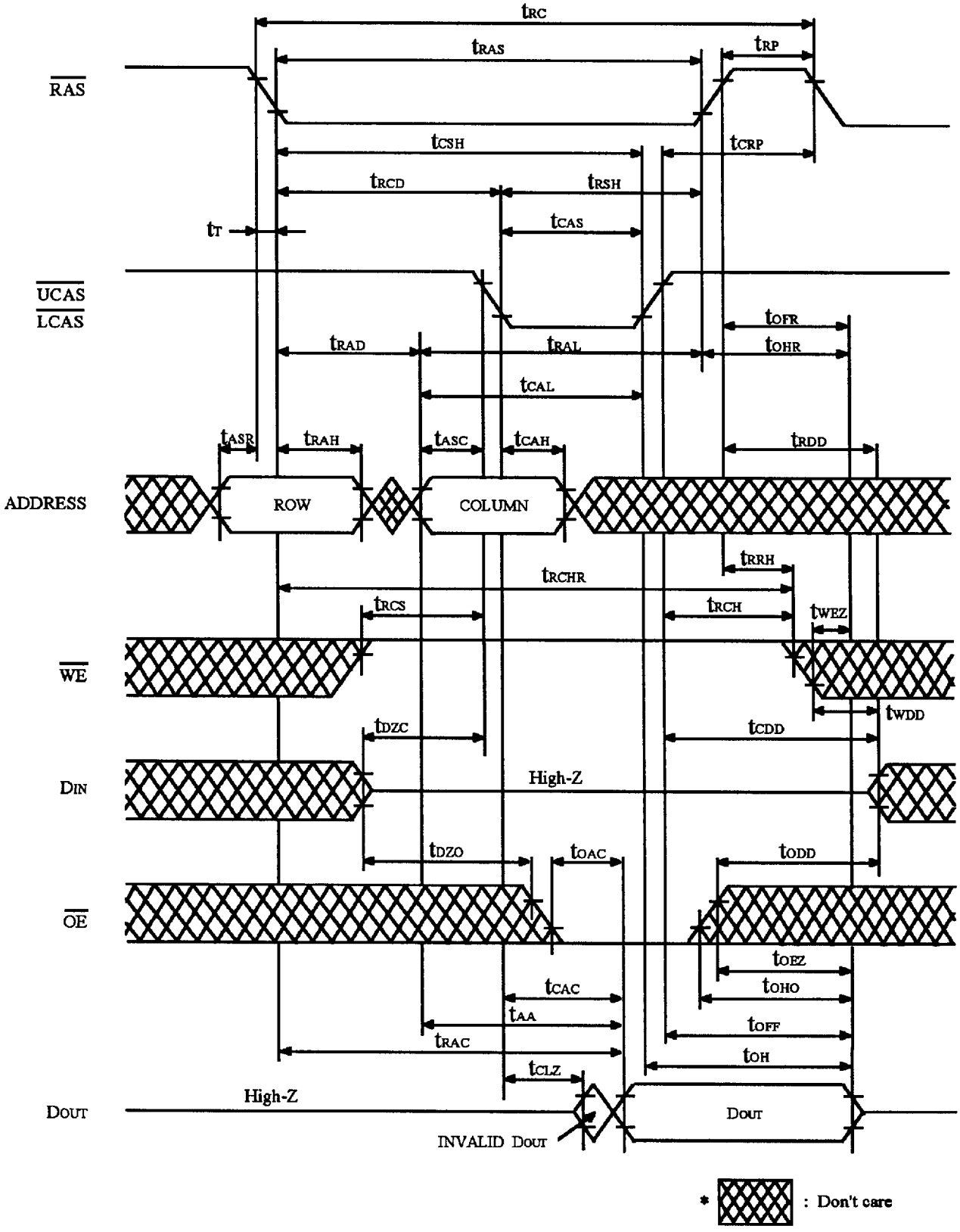


FIGURE 1. READ CYCLE

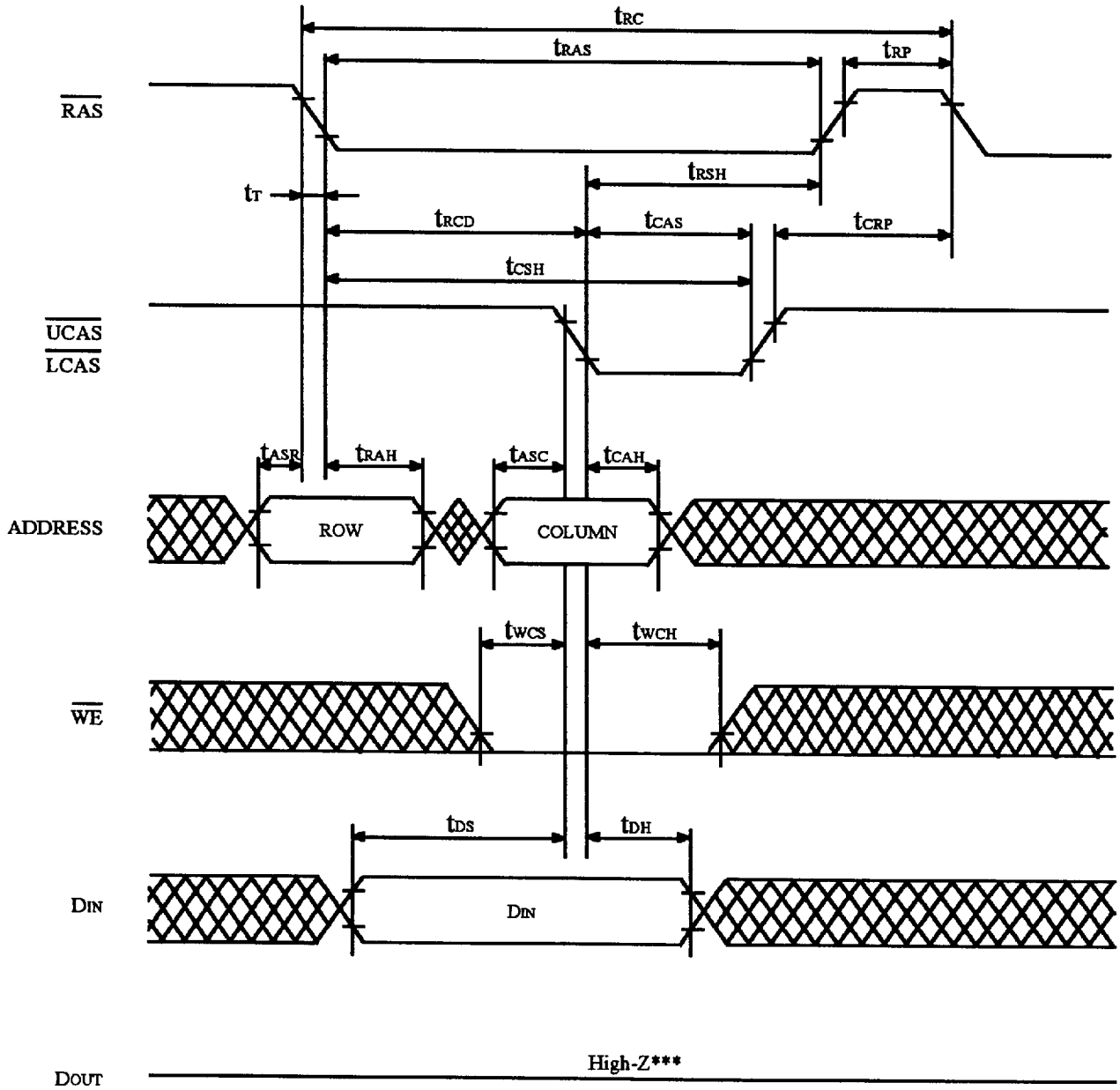


FIGURE 2. EARLY WRITE CYCLE

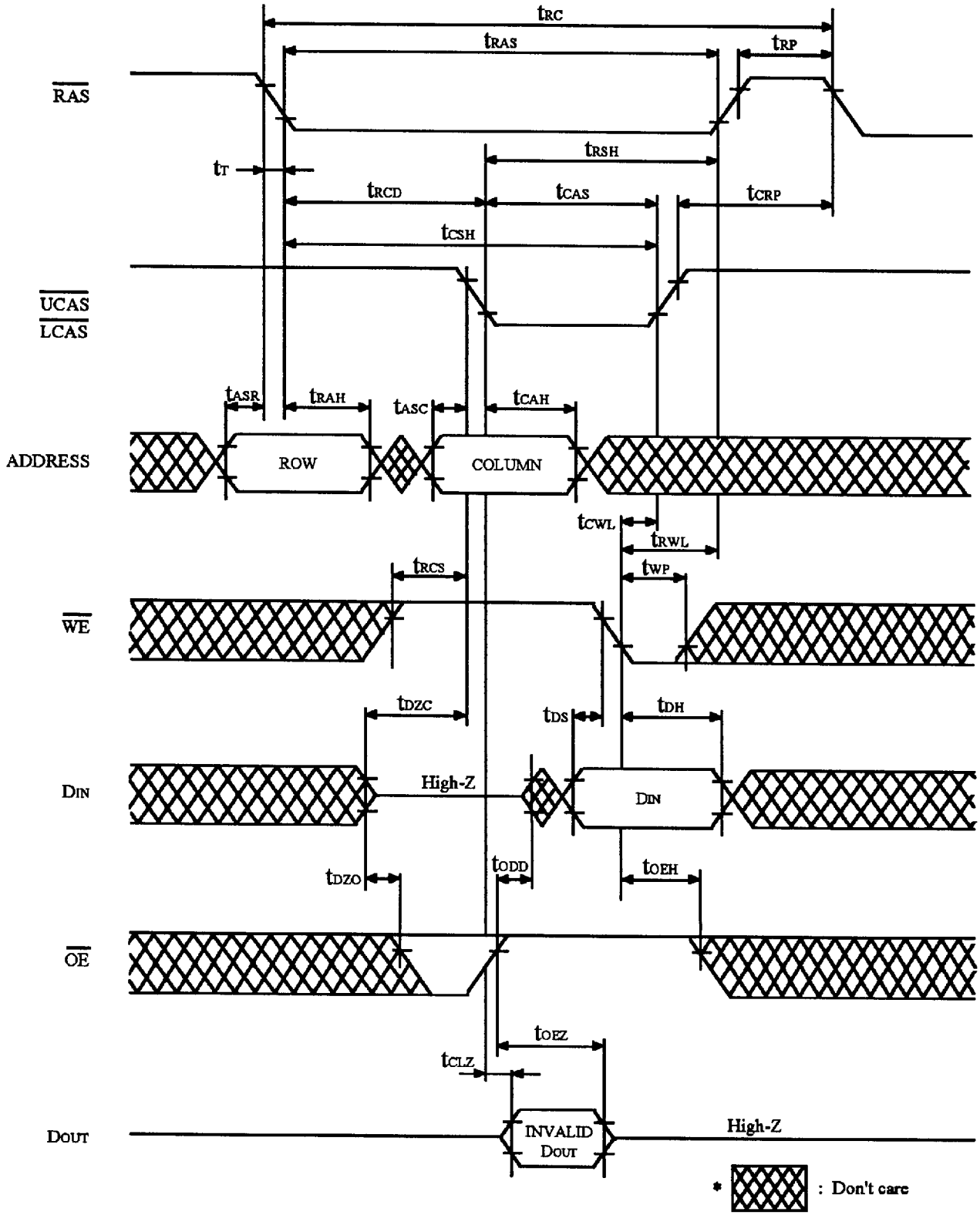


FIGURE 3. DELAYED WRITE CYCLE *18

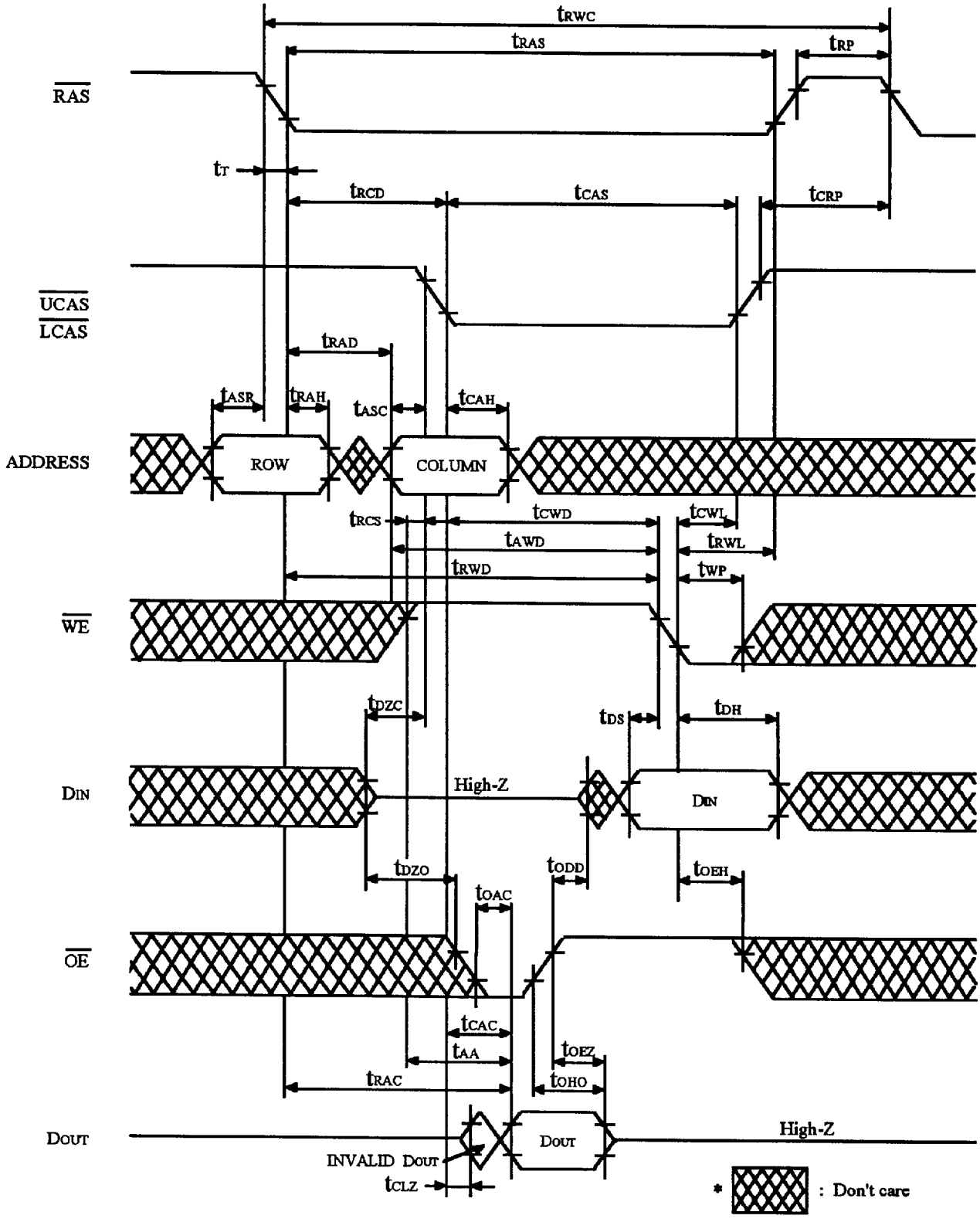
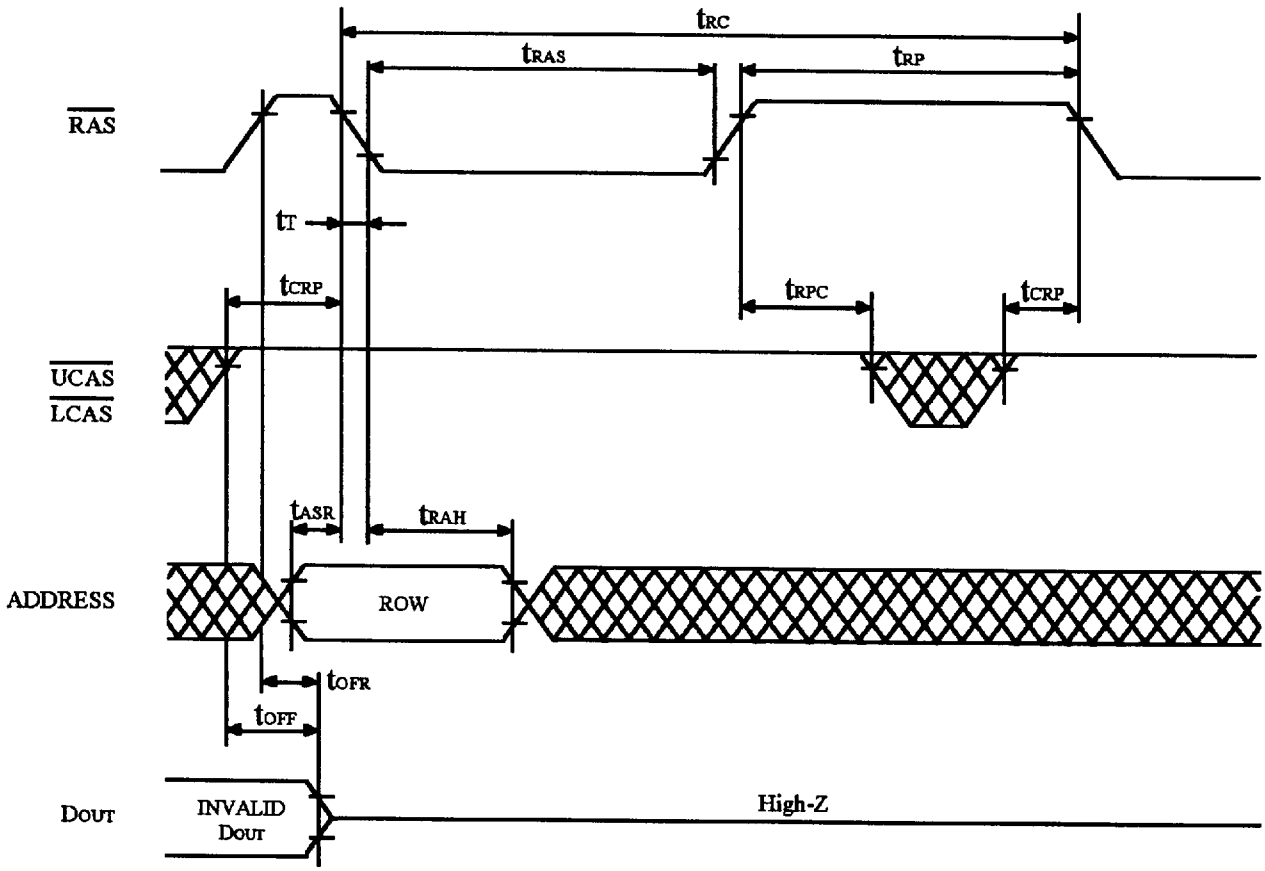


FIGURE 4. READ MODIFY WRITE CYCLE [*18]



* : Don't care

** $\overline{OE}$, $\overline{WE}$: Don't care

*** Refresh Address: A0-A9 (RA0-RA9)

FIGURE 5. $\overline{RAS}$ ONLY REFRESH CYCLE

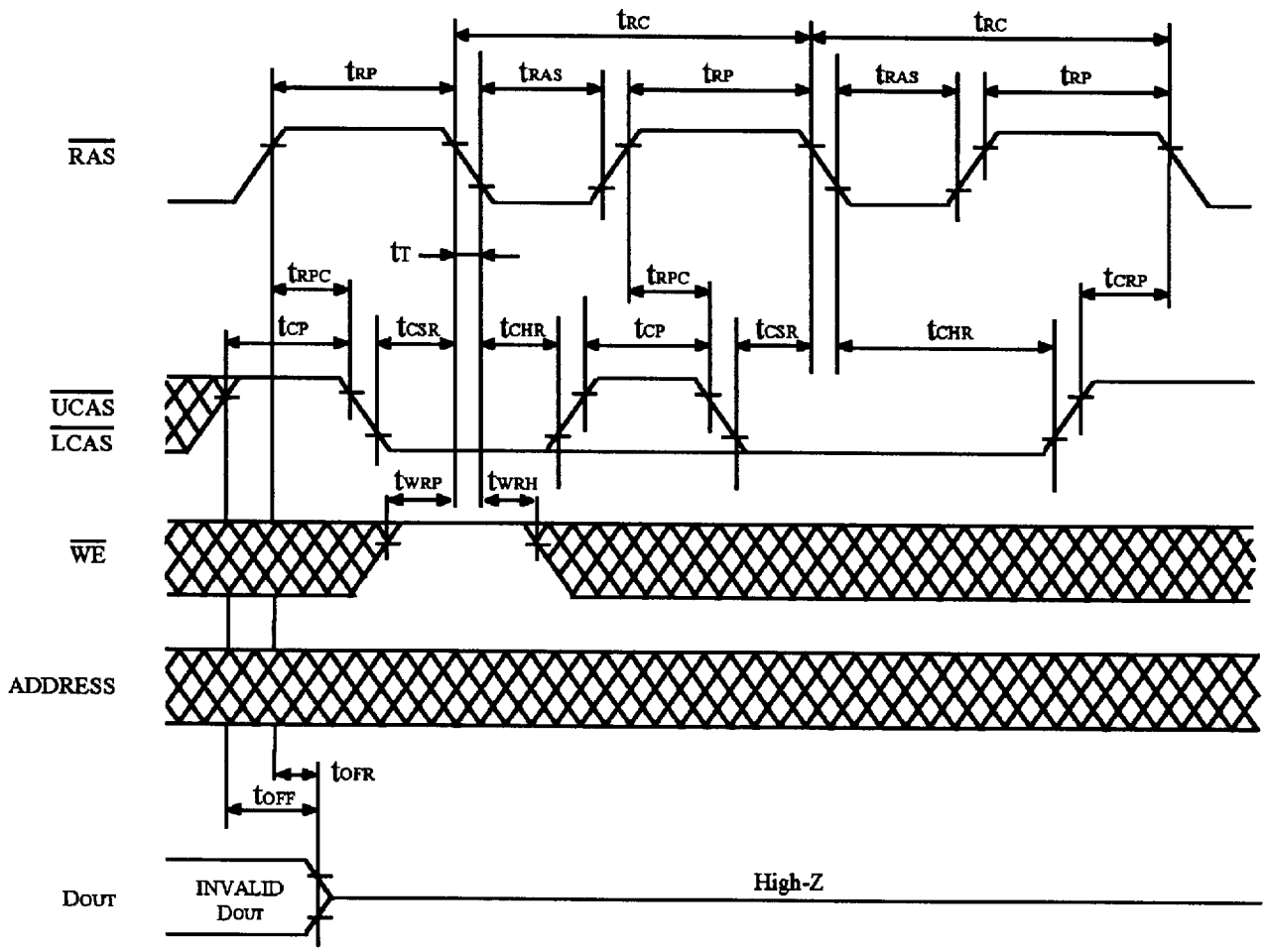


FIGURE 6. $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

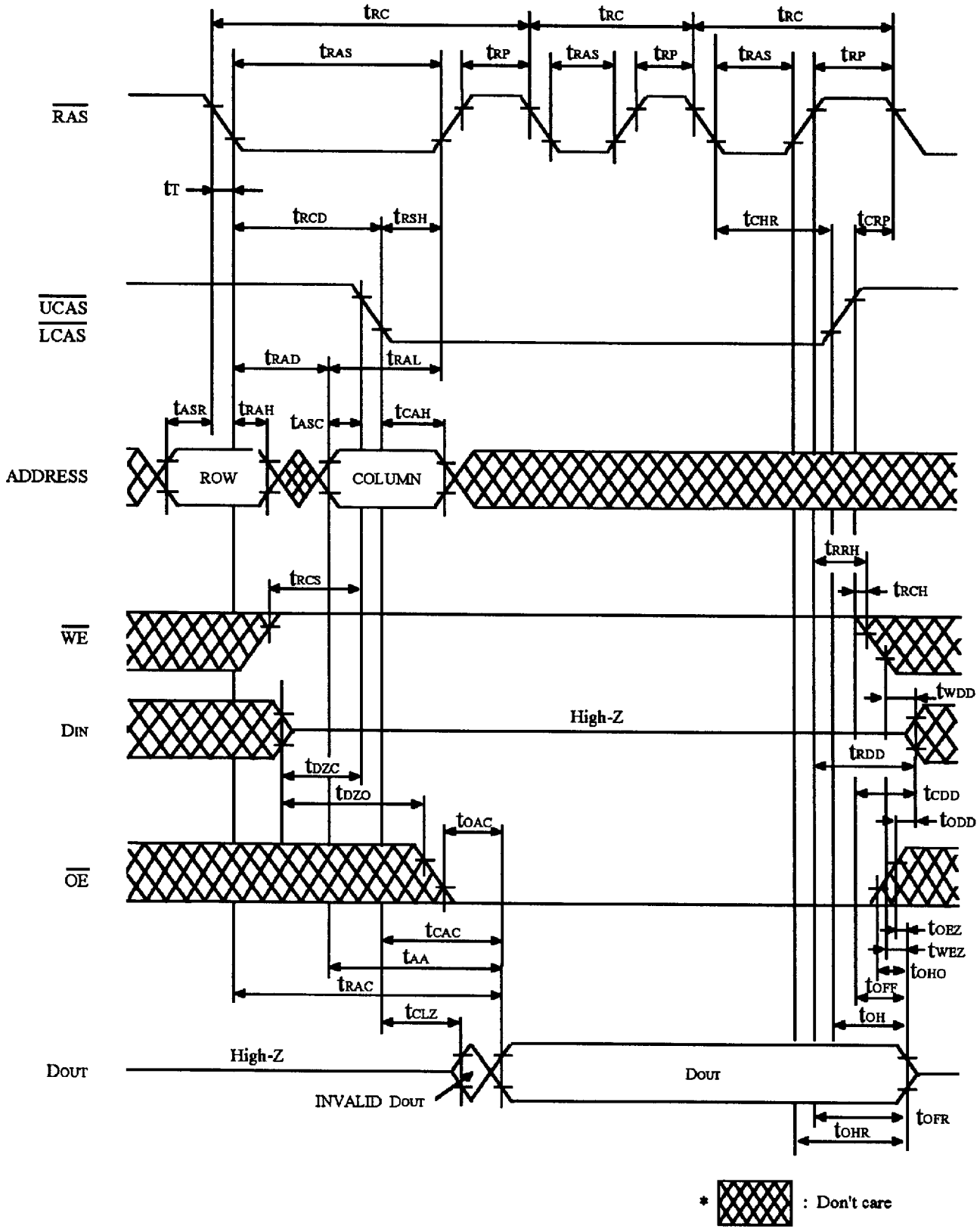


FIGURE 7. HIDDEN REFRESH CYCLE

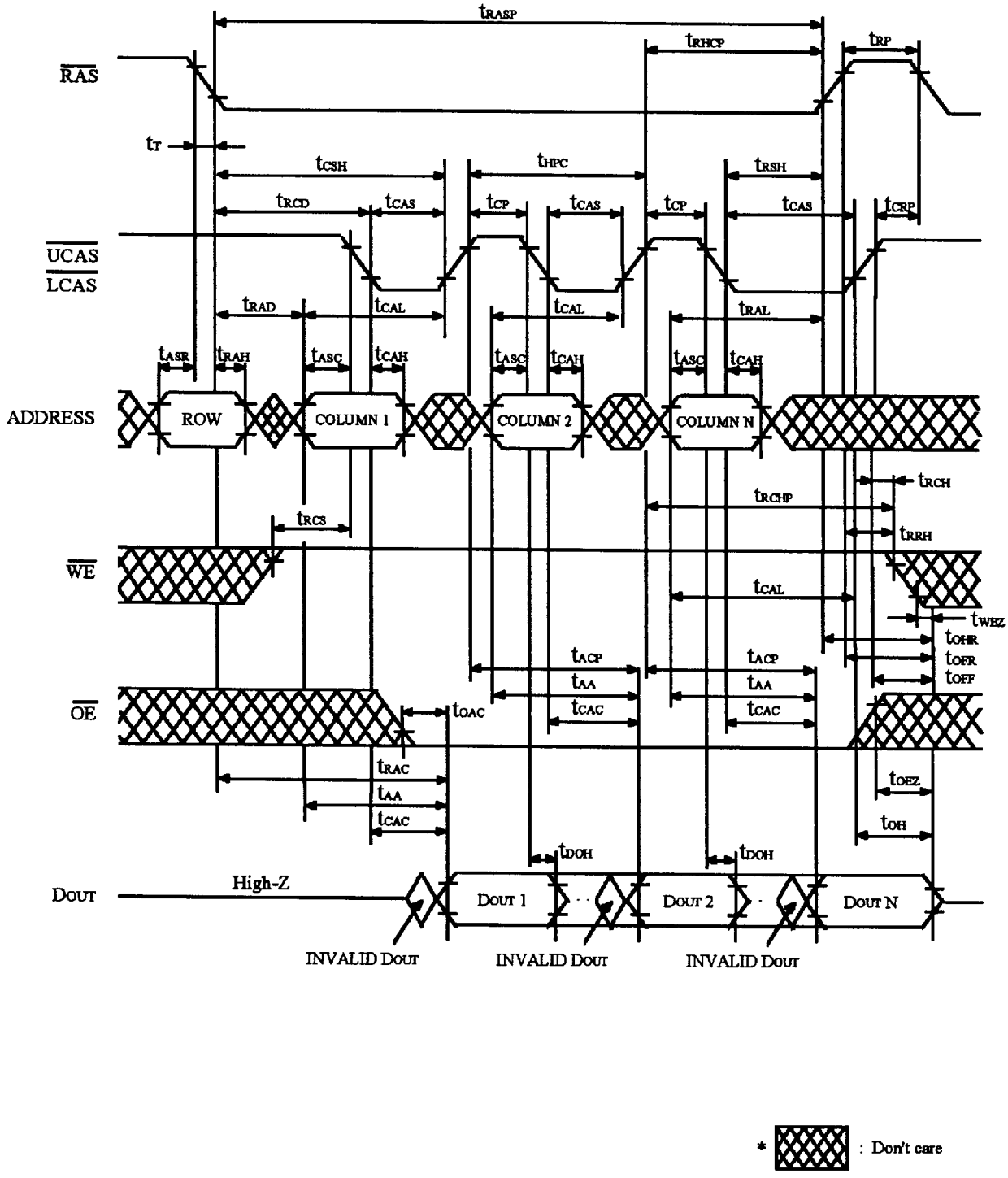


FIGURE 8. EXTENDED DATA OUT MODE READ CYCLE

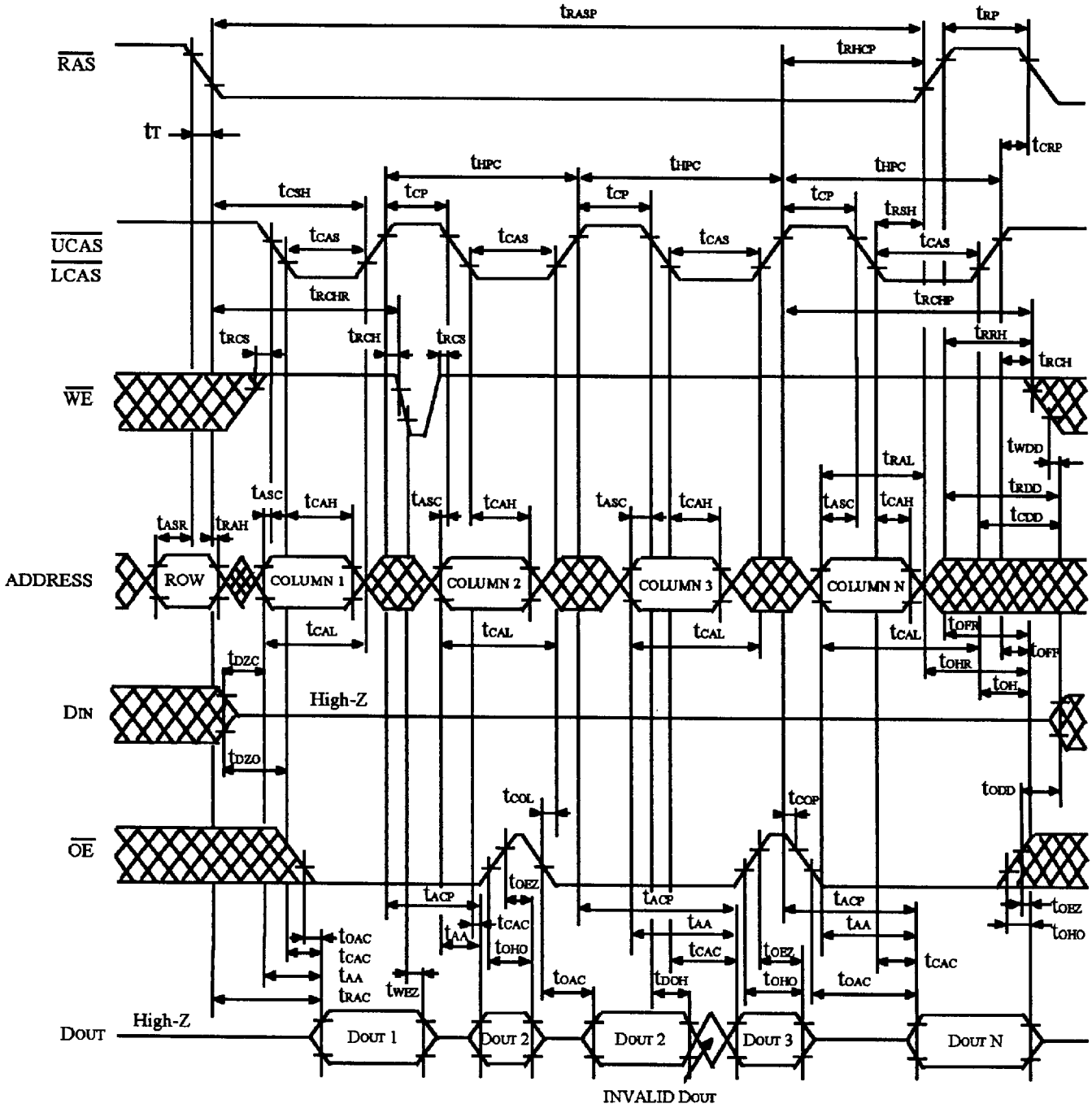


FIGURE 9. EXTENDED DATA OUT MODE READ CYCLE ($\overline{OE}$ CONTROL) *28

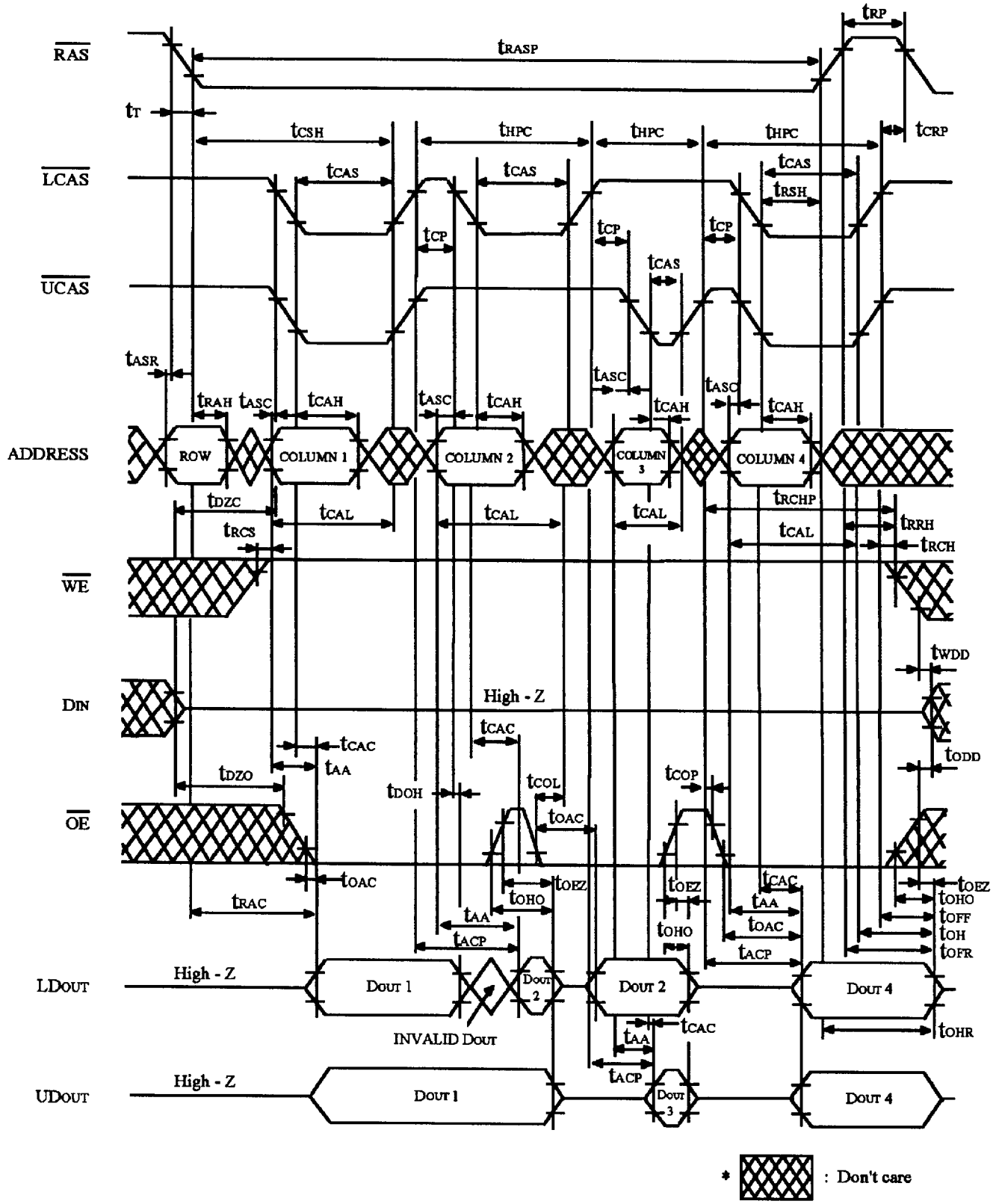


FIGURE 10. EXTENDED DATA OUT MODE READ CYCLE (2$\overline{CAS}$ TYPE)

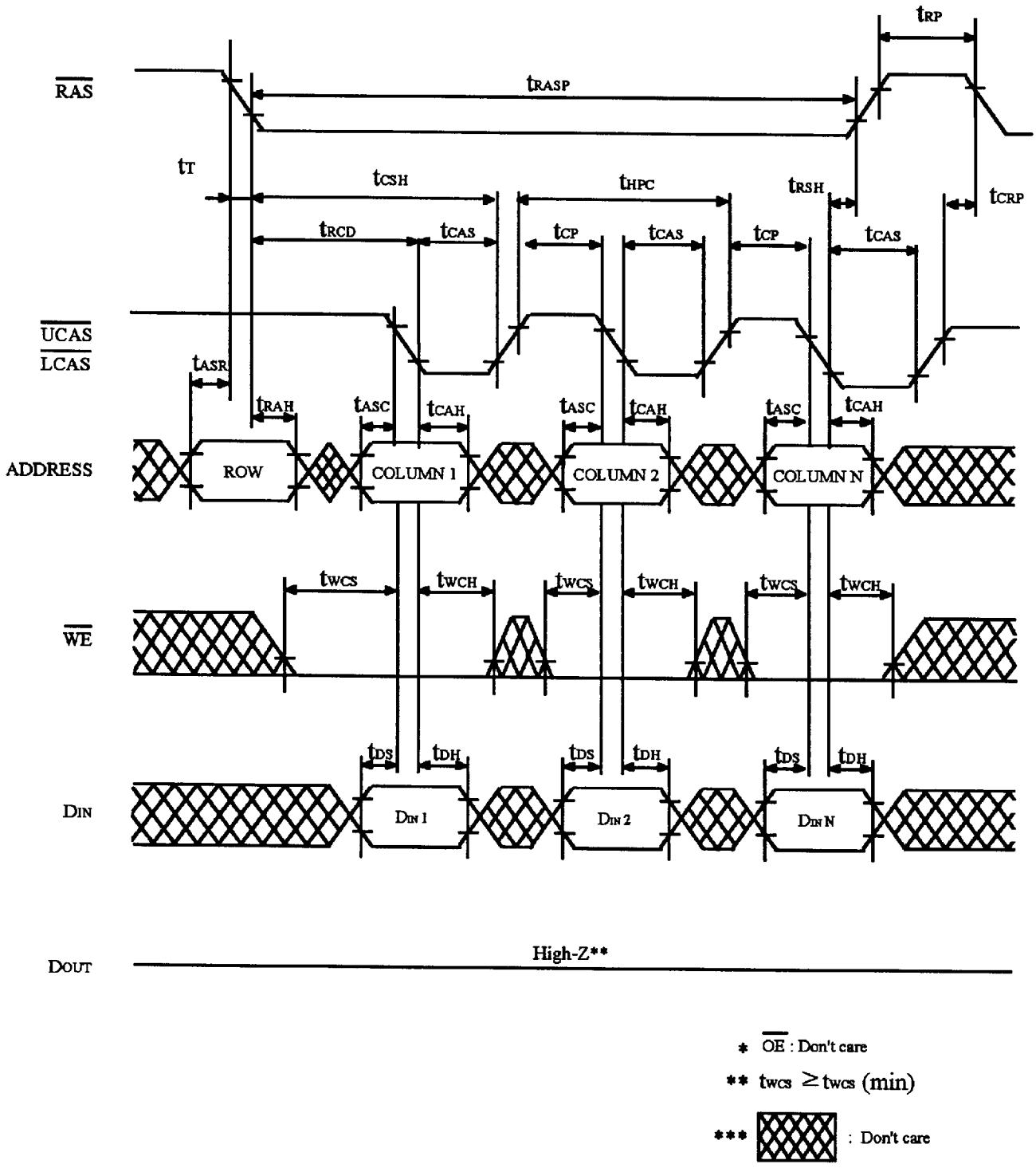


FIGURE 11. EXTENDED DATA OUT MODE EARLY WRITE CYCLE

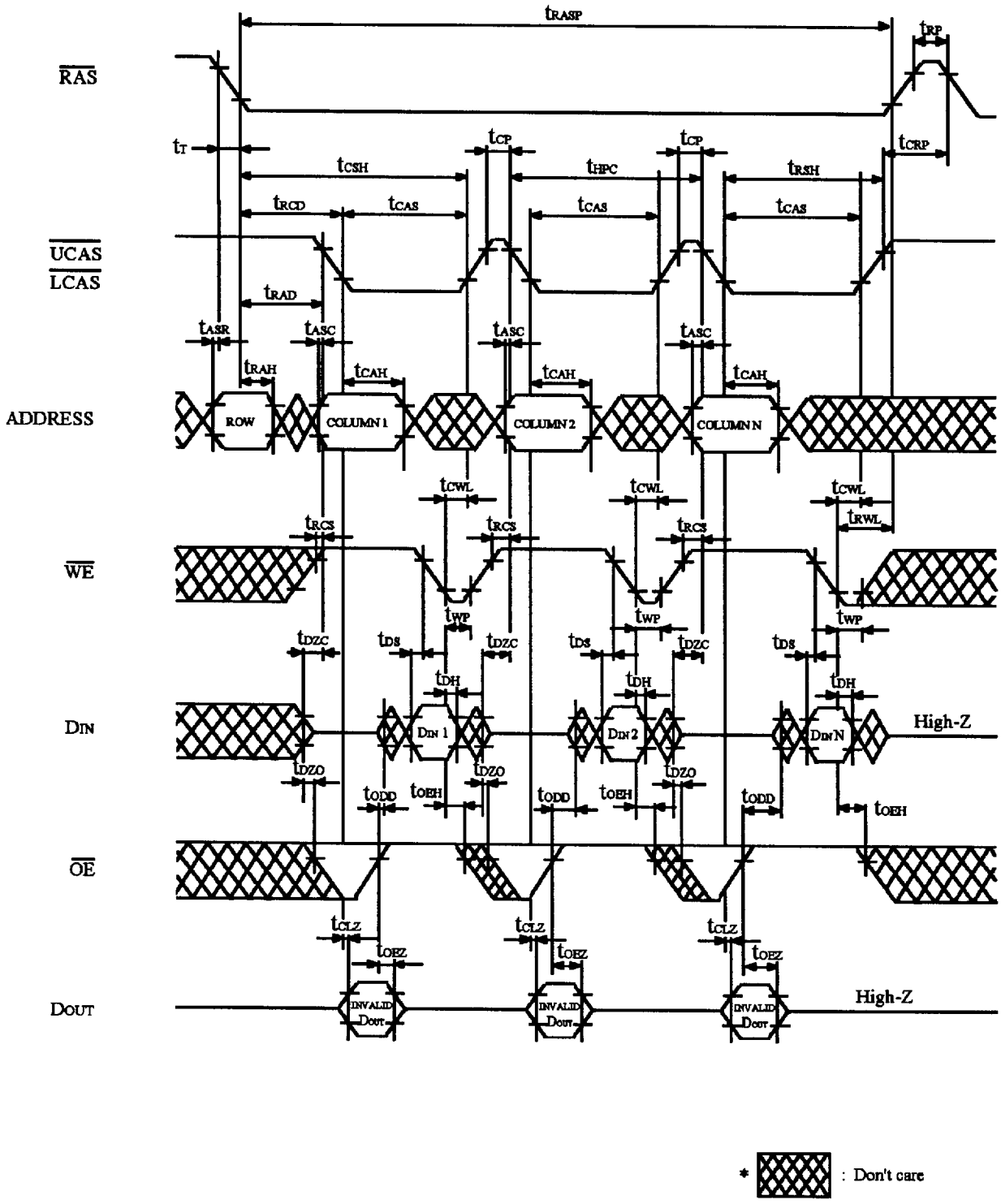


FIGURE 12. EXTENDED DATA OUT MODE DELAYED WRITE CYCLE *18

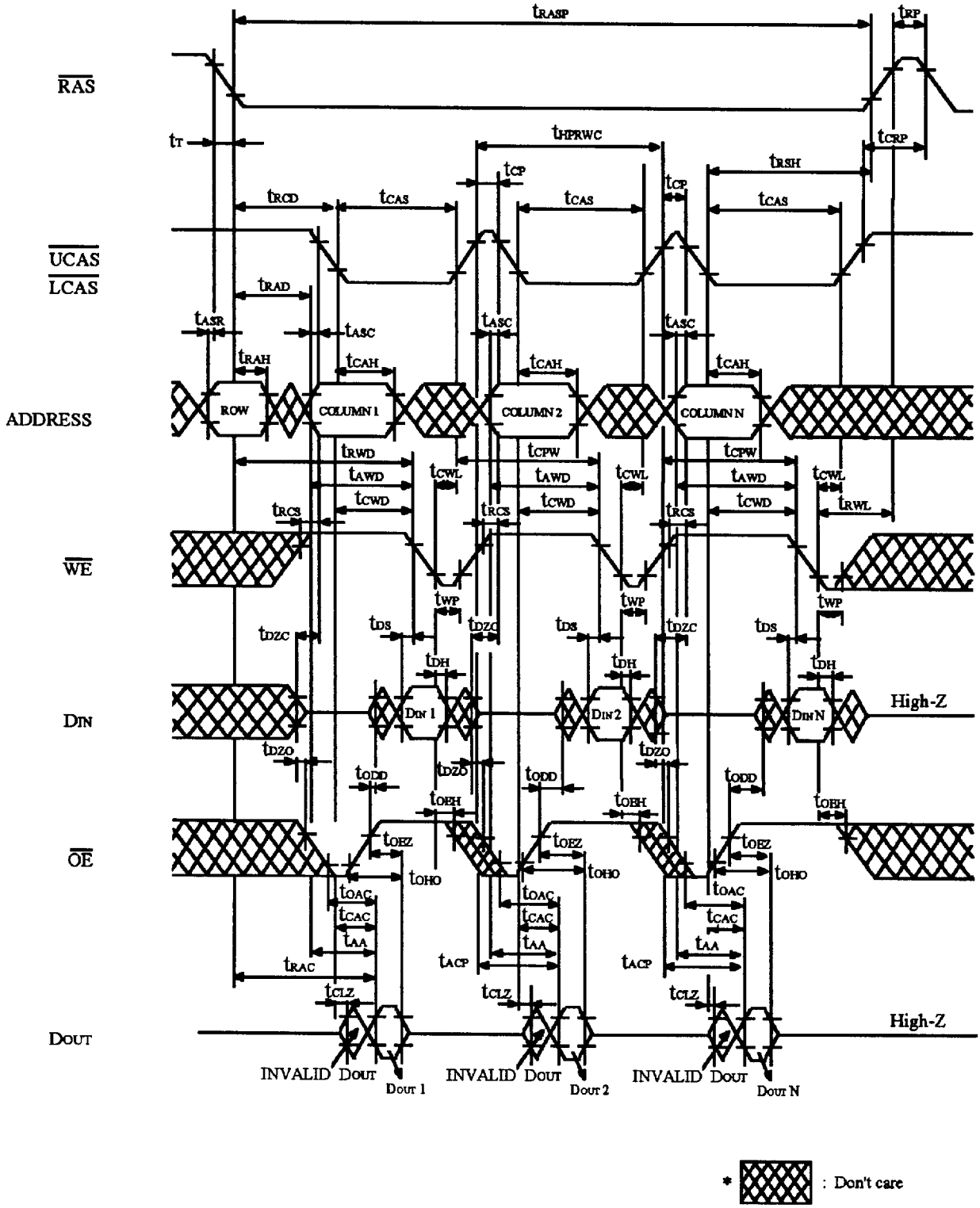


FIGURE 13. EXTENDED DATA OUT MODE READ MODIFY WRITE CYCLE [*18]

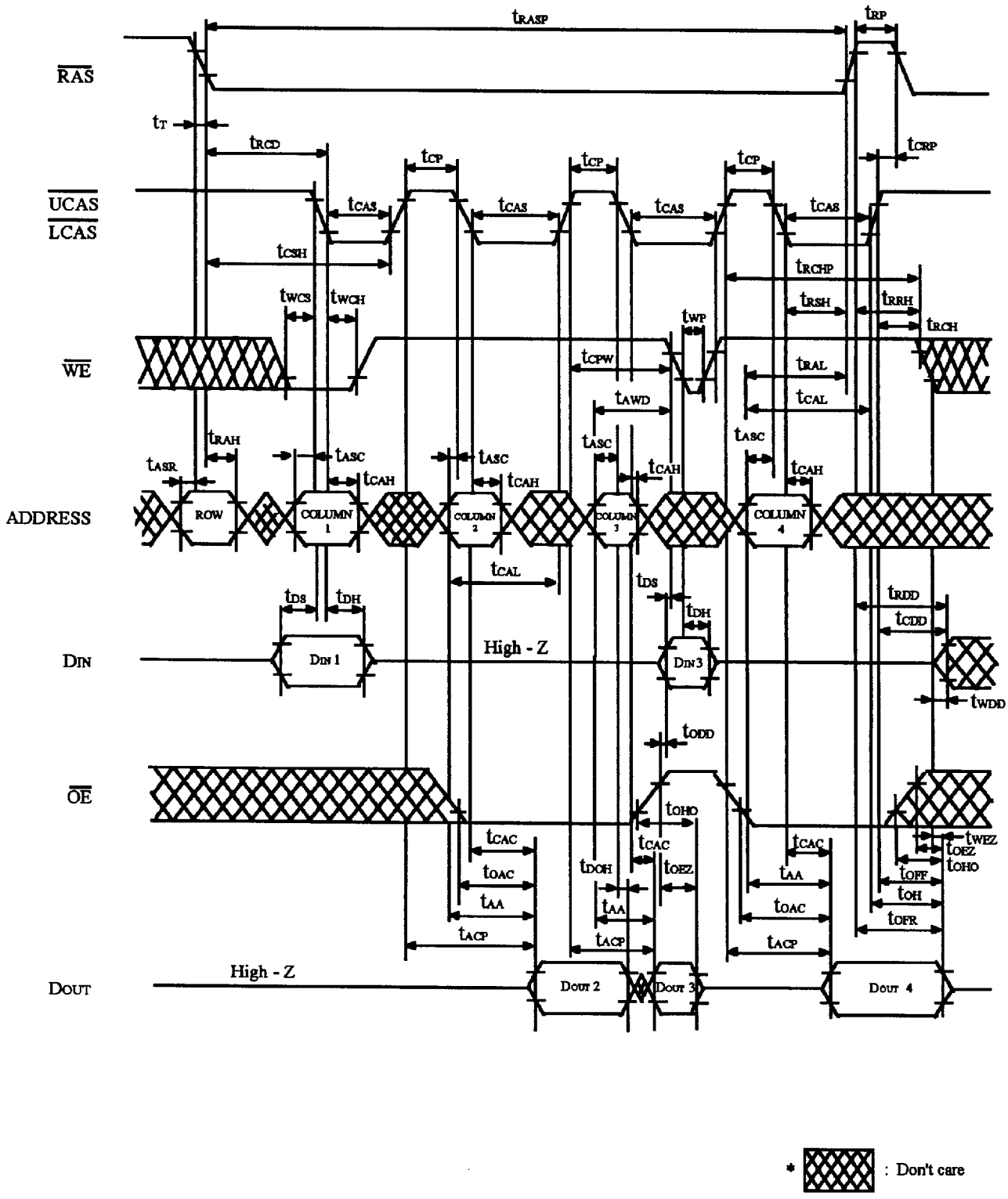


FIGURE 14. EXTENDED DATA OUT MODE MIX CYCLE (1) [*25]

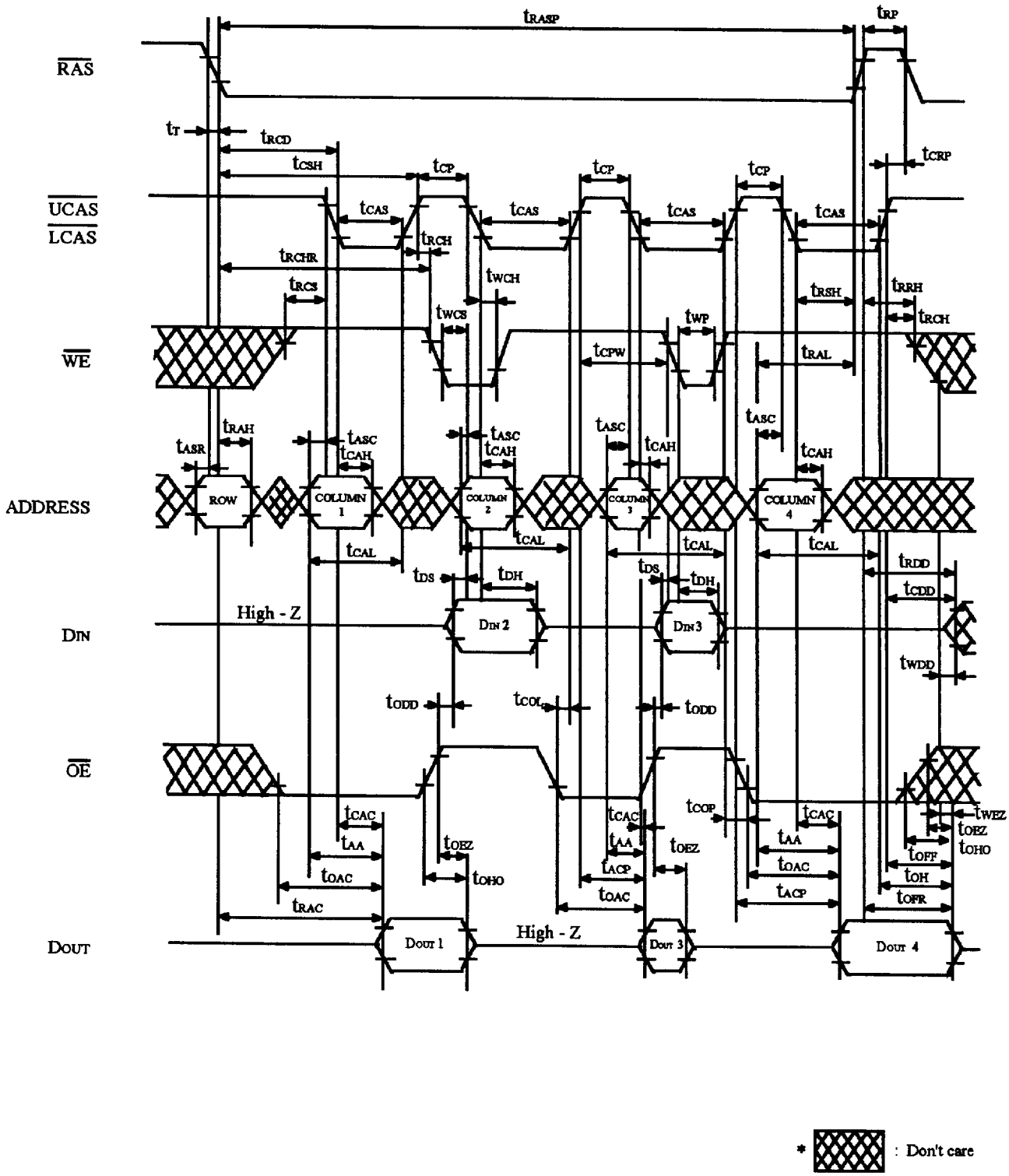
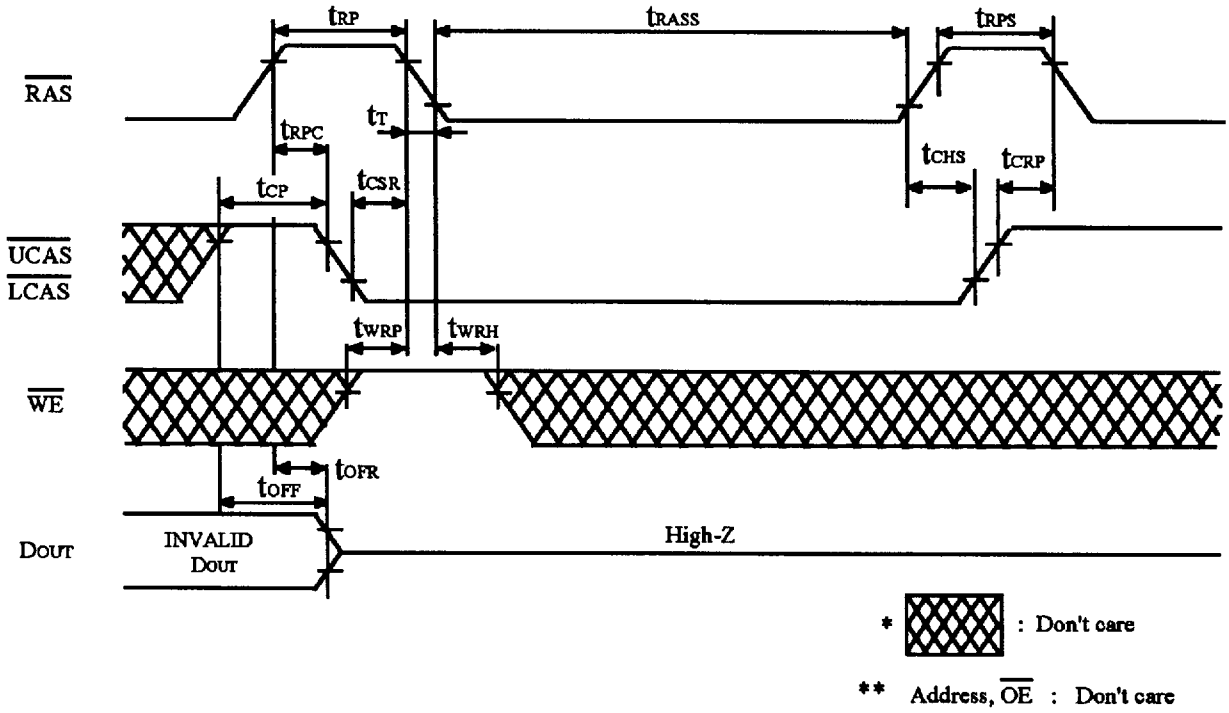


FIGURE 15. EXTENDED DATA OUT MODE MIX CYCLE (2) [25]



The low self refresh current is achieved by introducing extremely long internal refresh cycle. Therefore some care needs to be taken on the refresh.

1. Please do not t_{RASS} timing, $10\mu s \leq t_{RASS} \leq 100\mu s$. During this period, the device is in transition state from normal operation mode to self refresh mode. If $t_{RASS} \geq 100\mu s$, then $\overline{RAS}$ precharge time should use t_{RPS} instead of t_{RP}.
2. If you use $\overline{RAS}$ only refresh or CBR burst refresh mode in normal read/write cycle, 1024 cycles of distributed CBR refresh with 15.6μs interval should be executed within 16ms immediately after exiting from and before entering into the self refresh mode.
3. If you use distributed CBR refresh mode with 15.6μs interval in normal read/write cycle, CBR refresh should be executed within 15.6μs immediately after exiting from and before entering into the self refresh mode.
4. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.

FIGURE 16. SELF-REFRESH CYCLE

Package Dimensions

Unit: Inches (mm)

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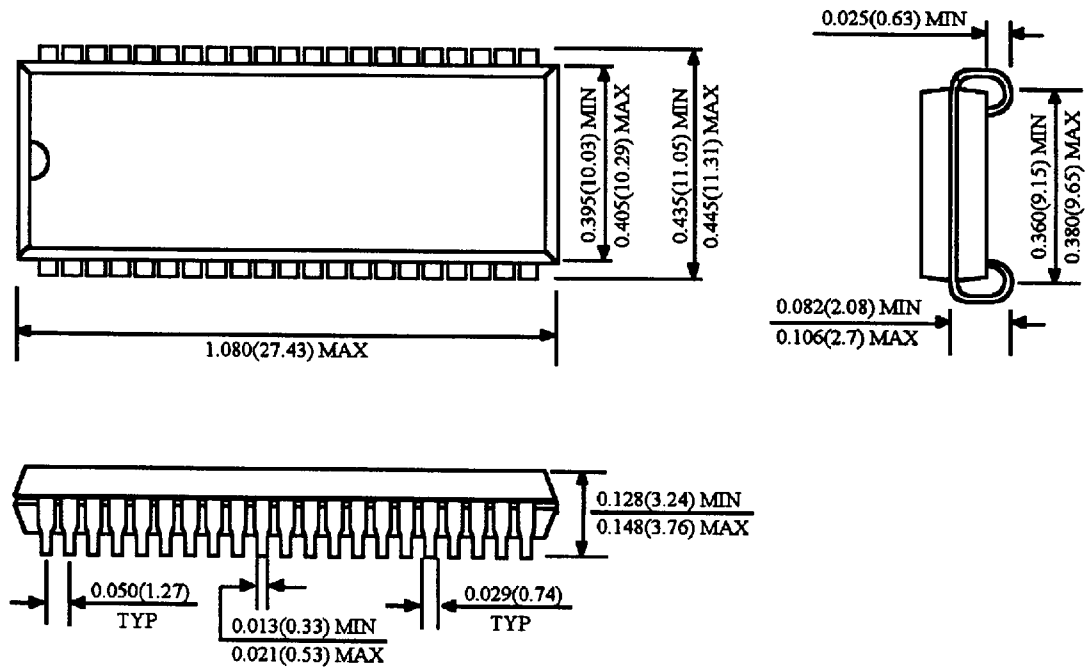

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