Winbond Electronics Corp.

256K x 32 bit x 2 Banks SGRAM

Features

- JEDEC standard 3.3V power supply
- Up to 143MHz clock frequency
- 262,144 words x 2 banks x 32 bits
- 1 Bank Select, Row Address A0~A9, Column Address A0~A7
- CAS Latency: 2 and 3
- Burst Length:1, 2, 4, 8 & full page
- Burst Type: Sequential & Interleave
- DQM 0-3 for byte masking
- Auto & self refresh
- Write Per Bit
- 8 columns Block Write
- 32ms refresh period, 2K cycle
- LVTTL compatible interface
- 100 Pin PQFP, TQFP (14 x 20 mm)

General Description

W971632AF is a 16,777216-bit synchronous graphic memory organized as 262,144 words x 2 banks x 32 bits. Using synchronous pipelined architecture, W971632AF delivers a data transmission rate of up to 143M words per second.

Accesses to the SGRAM are burst oriented. Consecutive memory location in one page can be accessed at a burst length of 1, 2, 4, 8 or full page when a bank and row is selected by an ACTIVE command. Column addresses are automatically generated by the SGRAM internal counter in burst operation. Random column read is also possible by providing its address at each clock cycle. The multiple bank nature enables interleaving among internal banks to hide the precharging time. Using a pogrammable Mode Register, the system can change burst length, latency cycle, interleave or sequential burst to maximize its performance.

With write-per-bit and block-write functions, W971632AF is optimized for graphics drawing operation.

Key Parameters

Symbol	Description	min/max	-7	-8	-10
t_{CK}	Clock Cycle Time	min	7ns	8ns	10ns
t_{AC}	Access Time from CLK	max	6ns	6.5ns	7ns
t_{RP}	Precharge to Active Command	min	21ns	24ns	30ns
t_{RCD}	Active to Read/Write Command	min	21ns	24ns	30ns
I_{CC1}	Operation Current (Single bank)	max	90mA	90mA	70mA
I_{CC4}	Burst Operation Current	max	165mA	135mA	115mA
I_{CC6}	Self-Refresh Current	max	1mA	1mA	1mA

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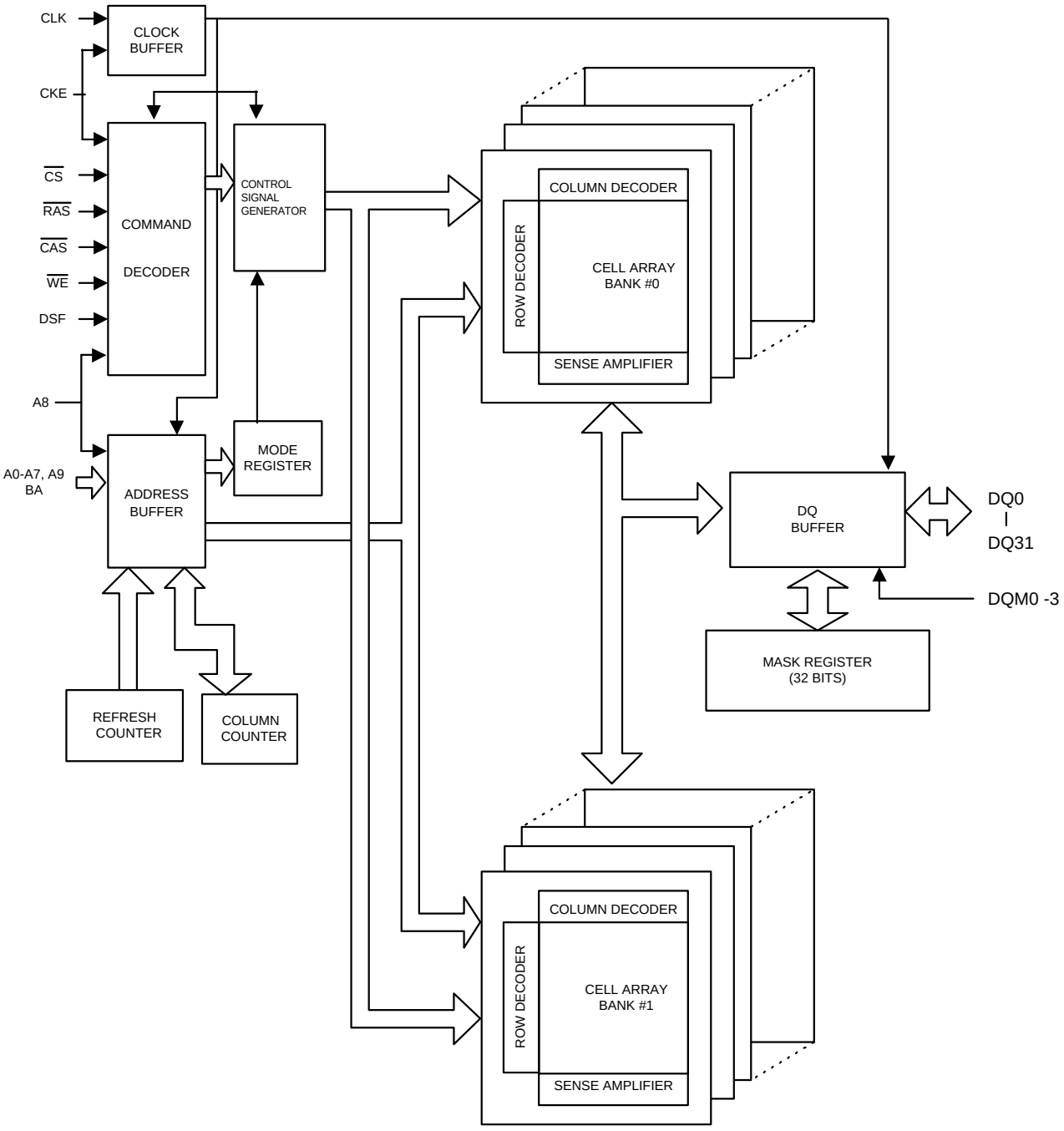
BLOCK DIAGRAM



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Pin Assignment

Pin Number	Pin Name	Function	Description
30,31~34, 47~51	A9, A0~A3, A4~8	Address	Multiplexed pins for row and column address. Row address: A0 ~ A9. Column address: A0 ~ A7.
29	BA(A10)	Bank Select	Select bank for BankActive, Read, Write, or Bank Precharge command.
1, 3, 4, 6, 7, 9, 10, 12, 13, 17, 18, 20, 21, 60, 61, 63, 64, 68, 69, 71, 72, 74, 75, 77, 78, 80, 81, 83, 84, 97, 98, 100	DQ0~ DQ31	Data Input/ Output	DQ0~31 are used as data input and output. These pins are masked during reads and writes by DQM0~3 for each byte.
28	CS#	Chip Select	Disable or enable the command decoder. When command decoder is disabled, new command is ignored and previous operation continues. System use CS# for multichip selection.
27	RAS#	Row Address Strobe	RAS#, CAS# and WE# define the operation to be executed.
26	CAS#	Column Address Strobe	Referred to RAS#
25	WE#	Write Enable	Referred to RAS#
55	CLK	Clock Inputs	System clock used to sample inputs on the rising edge of clock.
54	CKE	Clock Enable	CKE controls the clock activation and deactivation to chip. When CKE goes low, chip internal clock is suspended. Power Down mode, Suspend mode, or Self Refresh mode needs CKE goes low.
53	DSF	Define Special Function	Used with RAS, CAS, WE to define commands like mask write, block write, and Special Mode Register Set cycle.
23, 24, 56, 57	DQM0~DQM3	Data Input/Output Mask	DQM high mask input/output data from write and read, or put DQ in High Z. DQM0 mask DQ0~7, DQM1 for DQ8~15, DQM2 for DQ16~23, DQM3 for DQ24~31.
15, 35, 65, 96	V_{CC}	Power (+3.3 V)	3.3V input for chip logic and input buffers
16, 46, 66, 85	V_{SS}	Ground	Ground for chip internal logic and input buffers
2, 8, 14, 22, 59, 67, 73, 79	$V_{CC}Q$	Power (+ 3.3 V) for I/O buffer	Separated power from V_{CC} to improve DQ noise immunity.
5, 11, 19, 62, 70, 76, 82, 99	$V_{SS}Q$	Ground for I/O buffer	Separated ground from V_{SS} to improve output buffers noise immunity.
30, 36-45, 52, 58, 86-95	NC	No Connection	No connection

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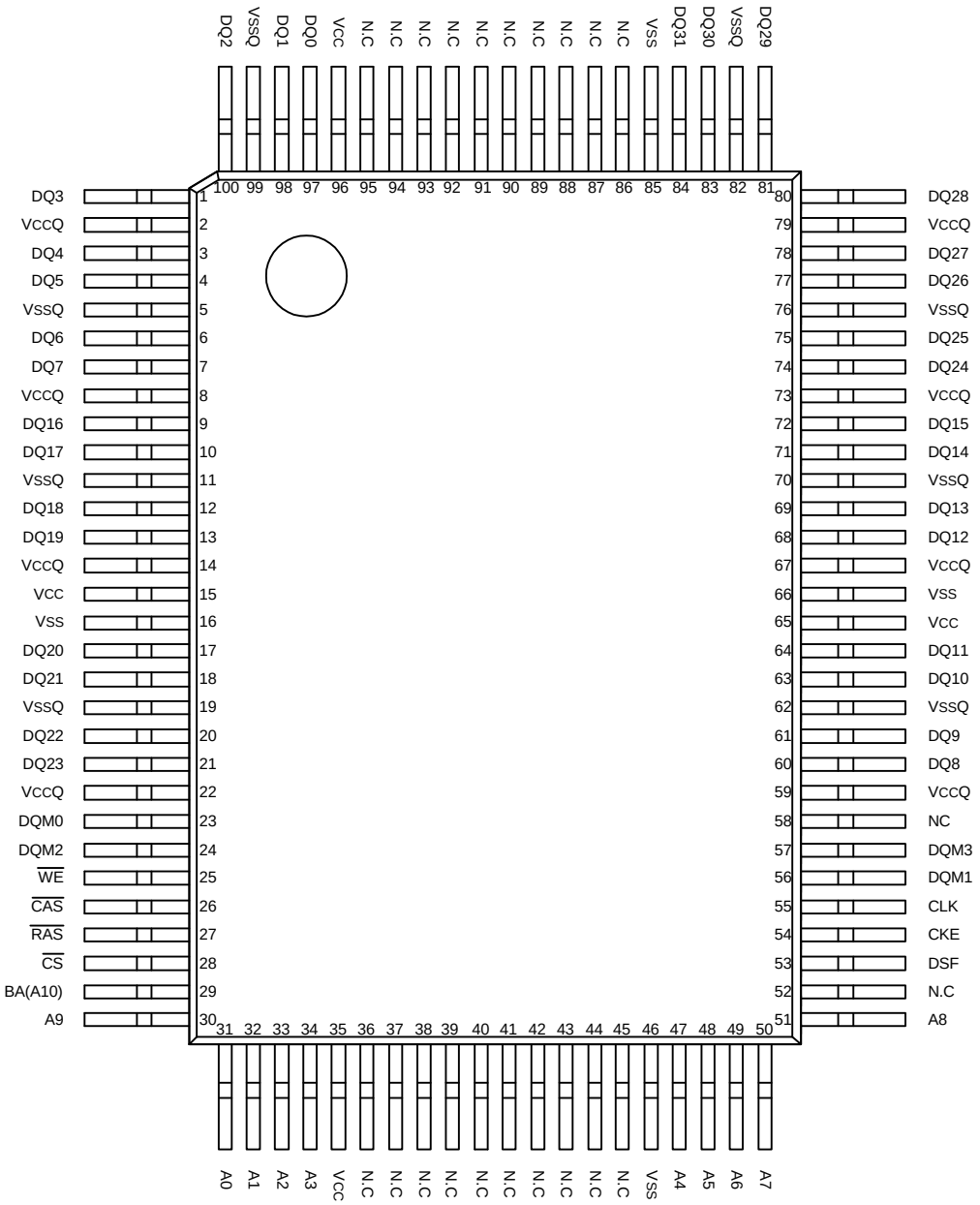
Pin Assignment (Top View)



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN},V_{OUT}	Input/Output Voltage	-0.3~4.6	V	1
V_{CC},$V_{CC}Q$	Power Supply Voltage	-0.3~4.6	V	1
T_{OPR}	Operating Temperature	0~70	°C	1
T_{STG}	Storage Temperature	-55~150	°C	1
T_{SOLDER}	Soldering Temperature(10s)	260	°C	1
P_D	Power Dissipation	1	W	1
I_{OS}	Short Circuit Output Current	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0 to 70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	NOTES
V_{CC}	Power Supply Voltage	3.0	3.3	3.6	V	2
$V_{CC}Q$	Power Supply Voltage (for I/O Buffer)	3.0	3.3	3.6	V	2
V_{IH}	LVTTL Input High Voltage	2.0	3.0	V_{CC}+0.3	V	2
V_{IL}	LVTTL Input Low Voltage	-0.3	0	0.8	V	2

Note: V_{IH}(max) = V_{CC}/$V_{CC}Q$+1.2V for pulse width ≤ 5ns
V_{IL}(min) = V_{SS}/$V_{SS}Q$-1.2V for pulse width ≤ 5ns

CAPACITANCE (V_{CC}=3.3V, Af = 1MHz, Ta=23°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_I	Input Capacitance (A0 to A9, BS, CS#, RAS#, CAS#, WE#, DQM0-3, CKE)	2.5	4.0	pF
	Input Capacitance (CLK)	2.5	4.0	pF
C_O	Input/Output capacitance	4.0	5.0	pF

Note: These parameters are periodically sampled and not 100% tested.

AC CHARACTERISTICS AND OPERATING CONDITION (5, 6, 7)

(Vcc=3.3V±0.3V, Ta=0° to 70°C)

SYMBOL	PARAMETER	-7		-8		-10		UNIT	NOTE
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Ref/Active to Ref/Active Command Period	70		72		80			
t_{RAS}	Active to Precharge Command Period	49	100000	48	100000	50	100000		
t_{RCD}	Active to Read/Write Command Delay	21		24		30			
t_{CCD}	Read/Write to Read/Write Command Period	7		8		10			
t_{RP}	Precharge to Active Command Period	21		24		30			
t_{RRD}	Active to Active Command Period	14		16		20			
t_{WR}	Write Recovery Time	7		8		10			
t_{CK}	CLK Cycle Time (CL=3)	7	1000	8	1000	10	1000		
	CLK Cycle Time (CL=2)	12		13		15			
t_{CH}	CLK High Level width	2.5		3		3.5			
t_{CL}	CLK Low Level width	2.5		3		3.5			
t_{AC}	Access Time from CLK (CL=3)		6		6.5		7		
	Access Time from CLK (CL=2)		7		7		8		
t_{OH}	Output Data Hold Time	2.5		2.5		2.5		ns	
t_{HZ}	Output Data High Impedance Time		6		6.5		7		8
t_{LZ}	Output Data Low Impedance Time	1		1		1			8
t_T	Transition Time of CLK (Rise and Fall)	0.5	10	1	10	1	10		
t_{DS}	Data-in Set-up Time	2		2.5		2.5			
t_{DH}	Data-in Hold Time	1		1		1			
t_{AS}	Address Set-up Time	2		2.5		2.5			
t_{AH}	Address Hold Time	1		1		1			
t_{CKS}	CKE Set-up Time	2		2.5		2.5			
t_{CKH}	CKE Hold Time	1		1		1			
t_{CMS}	Command Set-up Time	2		2.5		2.5			
t_{CMH}	Command Hold Time	1		1		1			
t_{REF}	Refresh Time		32		32		32	ms	
t_{RSC}	Mode Register Set Cycle Time	14		16		20		ns	
t_{BWC}	Block Write Cycle Time	7		8		10			
t_{BWL}	Block Write to precharge Time	7		8		10			

(CL=CAS Latency)

DC CHARACTERISTICS (V_{CC} = 3.3V ± 0.3V, Ta=0°~70°C)

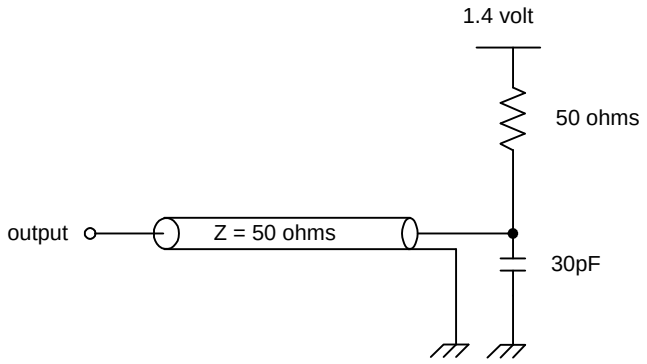
ITEMS		SYMBOL	-7		-8		-10		UNIT	NOTES
			MIN.	MAX	MIN.	MAX	MIN.	MAX		
OPERATING CURRENT t_{CK}≥min, t_{RC}≥min I_{OL}=0mA Active One bank, Precharge command cycling without Burst operation	1 bank operation	I_{CC1}		165		135		115	mA	3
STANDBY CURRENT t_{CK}=15ns $V_{IH/L}$=$V_{IH(min)}$/$V_{IL(max)}$ Bank : inactive state	CKE ≥ V_{IH}, CS# ≥ V_{IH},	I_{CC2N}		65		55		50		3
	CKE ≤ V_{IL} (Power Down mode)	I_{CC2P}		2		2		2		3
STANDBY CURRENT t_{CK}=∞, CLK≤V_{IL}, $V_{IH/L}$=V_{IH}(min)/V_{IL}(max) BANK : inactive state	CKE ≥ V_{IH}	I_{CC2NS}		15		15		15		
	CKE ≤ V_{IL} (Power Down mode)	I_{CC2PS}		2		2		2		
NO OPERATING CURRENT t_{CK}=15ns Bank : active state (1 bank)	CKE ≥ V_{IH}, CS# ≥ V_{IH},	I_{CC3N}		70		60		55		
	CKE ≤ V_{IL}(Power Down mode)	I_{CC3P}		4		4		4		
NO OPERATING CURRENT t_{CK}=∞, CLK≤V_{IL}, Bank : active state (1 bank)	CKE ≥ V_{IH}	I_{CC3NS}		15		15		15		
	CKE ≤ V_{IL}(Power Down mode)	I_{CC3PS}		2		2		2		
BURST OPERATING CURRENT t_{CK}=min, I_{OL}=0mA, CL=3 All bank active Read / Write command cycling		I_{CC4}		170		160		150		3,4
AUTO REFRESH CURRENT t_{CCD}=min Auto Refresh command cycling		I_{CC5}		130		120		110		3
SELF REFRESH CURRENT Self Refresh mode CKE ≤ 0.2V		I_{CC6}		1		1		1		
OPERATING CURRENT t_{CK}≥min, I_{OL}=0mA, t_{BWL}(min)		I_{CC7}		90		90		70		

ITEM	SYMBOL	MIN.	MAX.	UNIT	NOTES
INPUT LEAKAGE CURRENT (0V ≤ V_{IN} ≤ V_{CC} , all other pins not under test = 0V)	I_{IL}	-5	5	µA	
OUTPUT LEAKAGE CURRENT (Output disable, 0V ≤ V_{OUT} ≤ V_{CC}Q)	I_{OL}	-5	5	µA	
LVTTL OUTPUT ˝H˝ LEVEL VOLTAGE (I_{OUT} = -2mA)	V_{OH}	2.4	-	V	
LVTTL OUTPUT ˝L˝ LEVEL VOLTAGE (I_{OUT} = 2mA)	V_{OL}	-	0.4	V	

NOTES:

1. Operation exceeds "ABSOLUTE MAXIMUM RATING" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}
3. These parameters are dependent on cycle rate and listed values are measured at a cycle rate with the minimum values of t_{CK} and t_{RC}.
4. These parameters are dependent on output loading. Specified values are obtained with the outputs open.
5. Power up sequence is further described in the "Functional Description" section.
6. AC TESTING CONDITIONS

Output Reference Level	1.4V/1.4V
Output Load	See diagram A below
Input Signal Levels	2.4V/0.4V
Transition Time (Rise and Fall) of Input Signal	2ns
Input Reference Level	1.4V



AC TEST LOAD (A)

7. Transition times are measured between V_{IH} and V_{IL}.
8. t_{HZ} defines the time at which the outputs achieve the open circuit condition.

Operation Mode

Fully synchronous operations are performed to latch the commands at the positive edges of CLK. The truth table for the operation commands.

Truth Table (note (1) , (2))

Command	Current State	CKEn-1	CKEn	DQM(7)	BS	A8	A0-7, 9	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF
Bank Active & Mask Write Disable	Idle(3)	H	X	X	V	V	V	L	L	H	H	L
Bank Active & Mask write Enable	Idle(3)	H	X	X	V	V	V	L	L	H	H	H
Bank Prechage	Any	H	X	X	V	L	X	L	L	H	L	L
Precharge All	Any	H	X	X	X	H	X	L	L	H	L	L
Write	Active(3)	H	X	X	V	L	V	L	H	L	L	L
Mask Block Write	Active(3)	H	X	X	V	L	V	L	H	L	L	H
Write with Auto Precharge	Active(3)	H	X	X	V	H	V	L	H	L	L	L
Mask BW with Auto Precharge	Active(3)	H	X	X	V	H	V	L	H	L	L	H
Read	Active(3)	H	X	X	V	L	V	L	H	L	H	L
Read with Auto Precharge	Active(3)	H	X	X	V	H	V	L	H	L	H	L
Mode Register Set	Idle	H	X	X	V	V	V	L	L	L	L	L
Special Mode Register Set	Idle(5)	H	X	X	X	X	V	L	L	L	L	H
No – Operation	Any	H	X	X	X	X	X	L	H	H	H	X
Burst Stop	Active(4)	H	X	X	X	X	X	L	H	H	L	L
Device Deselect	Any	H	X	X	X	X	X	H	X	X	X	X
Auto – Refresh	Idle	H	H	X	X	X	X	L	L	L	H	L
Self - Refresh Entry	Idle	H	L	X	X	X	X	L	L	L	H	X
Self Refresh Exit	Idle (Self Refresh)	L	H	X	X	X	X	H	X	X	X	X
								L	H	H	H	X
Clock suspend Mode Entry	Active	H	L	X	X	X	X	X	X	X	X	X
Power Down Mode Entry	Any(6)	H	L	X	X	X	X	X	X	X	X	X
Clock Suspend Mode Exit	Active	L	H	X	X	X	X	X	X	X	X	X
Power Down Mode Exit	Any (power-down)	L	H	X	X	X	X	H	X	X	X	X
								L	H	H	H	X
Data write/Output Enable	Active	H	X	L	X	X	X	X	X	X	X	X
Data Write/Output Disable	Active	H	X	H	X	X	X	X	X	X	X	X

Notes: (1) V= Valid X = Don't care L= Low Level H= High Level
(2) CKEn signal is the input level when the command is issued
CKEn-1 signal is the input level one clock cycle before the command is issued
(3) The bank state is designated by the BS signal
(4) Device state sre 1, 2, 4, 8 and Full Page Burst operation.
(5) The Special Mode Register Set operation is also available in Row Active state
(6) Power-down mode cannot be initiated during a Burst cycle.
When this command asserts during a Burst cycle, the device enters Clock Suspend mode.
(7) DQM0 to DQM3

Functional Description

Power Up and Initialization

The default power up state of the mode register is unspecified. The following power up and initialization sequence need to be followed to guarantee the device being preconditioned to each user specific needs.

During power up, all V_{CC} and $V_{CC}Q$ pins must be ramp up simultaneously to the specified voltage when the input signals are held in the "NOP" state. The power up voltage must not exceed V_{CC}+0.3V on any of the input pins or V_{CC} supplies. After power up, an initial pause of 200us is required followed by a precharge of all banks using the precharge command. To prevent data contention on the DQ bus during power up, it is required that the DQM and CKE pins be held high during the initial pause period. Once all banks have been precharged, the Mode Register Set Command must be issued to initialize the Mode Register. An additional eight Auto Refresh cycles (CBR) are also required before or after programming the Mode Register to ensure proper subsequent operation.

Programming Mode Register

After initial power up, the Mode Register Set Command must be issued for proper device operation. All banks must be in a precharged state and CKE must be high at least one cycle before the Mode Register Set Command can be issued. The Mode Register Set Command is activated by the low signals of RAS, CAS, CS, WE and DSF at the clock rising edge. The address inputs data during this cycle defines the parameters to be set as shown in the Mode Register Operation table. A new command may be issued following the mode register set command once a delay equal to t_{RSC} has elapsed. Please refer to the Mode Register Set Cycle and Operation Table.

Bank Activate Command

The Bank Activate command must be applied before any Read or Write operation can be executed. The operation is similar to RAS# activate in EDO DRAM. The delay from the Bank Activate command is applied to the first read or write operation can begin must not be less than the RAS to CAS delay time (t_{RCD}). Once a bank has been activated it must be precharged before another Bank Activate command can be issued to the same bank. The minimum time interval between successive Bank Activate commands to the same bank is determined by the RAS cycle time of the device (t_{RC}). The minimum time interval between interleaved Bank Activate commands (Bank A to Bank B and vice versa) is the Bank to Bank delay time (t_{RRD}). The maximum time that a bank can be held active is specified as t_{RAS}(max).

Read and Write Access Modes

After a bank has been activated, a read or write cycle can follow. This is accomplished by setting RAS high and CAS low at the clock rising edge after minimum of t_{RCD} delay. WE pin voltage level defines whether the access cycle is a read operation (WE high), or a write operation (WE low). The address inputs determine the starting column address.

Reading or writing to a different row within an activated bank requires the bank be precharged and a new Bank Activate command be issued. When more than one bank is activated, interleaved bank Read or Write operations are possible. By using the programmed burst length and alternating the access and precharge operations between multiple banks, seamless data access operation among many different pages can be realized. Read or Write Commands can also be issued to the same bank or between active banks on every clock cycle.

Burst Read Command

The Burst Read command is initiated by applying logic low level to CS and CAS while holding RAS and WE high at the rising edge of the clock. The address inputs determine the starting column address for the burst. The Mode Register sets type of burst (sequential or interleave) and the burst length (1, 2, 4, 8, full page) during the Mode Register Set cycle. Table 2 and 3 on the next page explain the address sequence of interleave mode and sequential mode.

Burst Write Command

The Burst Write command is initiated by applying logic low level to CS, CAS and WE while holding RAS high at the rising edge of the clock. The address inputs determine the starting column address. Data for the first burst write cycle must be applied on the DQ pins on the same clock cycle that the Write Command is issued. The remaining data inputs must be supplied on each subsequent rising clock edge until the burst length is completed. Data supplied to the DQ pins after burst finishes will be ignored.

Read Interrupted by a Read

Another Read Command may interrupt a Burst Read. When the previous burst is interrupted, the remaining addresses are overridden by the new read address with the full burst length. The data from the first Read Command continues to appear on the outputs until the CAS latency from the interrupting Read Command is satisfied.

Read Interrupted by a Write

To interrupt a burst read with a Write Command, DQM may be needed to place the DQs (output drivers) in a high impedance state to avoid data contention on the DQ bus. If a Read Command will issue data on the first and second clocks cycles of the write operation, DQM is needed to insure the DQs are tri-stated. After that point the Write Command will have control of the DQ bus and DQM masking is no longer needed.

Write Interrupted by a Write

A burst write may be interrupted before completion of the burst by another Write Command. When the previous burst is interrupted, the remaining addresses are overridden by the new address and data will be written into the device until the programmed burst length is satisfied.

Write Interrupted by a Read

A Read Command will interrupt a burst write operation on the same clock cycle that the Read Command is activated. The DQs must be in the high impedance state at least one cycle before the new read data appears on the outputs to avoid data contention. When the Read Command is activated, any residual data from the burst write cycle will be ignored.

Burst Stop Command

A Burst Stop Command may be used to terminate the existing burst operation but leave the bank open for future Read or Write Commands to the same page of the active bank, if the burst length is full page. Use of the Burst Stop Command during other burst length operations is illegal. The Burst Stop Command is defined by having RAS and CAS high with CS and WE low at the rising edge of the clock. The data DQs go to a high impedance state after a delay which is equal to the CAS Latency in a burst read cycle, interrupted by Burst Stop. If a Burst Stop Command is issued during a full page burst write operation, then any residual data from the burst write cycle will be ignored.

Table 2 Address Sequence of Sequential Mode

DATA	Access Address	Burst Length
Data 0	n	BL= 2 (disturb address is A0)
Data 1	n + 1	No address carry from A0 to A1
Data 2	n + 2	BL= 4 (disturb addresses are A0 and A1)
Data 3	n + 3	No address carry from A1 to A2
Data 4	n + 4	
Data 5	n + 5	BL= 8 (disturb addresses are A0, A1 and A2)
Data 6	n + 6	No address carry from A2 to A3
Data 7	n + 7	

- Addressing Sequence of Sequential Mode

  A column access is performed by increasing the address from the column address which is input to the device. The disturb address is varied by the Burst Length as shown in Table 2.

- Addressing Sequence of Interleave Mode

  A column access is started in the input column address and is performed by inverting the address bit in the sequence shown in Table 3.

Table 3 Address Sequence of Interleave Mode

DATA	Access Address	Burst Length
Data 0	A8 A7 A6 A5 A4 A3 A2 A1 A0	BL = 2
Data 1	A8 A7 A6 A5 A4 A3 A2 A1 $\overline{A0}$	
Data 2	A8 A7 A6 A5 A4 A3 A2 $\overline{A1}$ A0	BL = 4
Data 3	A8 A7 A6 A5 A4 A3 A2 $\overline{A1}$ $\overline{A0}$	
Data 4	A8 A7 A6 A5 A4 A3 $\overline{A2}$ A1 A0	
Data 5	A8 A7 A6 A5 A4 A3 $\overline{A2}$ A1 $\overline{A0}$	BL = 8
Data 6	A8 A7 A6 A5 A4 A3 $\overline{A2}$ $\overline{A1}$ A0	
Data 7	A8 A7 A6 A5 A4 A3 $\overline{A2}$ $\overline{A1}$ $\overline{A0}$	

Auto-Precharge Command

If A8 is set to high when the Read or Write Command is issued, then the auto-precharge function is entered. During autoprecharge, a Read Command will execute as normal with the exception that the active bank will begin to precharge automatically before all burst read cycles have been completed. Regardless of burst length, it will begin a certain number of clocks prior to the end of the scheduled burst cycle. The number of clocks is determined by CAS latency.

A Read or Write Command with auto-precharge can not be interrupted before the entire burst operation is completed. Therefore, use of a Read, Write, or Precharge Command is prohibited during a read or write cycle with auto-precharge. Once the precharge operation has started, the bank cannot be reactivated until the Precharge time (t_{RP}) has been satisfied. Issue of Auto-Precharge command is illegal if the burst is set to full page length. If A8 is high when a Write Command is issued, the Write with Auto-Precharge function is initiated. The SGRAM automatically enters the precharge operation one clock delay from the last burst write cycle. This delay is referred to as Write tDPL. The bank undergoing auto-precharge can not be reactivated until tDPL and t_{RP} are satisfied. This is referred to as t_{DAL}, Data-in to Active delay (t_{DAL} = t_{DPL} + t_{RP}). When using the Auto-precharge Command, the interval between the Bank Activate Command and the beginning of the internal precharge operation must satisfy t_{RAS}(min).

Precharge Command

The Precharge Command is used to precharge or close a bank that has been activated. The Precharge Command is entered when CS, RAS and WE are low and CAS is high at the rising edge of the clock. The Precharge Command can be used to precharge each bank separately or all banks simultaneously. Two address bits, A10, and A8, are used to define which bank(s) is to be precharged when the command is issued. After the Precharge Command is issued, the precharged bank must be reactivated before a new read or write access can be executed. The delay between the Precharge Command and the Activate Command must be greater than or equal to the Precharge time (t_{RP}).

Self Refresh Command

The Self Refresh Command is defined by having CS, RAS, CAS and CKE held low with WE high at the rising edge of the clock. All banks must be idle prior to issuing the Self Refresh Command. Once the command is registered, CKE must be held low to keep the device in Self Refresh mode. When the SGRAM has entered Self Refresh mode all of the external control signals, except CKE, are disabled. The clock is internally disabled during Self Refresh Operation to save power. The device will exit Self Refresh operation after CKE is returned high. A minimum delay time is required when the device exits Self Refresh Operation and before the next command can be issued. This delay is equal to the RAS cycle time plus the Self Refresh exit time.

Power Down Mode

The Power Down mode is initiated by holding CKE low. All of the receiver circuits except CKE are gated off to reduce the power. The Power Down mode does not perform any refresh operations, therefore the device can not remain in Power Down mode longer than the Refresh period (t_{REF}) of the device.

The Power Down mode is exited by bringing CKE high. When CKE goes high, a No Operation Command is required on the next rising clock edge, depending on t_{CK}. The input buffers need to be enabled with CKE held high for a period equal to t_{CES}(min) + t_{CK}(min).

No Operation Command

The No Operation Command should be used in cases when the SGRAM is in a idle or a wait state to prevent the SGRAM from registering any unwanted commands between operations. A No Operation Command is registered when CS is low with RAS, CAS, and WE held high at the rising edge of the clock. A No Operation Command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

Deselect Command

The Deselect Command performs the same function as a No Operation Command. Deselect Command occurs when CS is brought high, the RAS, CAS, and WE signals become don't cares.

Clock Suspend Mode

During normal access mode, CKE must be held high enabling the clock. When CKE is registered low while at least one of the banks is active, Clock Suspend Mode is entered. The Clock Suspend mode deactivates the internal clock and suspends any clocked operation that was currently being executed. There is a one clock delay between the registration of CKE low and the time at which the SGRAM operation suspends. While in Clock Suspend mode, the SGRAM ignores any new commands that are issued. The Clock Suspend mode is exited by bringing CKE high. There is a one clock cycle delay from when CKE returns high to when Clock Suspend mode is exited.

DEFINE SPECIAL FUNCTION (DSF)

The DSF controls the graphic applications of SGRAM. If DSF is tied to low, SGRAM functions as 256K x 32 x2 Bank SDRAM. SGRAM can be used as an unified memory by the appropriate DSF command. All the graphic function mode can be entered only by setting DSF high when issuing commands which otherwise would be normal SDRAM commands. SDRAM functions such as RAS Active, Write, and WCBR change to SGRAM functions such as RAS Active with WPB, Block Write and SWCBR respectively. See sessions below for the graphic functions that DSF control.

SPECIAL MODE REGISTER SET (SMRS)

There are two kinds of special mode registers in SGRAM.One is color register and the other is mask register. Those usages will be explained at "WRITE PER BIT" and "BLOCK WRITE" session. When A5 and DSF goes high in the same cycle as CS, RAS, CAS and WE going low, load mask register (LMR) process is executed and the mask registers are filled with the masks for associated DQ’s through DQ pins. And when A 6 and DSF goes high in the same cycle as CS, RAS, CAS and WE going low, load color register(LCR) process is executed and the color register is filled with color data for associated DQ’s through the DQ pins. The next clock of LMR or LCR, a new command can be issued. Special Mode Rregister Set, compared with Mode Rregister Set, can be issued at the active state under the condition that DQ’s are idle. As in write operation, Special Mode Rregister Set accepts the data needed through DQ pins. Therefore it should be attended not to induce bus contention. The more detailed materials can be obtained by referring corresponding timing diagram.

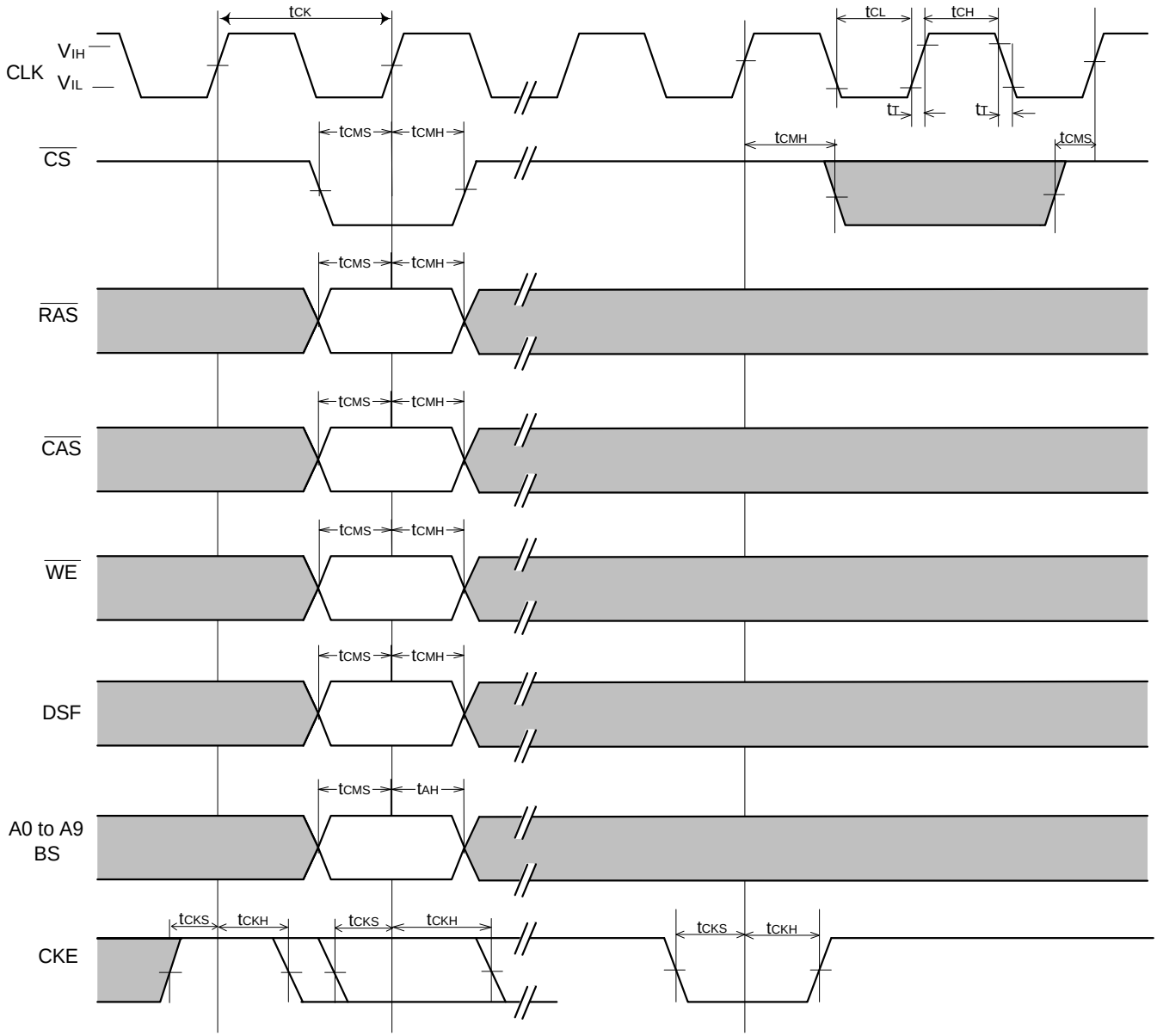
WRITE PER BIT

Write Per Bit (i.e. I/O mask mode) for SGRAM is a function that selectively masks bits of data being written to the devices. The mask is stored in an internal register and applied to each bit of data written when enabled. Bank active command with DSF=High enabled write per bit for associated bank. Bank active command with DSF=Low disables write per bit for the associ-ated bank. The mask used for write per bit operations is stored in the mask register accessed by SWCBR (Special Mode Register Set Command). When a mask bit=1, the associated data bit is written when a write command is executed and write per bit has been enabled for the bank being written. When a mask bit=0, the associated data bit is unaltered when a write command is executed and the write per bit has been enabled for the bank being written. No additional timing conditions are required for write per bit operations. Write per bit writes can be either single write, burst writes or block writes. DQM masking is the same for write per bit and non Write Per Bit write.

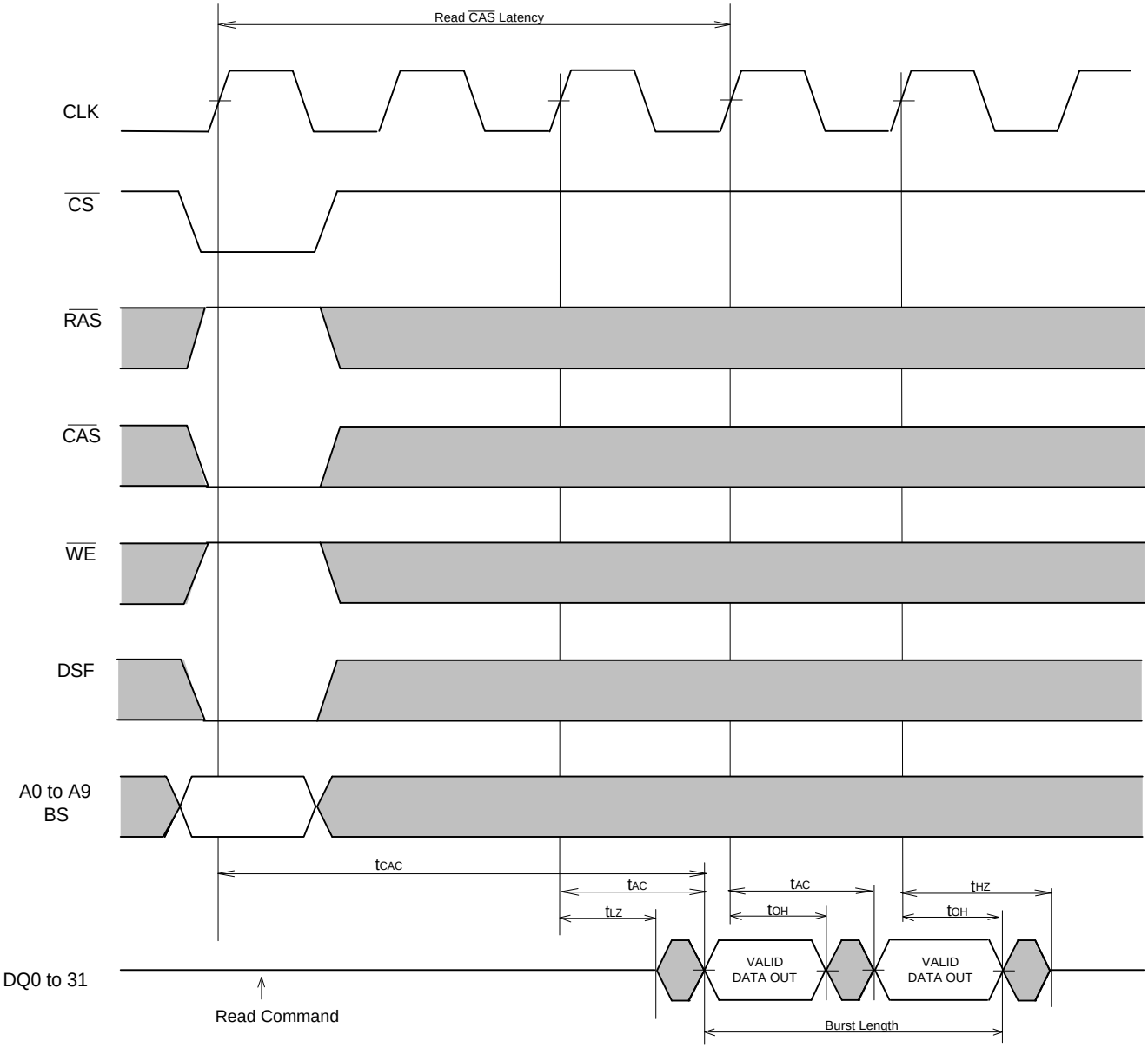
BLOCK WRITE

Block write is a feature allowing the simultaneous writing of consecutive 8 columns of data within a RAM device during a sin-gle access cycle. During block write the data to be written comes from an internal "color" register and DQ I/O pins are used for independent column selection. The block of column to be written is aligned on 8 column boundaries and is defined by the column address with the 3 LSB's ignored. Write command with DSF=1 enables block write for the associated bank. A write command with DSF=0 enables normal write for the associated bank. The block width is 8 column where column="n" bits for by "n" part. The color register is the same width as the data port of the chip.It is written via a SWCBR where data present on the DQ pin is to be coupled into the internal color register. The color register provides the data masked by the DQ column select, WPB mask(If enabled), and DQM byte mask. Column data masking(Pixel masking) is provided on an individual column basis for each byte of data. The column mask is driven on the DQ pins during a block write command. The DQ column mask function is segmented on a per bit basis(i.e. DQ[0:7] provides the column mask for data bits[0:7], DQ[8:15] provides the column mask for data bits[8:15], DQ0 masks column[0] for data bits[0:7], DQ9 masks column [1] for data bits [8:15], etc). Block writes are always non-burst, independent of the burst length that has been programmed into the mode register. Back to back block writes are allowed provided that the specified block write cycle time(t_{BWC}) is satisfied. If write per bit was enabled by the bank active command with DSF=1, then write per bit masking of the color register data is enabled. If write per bit was disabled by a bank active command with DSF=0, the write per bit masking of the color register data is disabled. DQM masking provides independent data byte masking during block writes exactly the same as it does during normal write operations, except that the control is extended to the consecutive 8 columns of the block write.

Command Input Timing

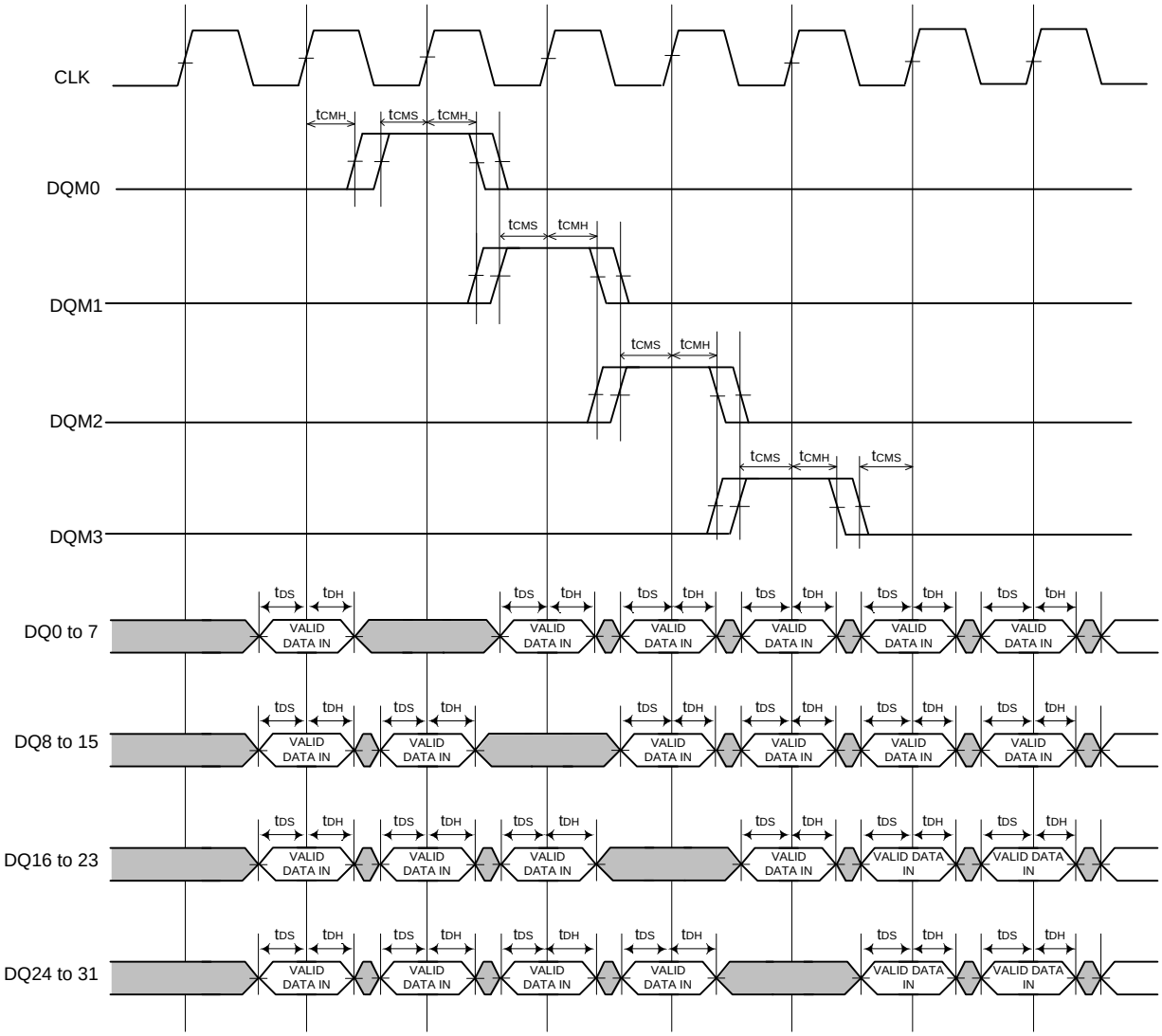


Read Timing

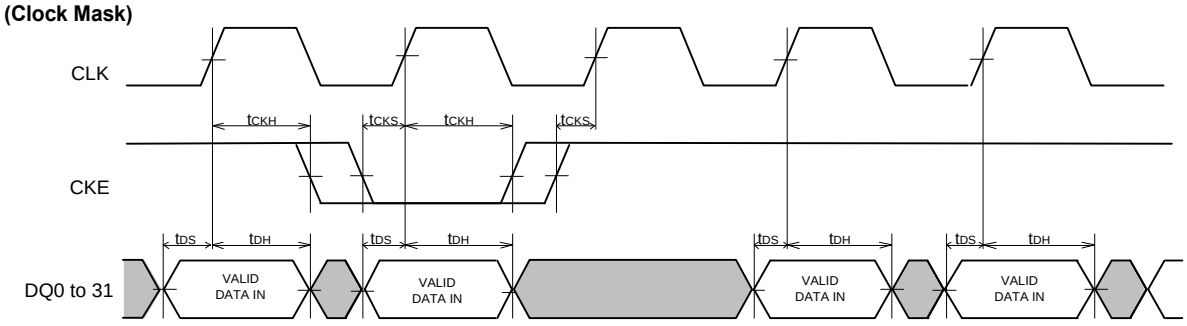

Read CAS Latency
CLK
CS
RAS
CAS
WE
DSF
A0 to A9
BS
tCAC
tAC
tLZ
tAC
tOH
tHZ
tOH
DQ0 to 31
VALID DATA OUT
VALID DATA OUT
Read Command
Burst Length

Control Timing of Input Data

(Word Mask)

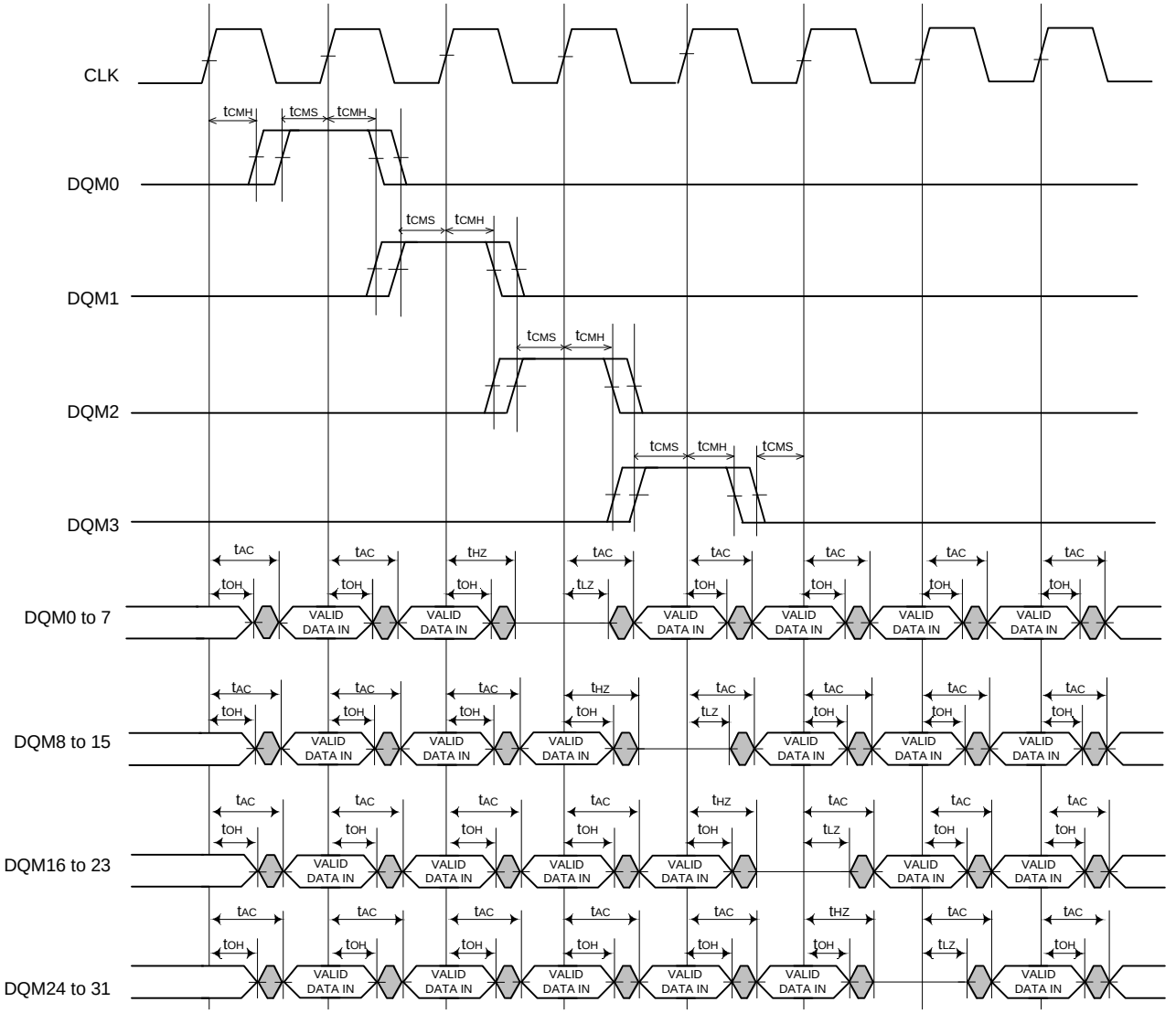


(Clock Mask)

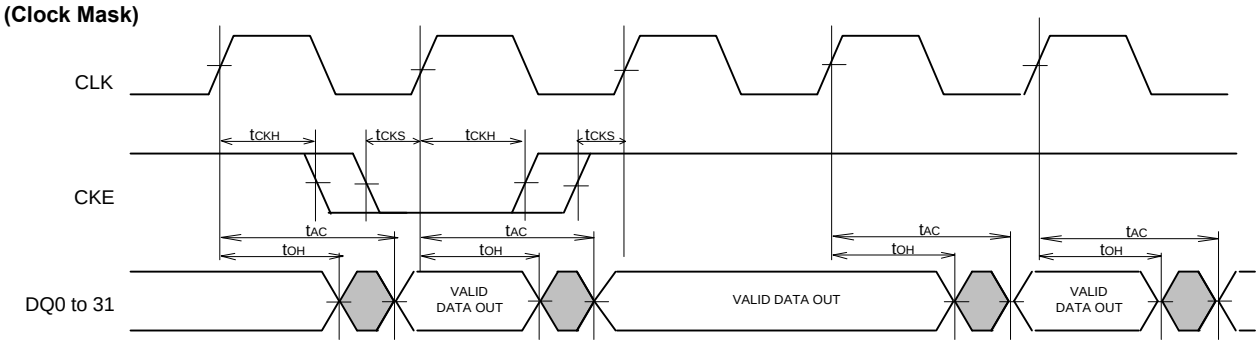


Control Timing of Output Data

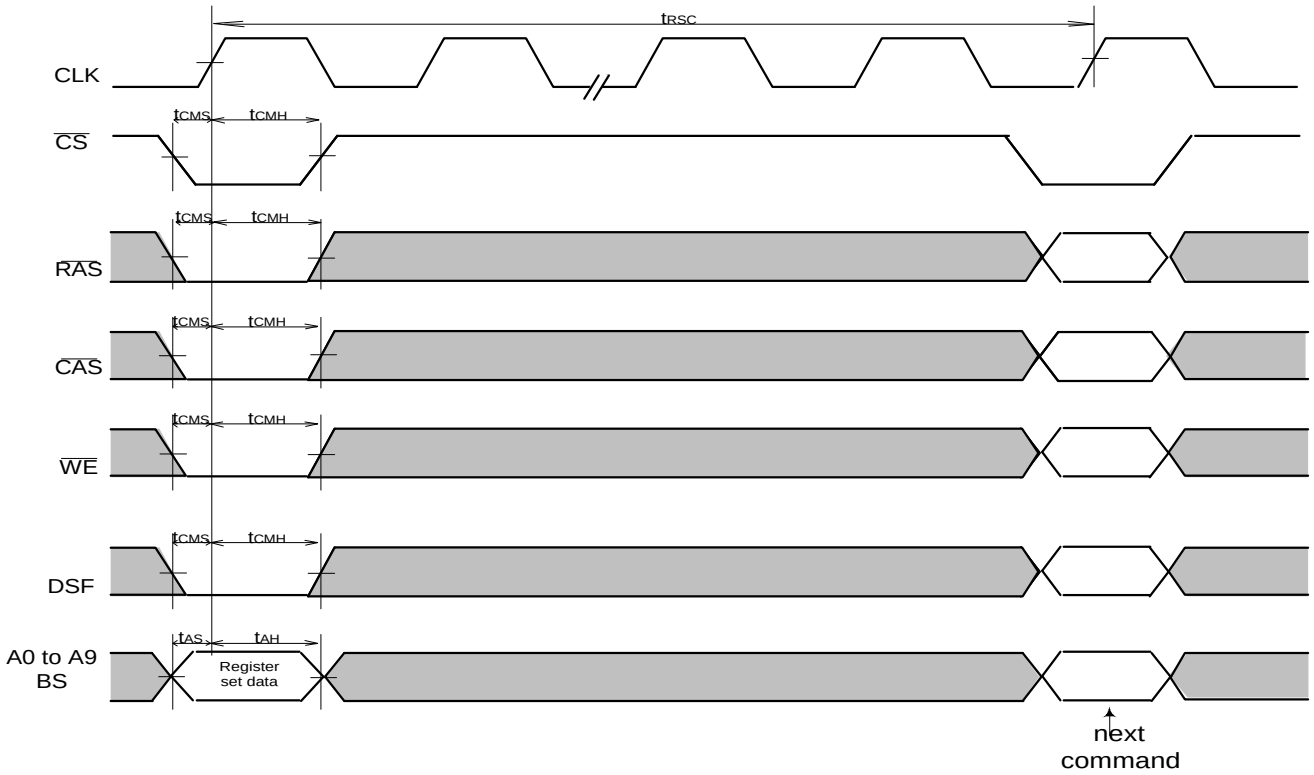
(Output Enable)



(Clock Mask)



Mode Register Set Cycle



A0	Burst Length	
A1		
A2		
A3	Burst Type	
A4	$\overline{CAS}$ Latency	
A5		
A6		
A7	"0"	(Test Mode)
A8	Write Mode	
A9	"0"	Reserved
BS	"X"	Reserved

NOTE: 0=Low level
1=High level
X=Don't care

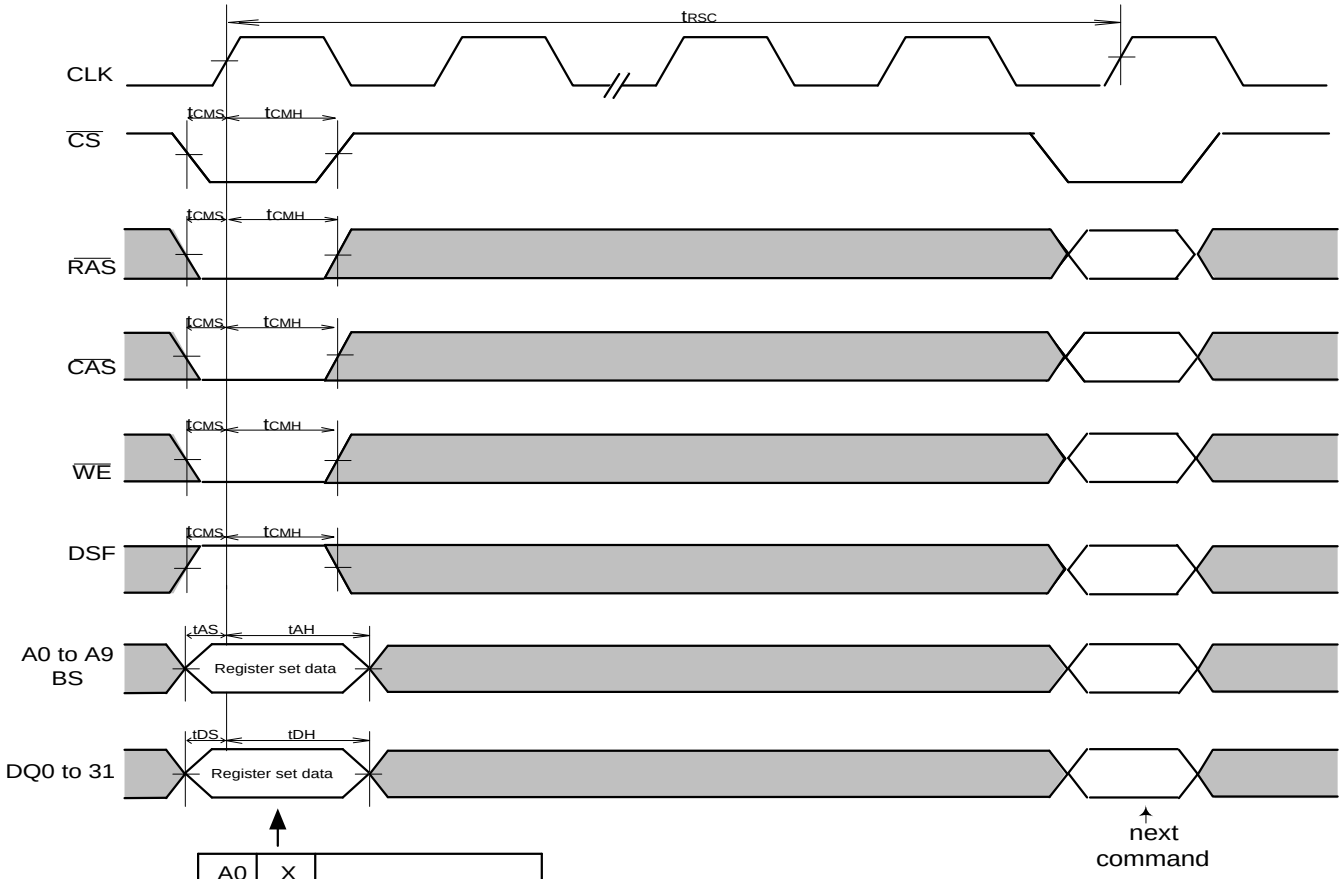
			Burst Length	
A2	A1	A0	Sequential	Interleaved
0	0	0	1	Reserved
0	0	1	2	Reserved
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1		
1	1	0		
1	1	1	Full Page	

A3	Burst Type
0	Sequential
1	Interleave

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	-
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	
1	1	0	
1	1	1	

A8	Single Write Mode
0	Burst read and Burst write
1	Burst read and single write

Special Mode Register Set Cycle



A0	X	Reserved
A1	X	
A2	X	
A3	X	
A4	X	
A5	Load Mask (LM)	
A6	Load Color (LC)	
A7	X	Reserved
A8	X	
A9	X	
BS	X	

A5	Load Mask Register Set Mode
0	Unchanged
1	Load

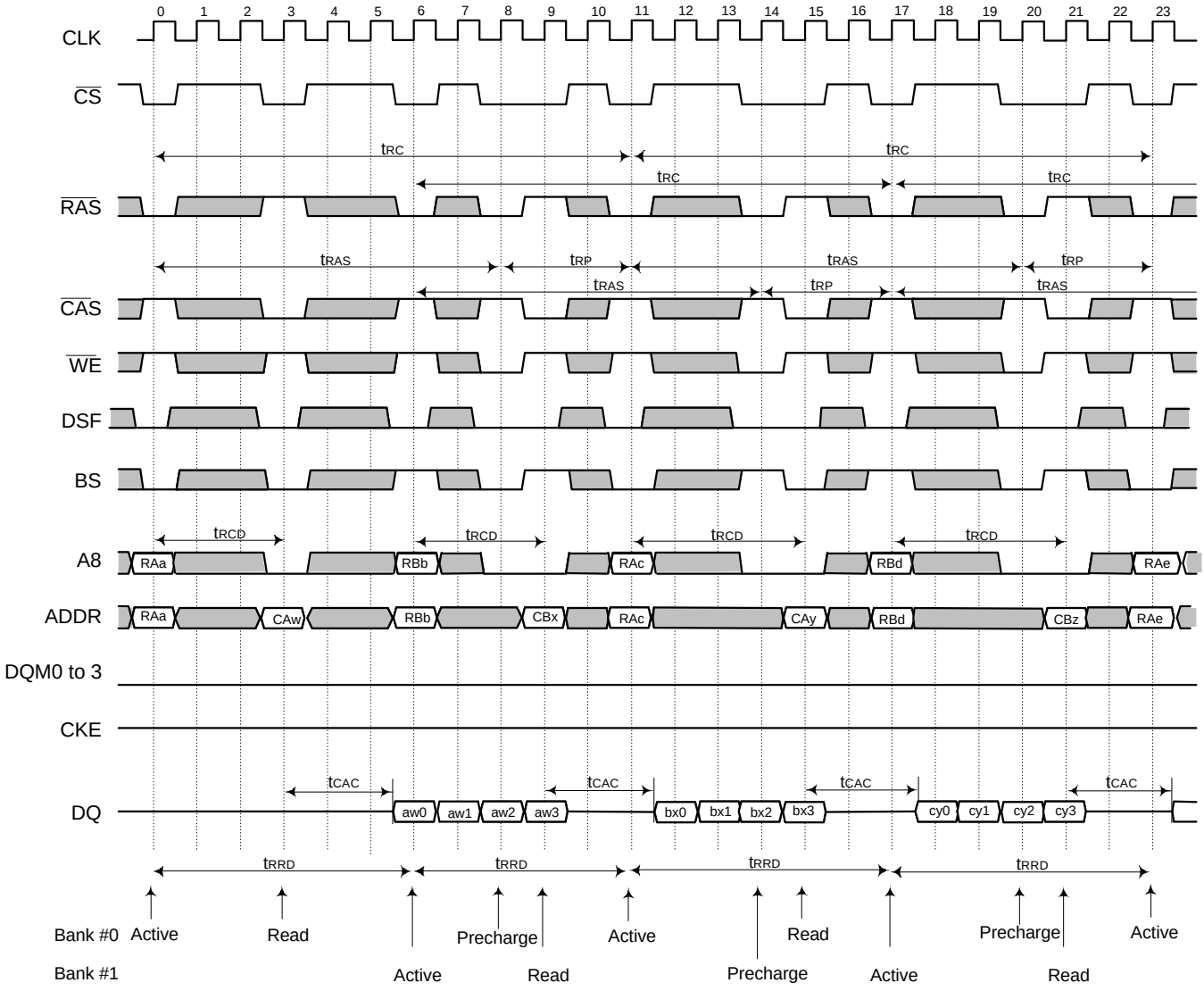
A6	Load Color Register Set Mode
0	Unchanged
1	Load

DQi	Load Mask	Load Color
0	Enable	Write 0
1	Disable	Write 1

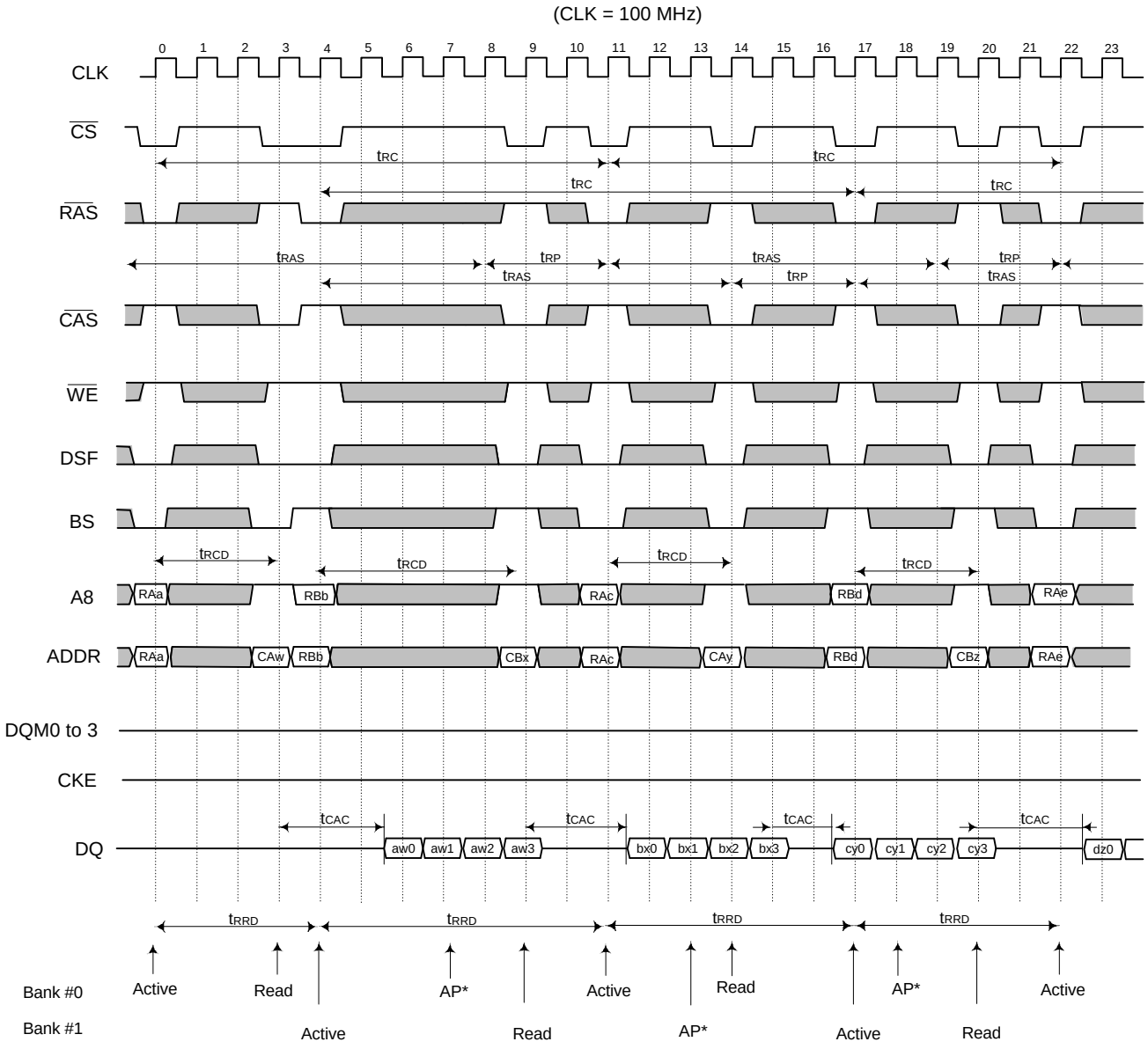
NOTE: A5 and A6 cannot both be set to 1 at the same time

Interleaved Bank Read (Burst Length = 4, $\overline{CAS}$ Latency = 3)

(CLK = 100 MHz)

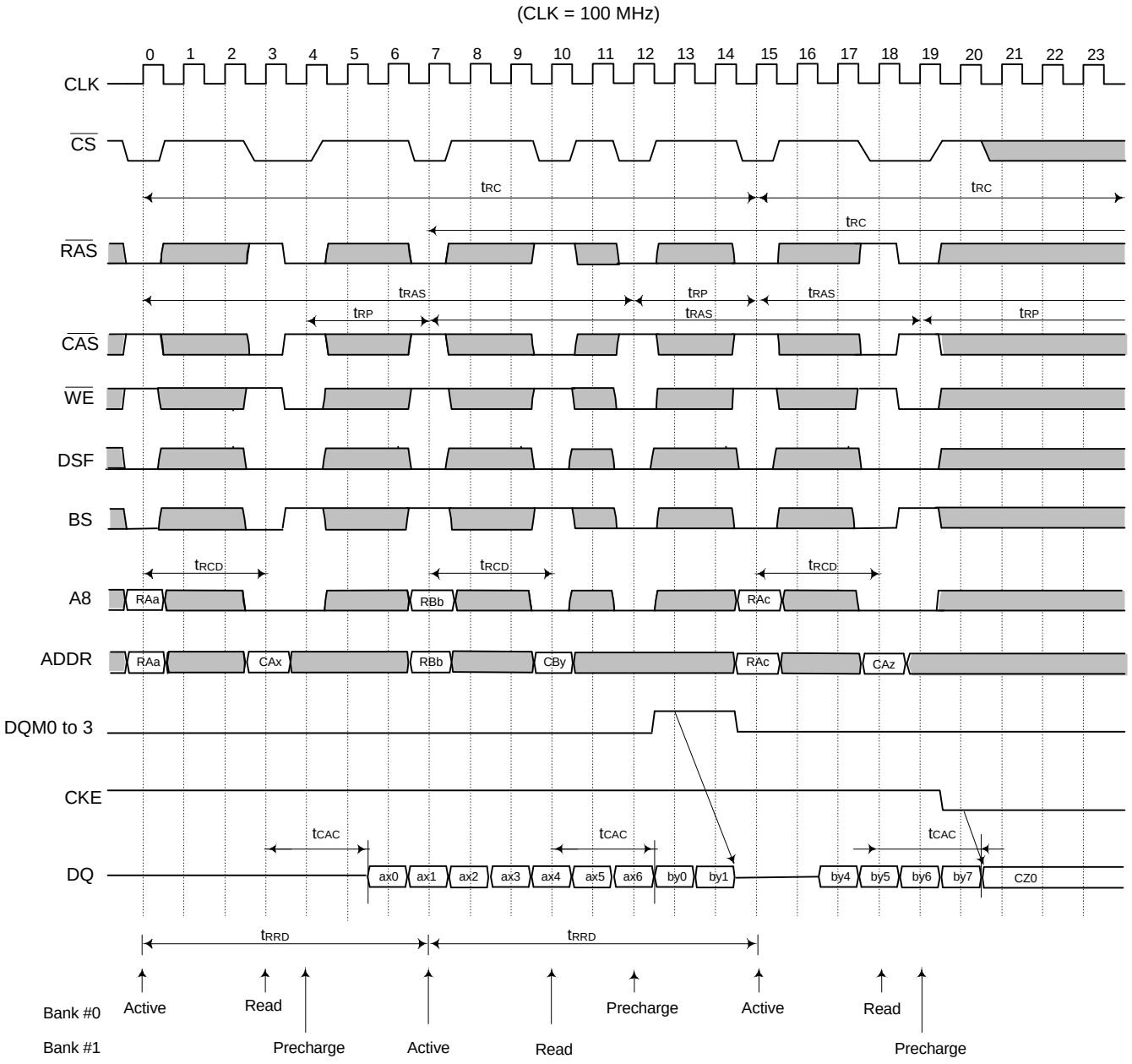


Interleaved Bank Read (Burst Length = 4, CAS Latency = 3, Autoprecharge)



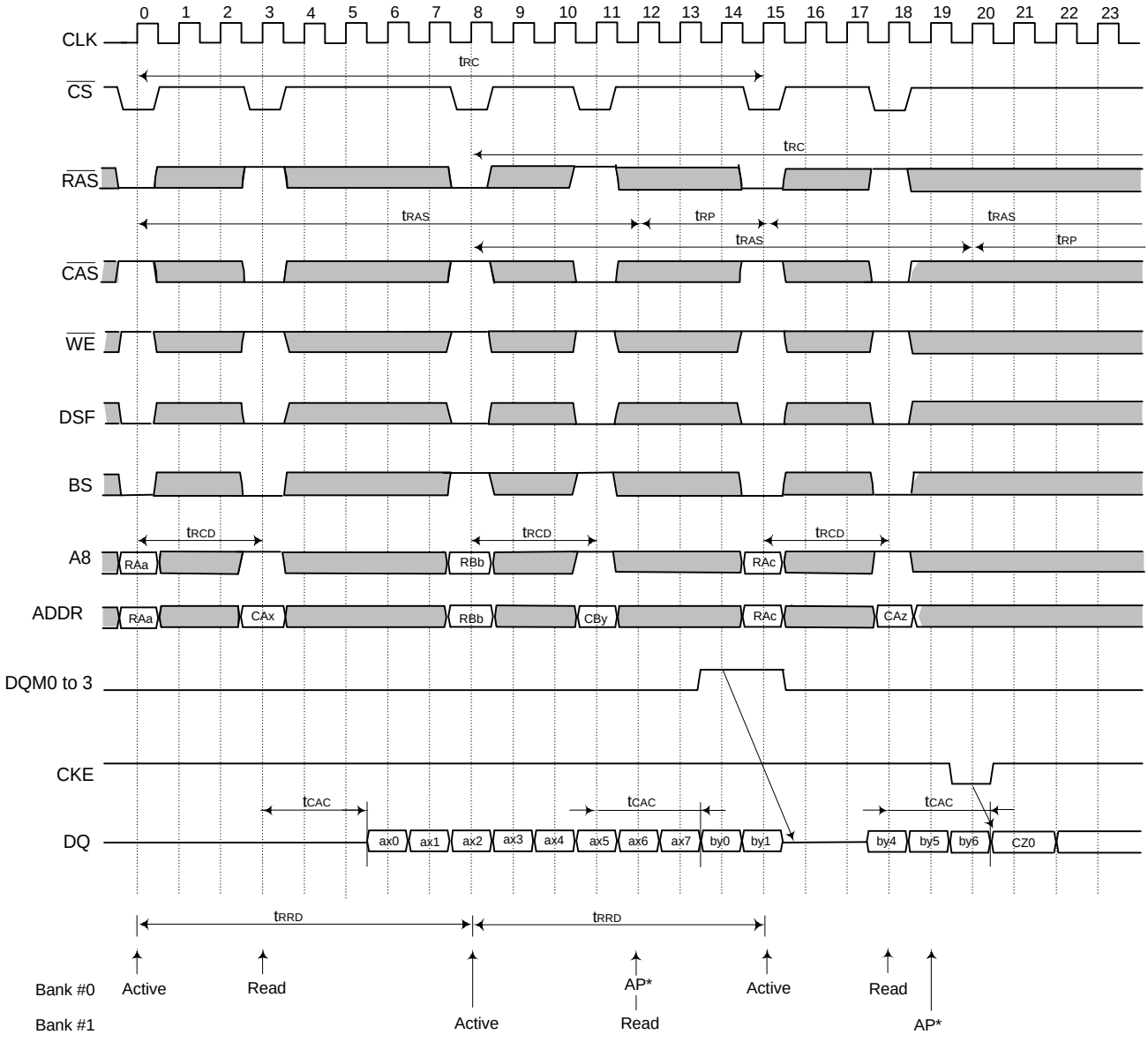
* AP is the internal precharge start timing

Interleaved Bank Read (Burst Length=8, $\overline{CAS}$ Latency=3)



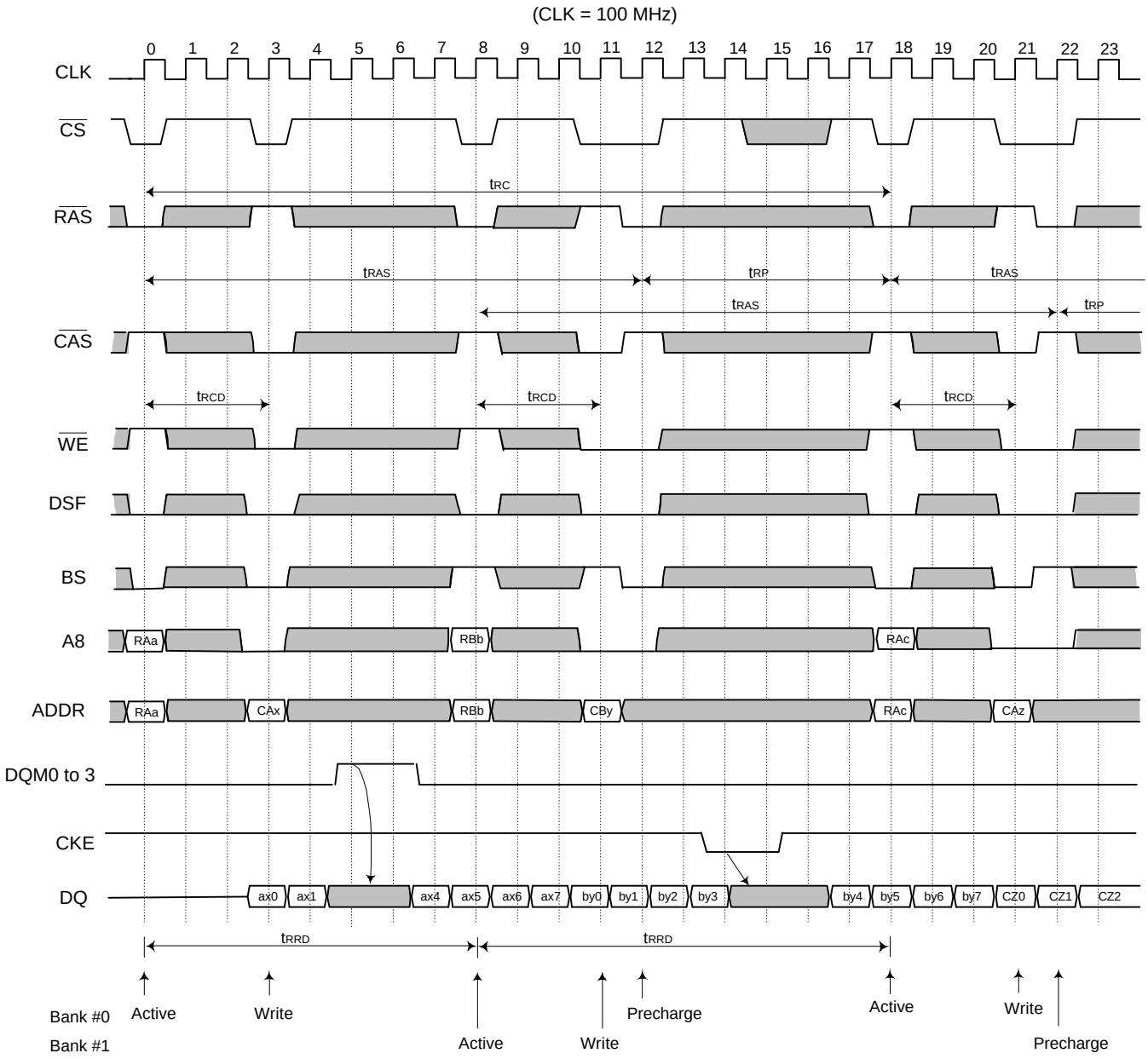
Interleaved Bank Read (Burst Length=8, $\overline{CAS}$ Latency=3, Autoprecharge)

(CLK = 100 MHz)

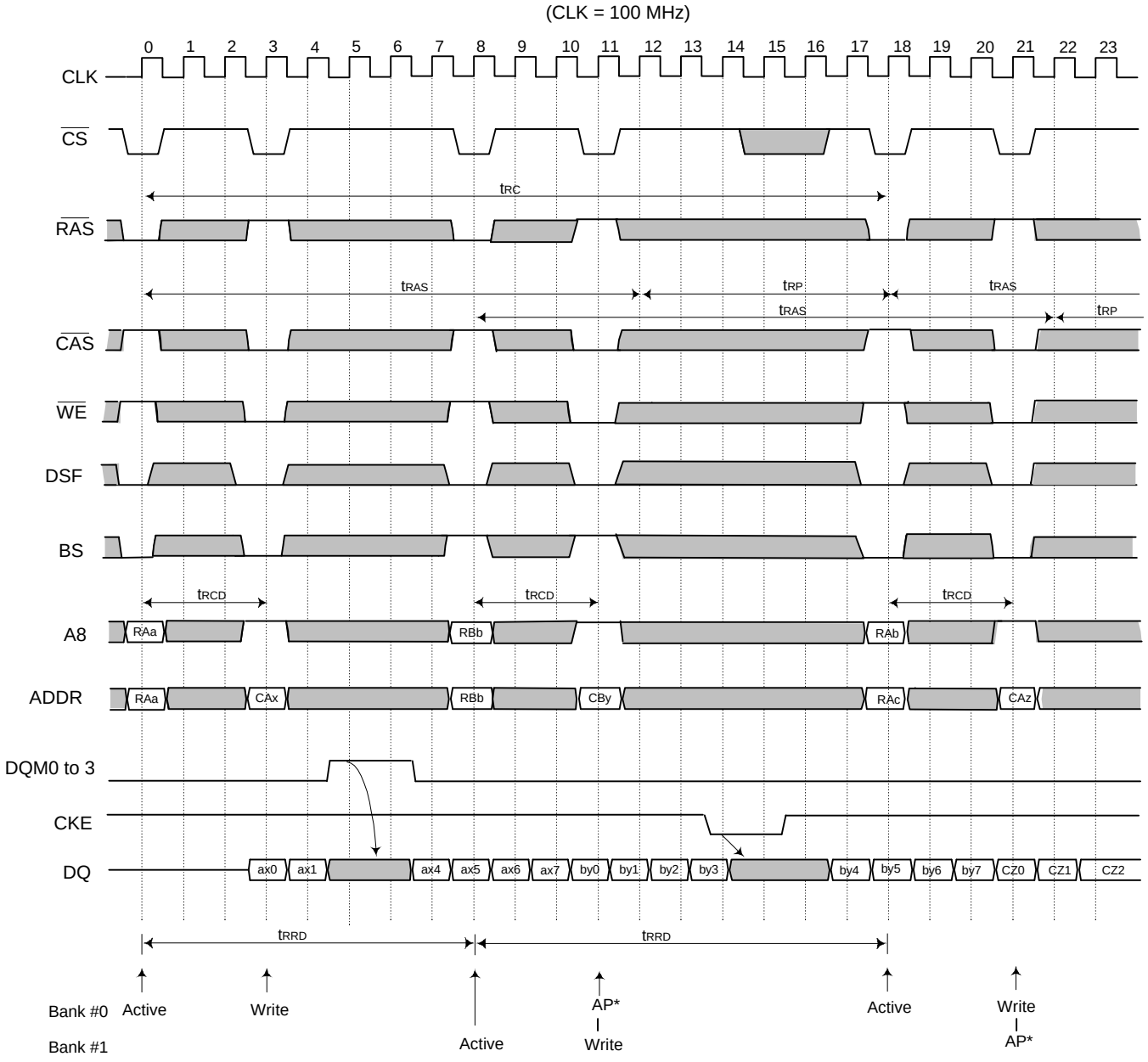


* AP is the internal precharge start timing

Interleaved Bank Write (Burst Length=8)



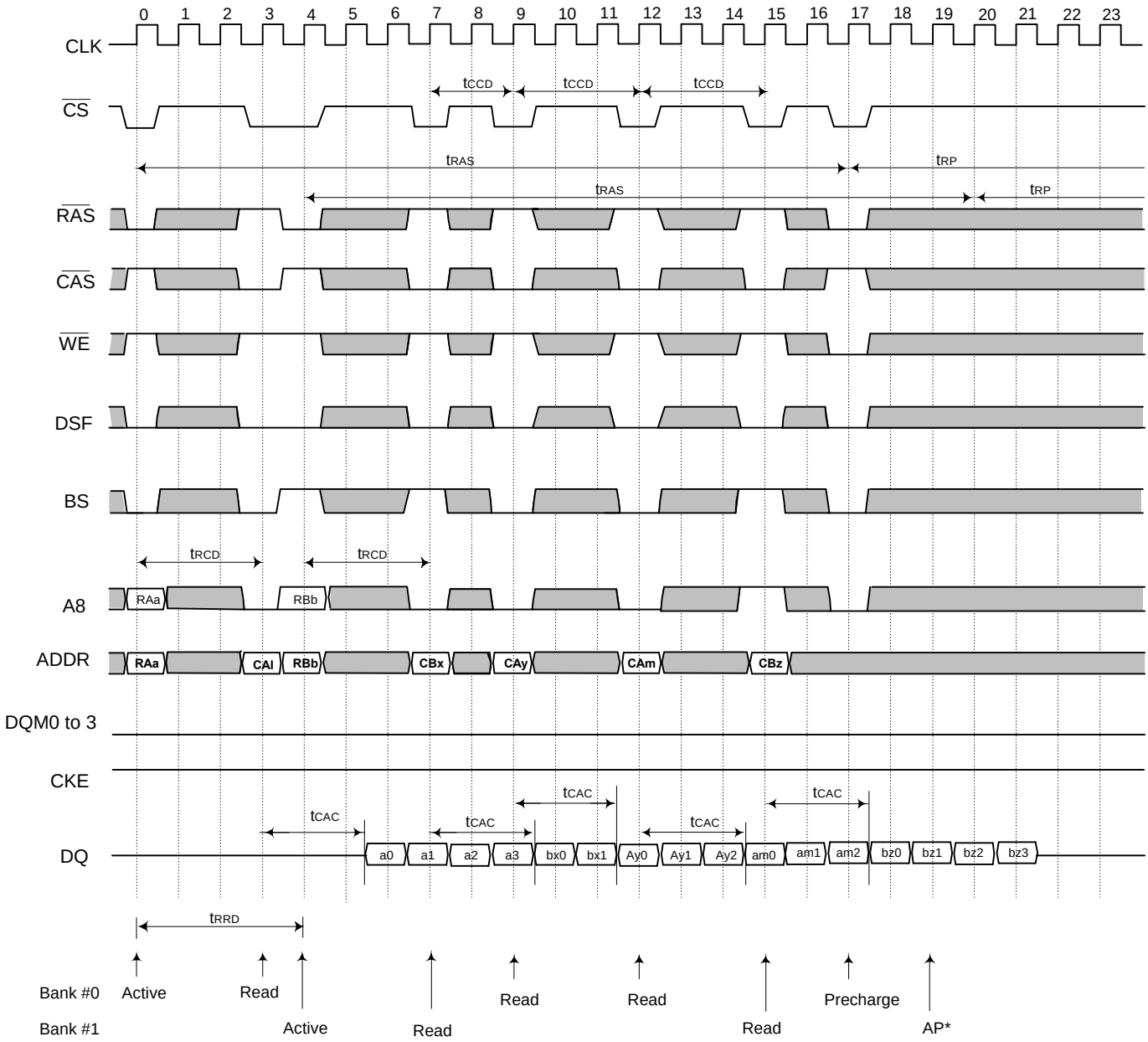
Interleaved Bank Write (Burst Length=8, Auto Precharge)



* AP is the internal precharge start timing

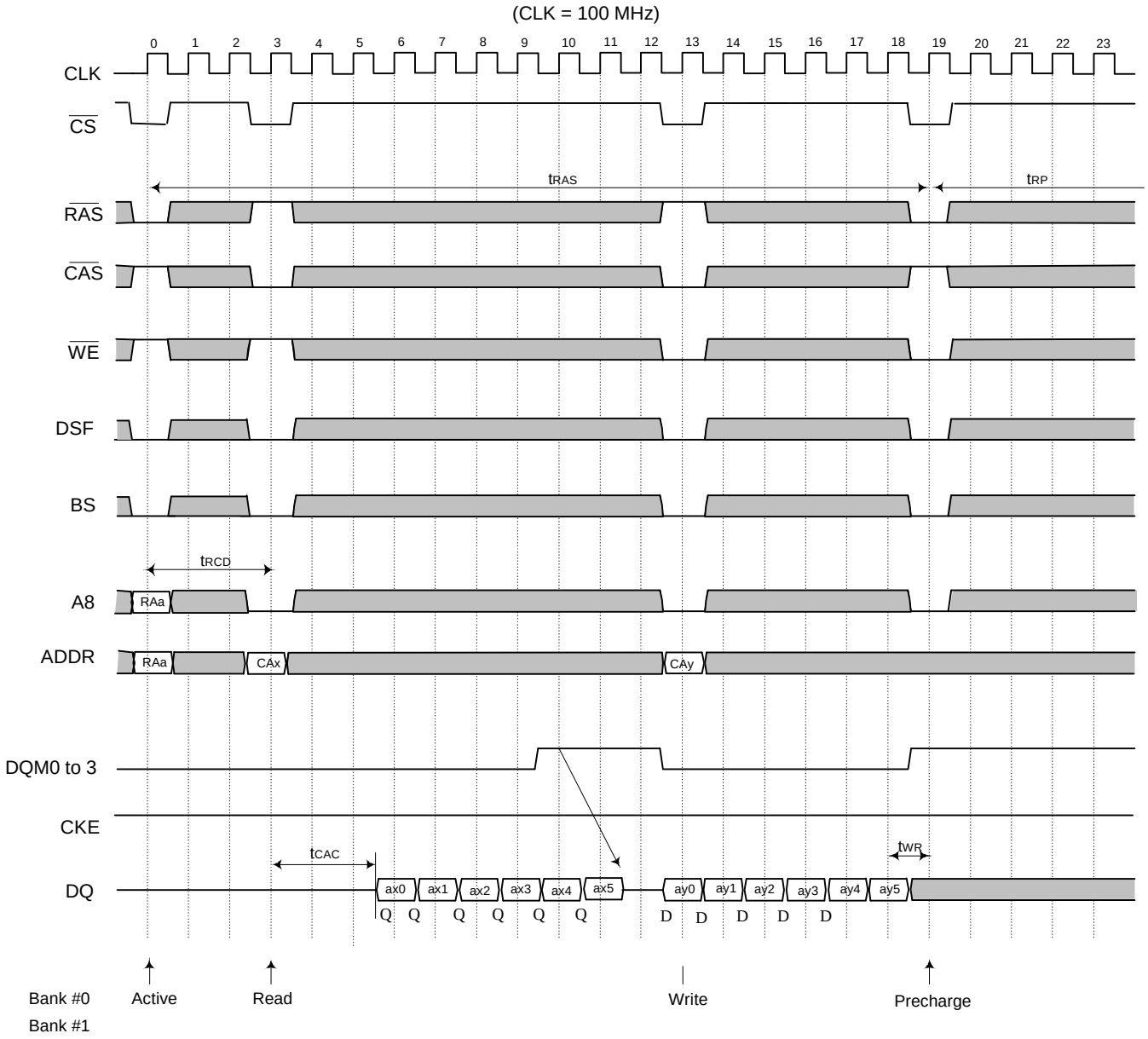
Page Mode Read (Burst Length=4, $\overline{CAS}$ Latency=3)

(CLK = 100 MHz)

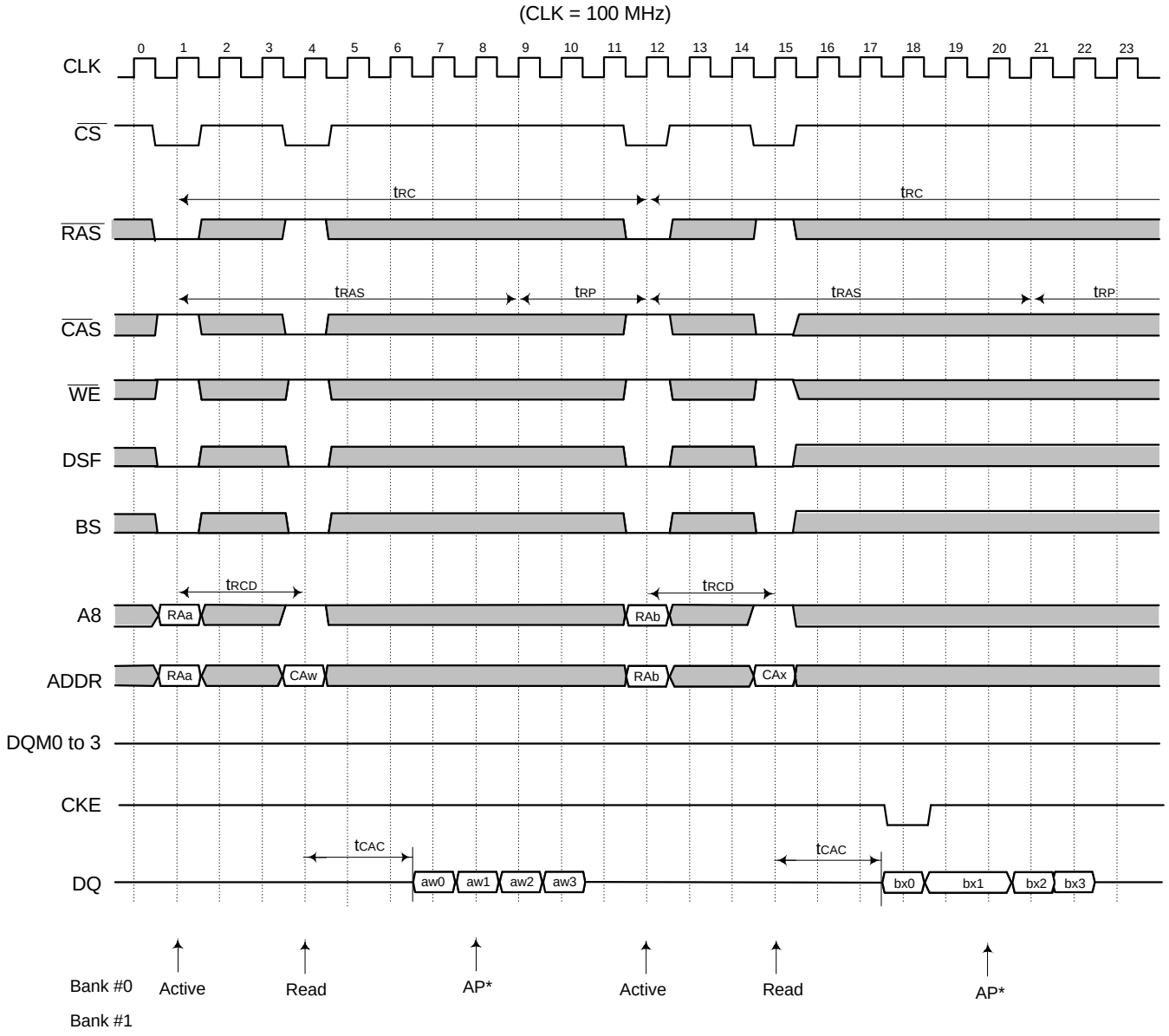


* AP is the internal precharge start timing

Page Mode Read / Write (Burst Length=8, $\overline{CAS}$ Latency=3)



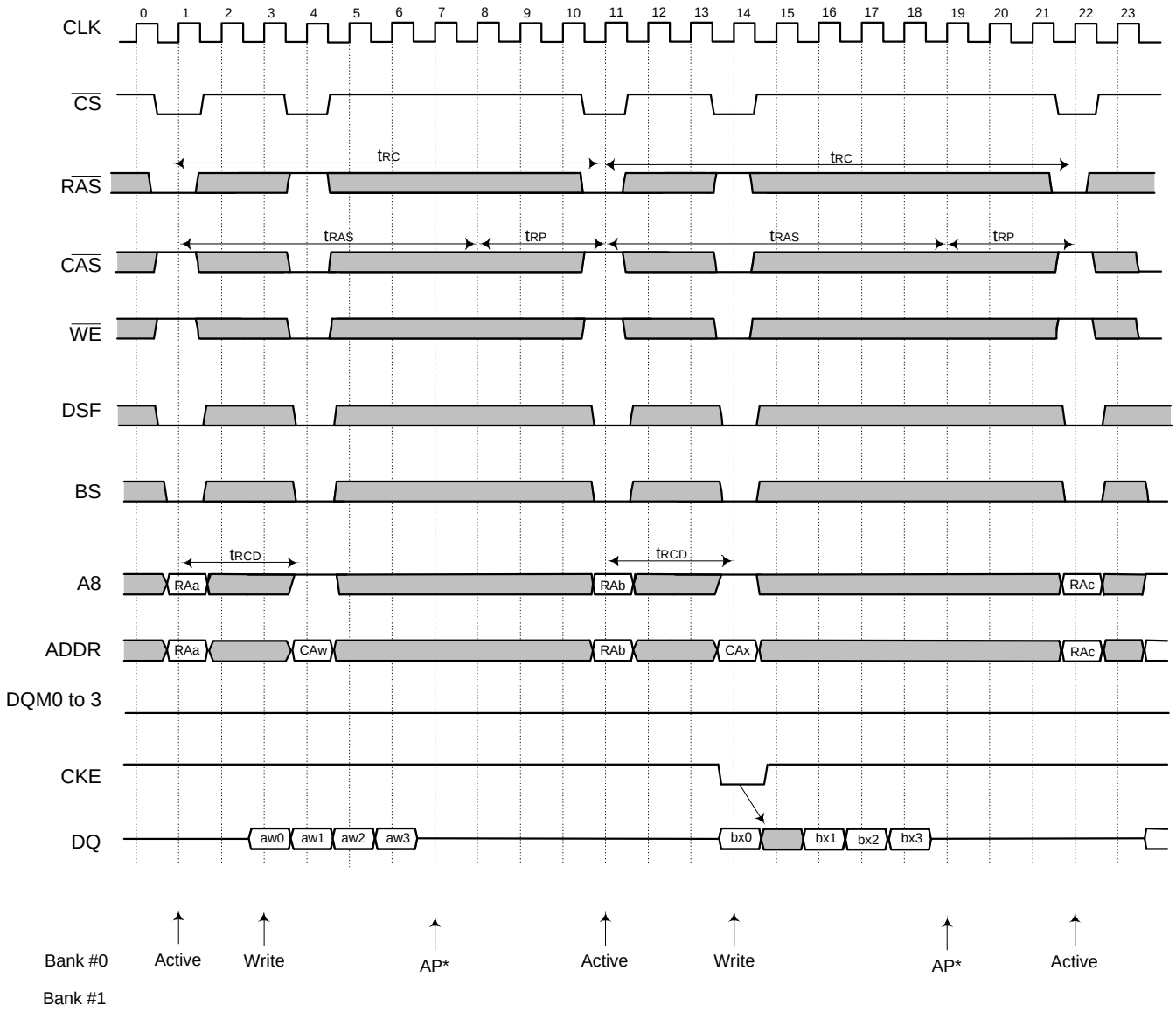
Auto Precharge Read (Burst Length = 4, CAS Latency = 3)



* AP is the internal precharge start timing

Auto Precharge Write (Burst Length = 4)

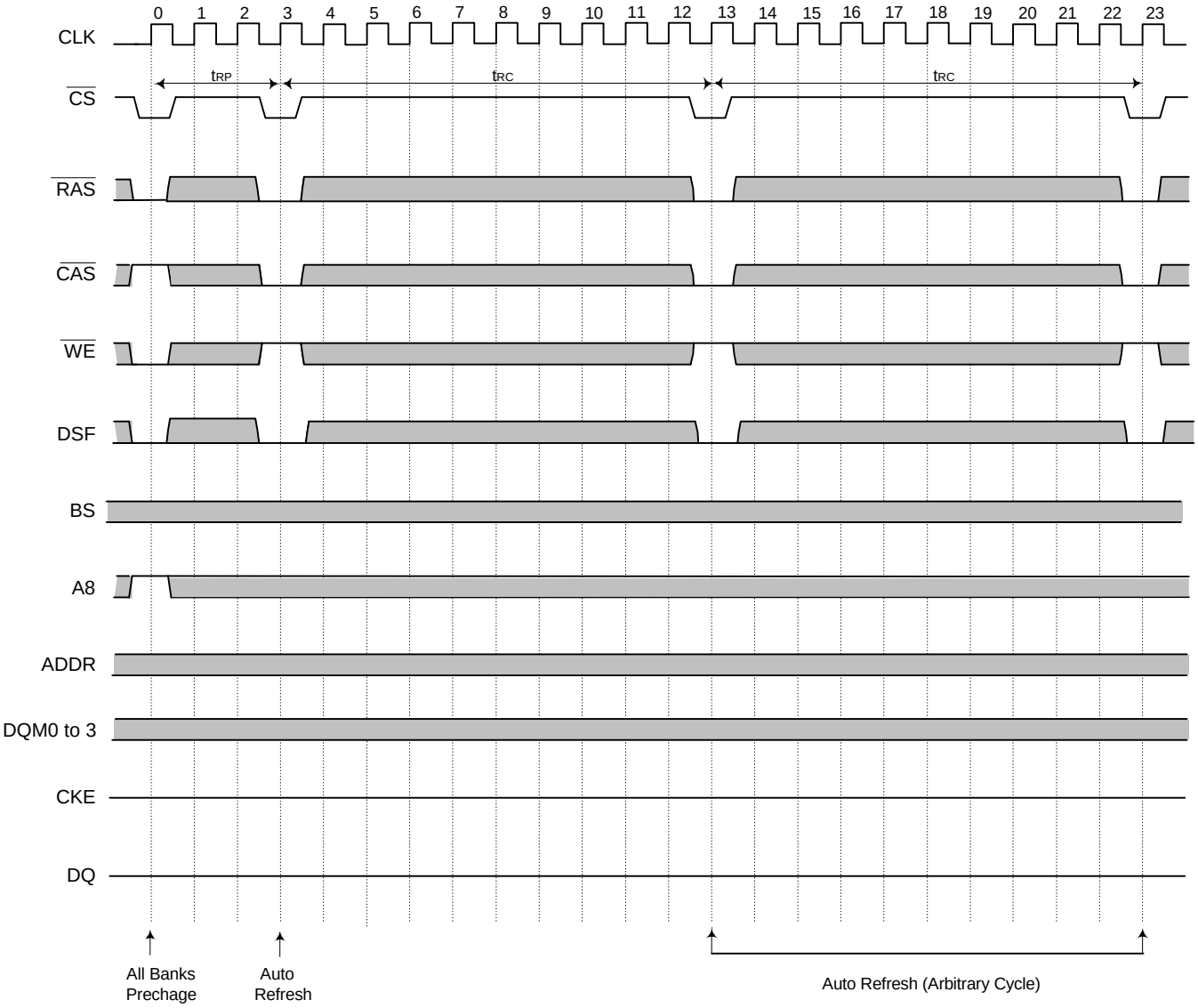
(CLK = 100 MHz)



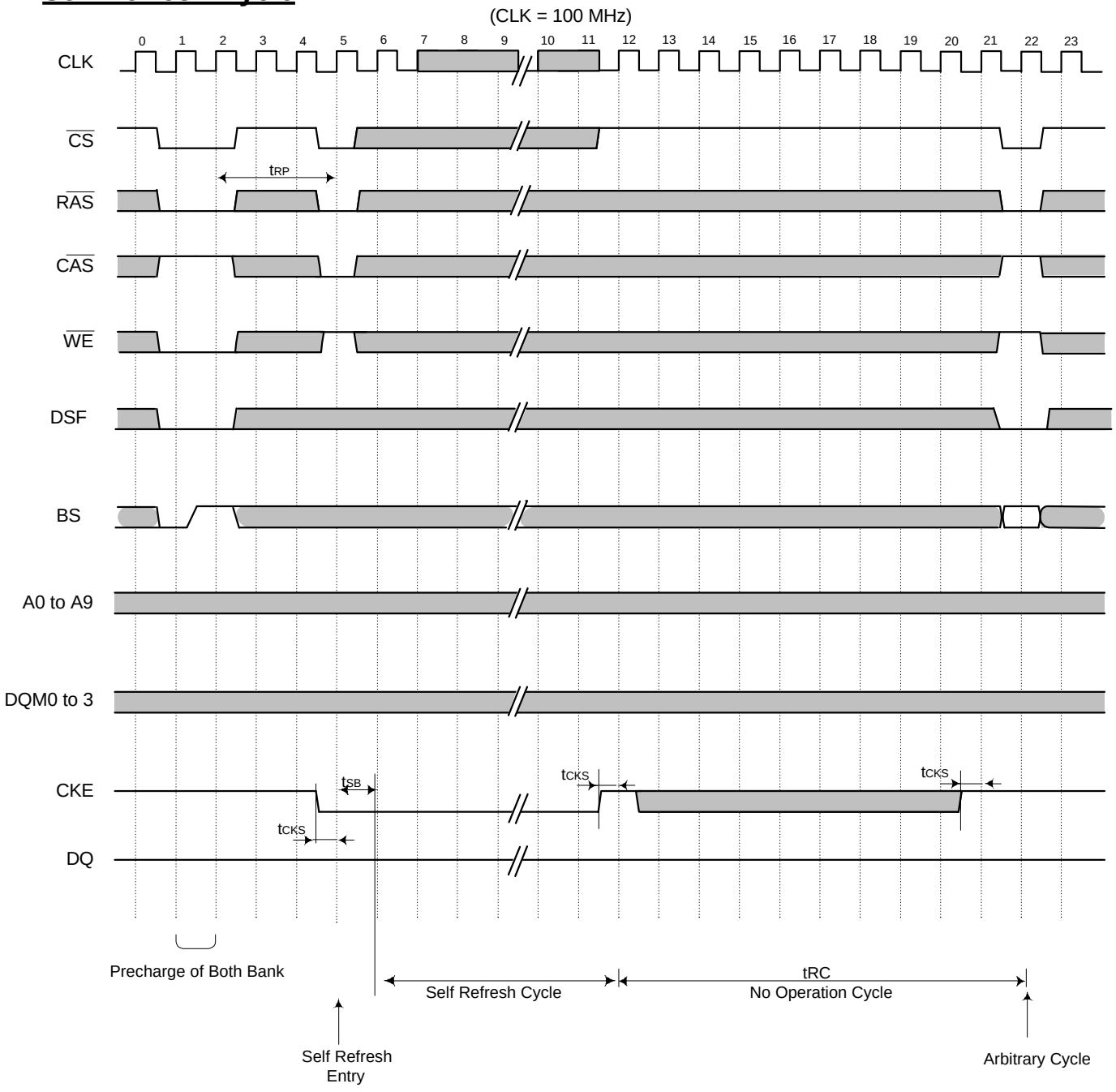
* AP is the internal precharge start timing

Auto Refresh cycle

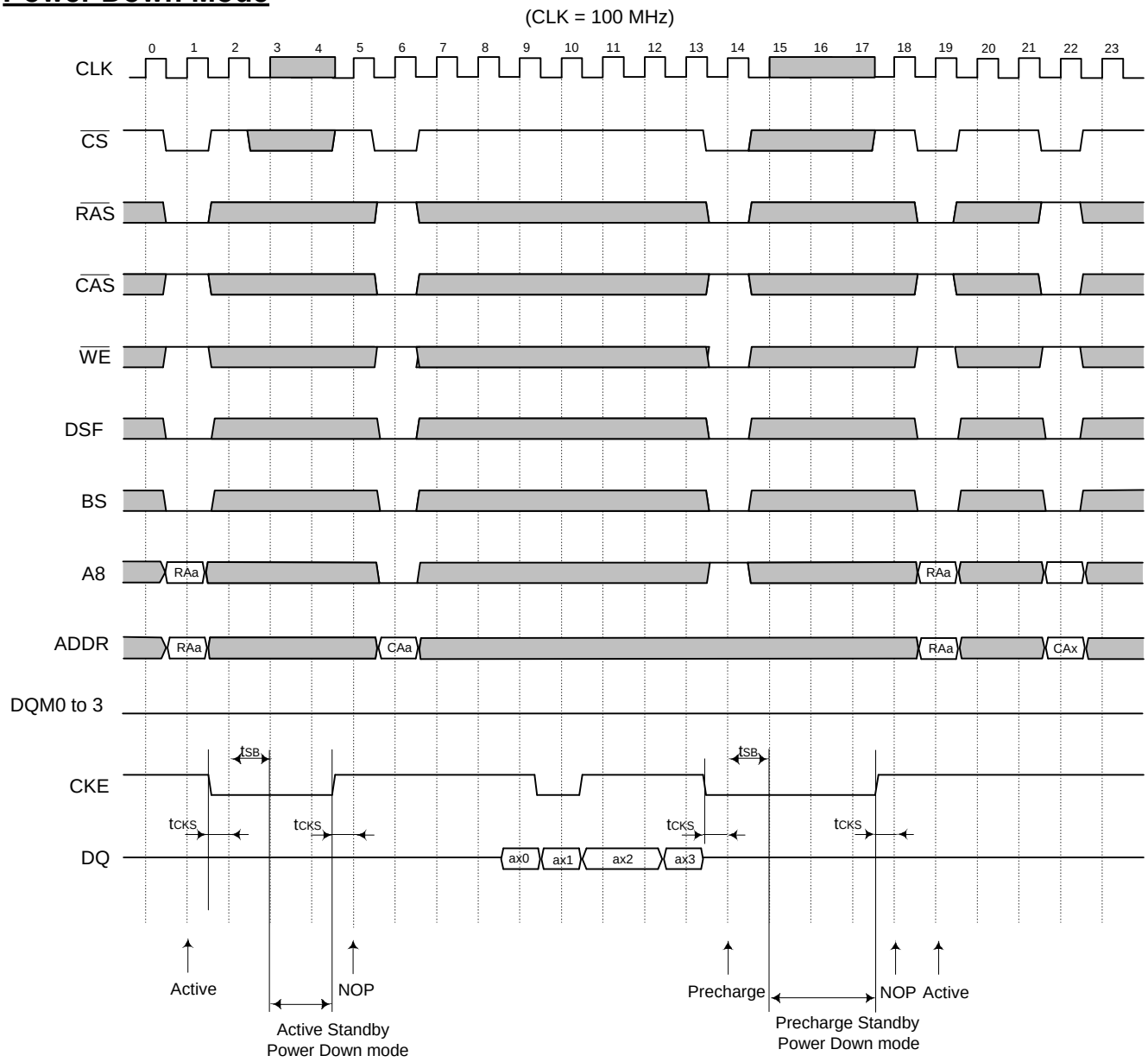
(CLK = 100 MHz)



Self Refresh Cycle

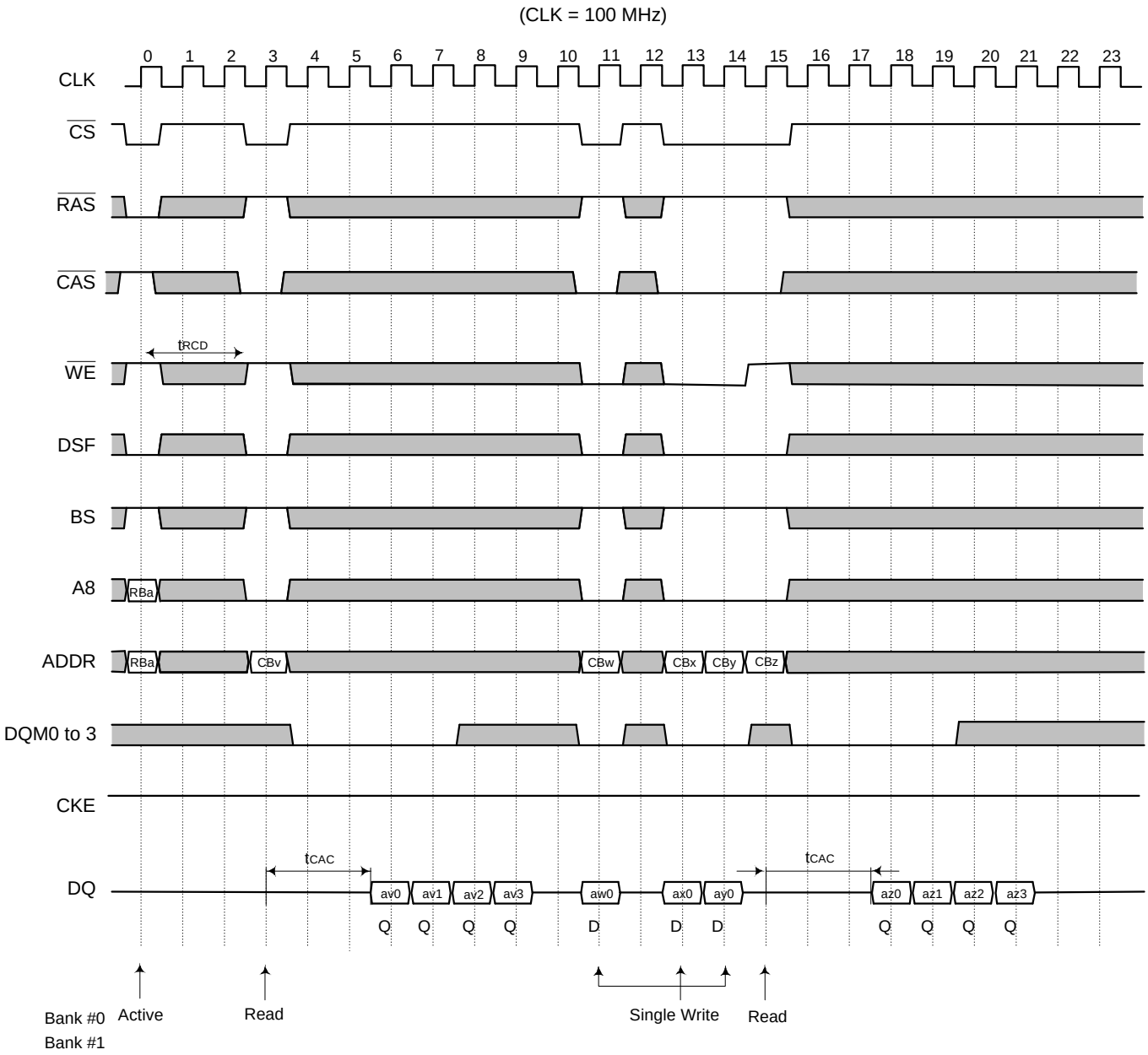


Power Down Mode



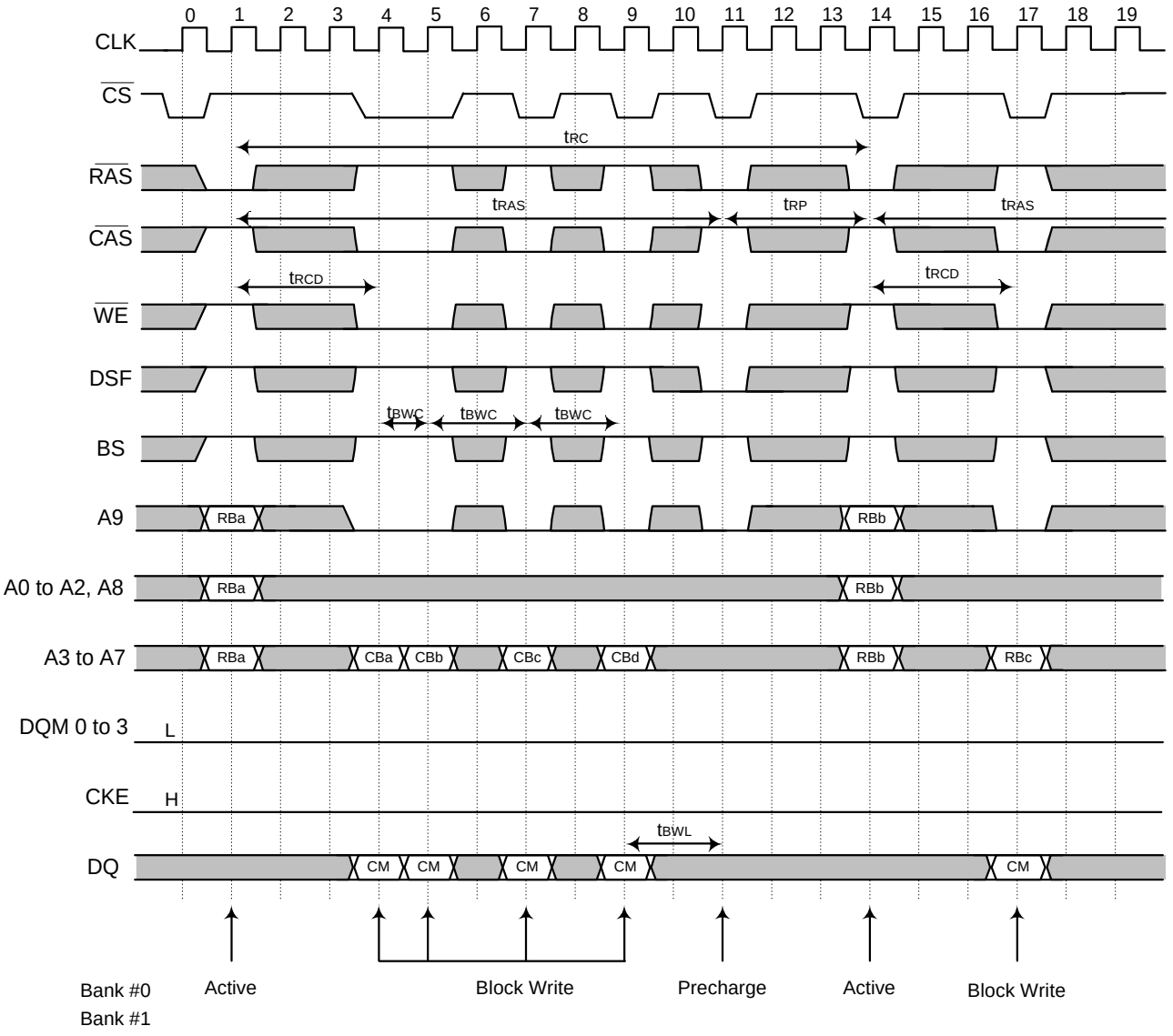
Note: The PowerDown Mode is entered by asserting CKE "low".
All Input/Output buffers (except CKE buffers) are turned off in the PowerDown mode.
When CKE goes high, command input must be No operation at next CLK rising edge.

Burst Read and Single Write (Burst Lenght = 4, CAS Latency = 3)

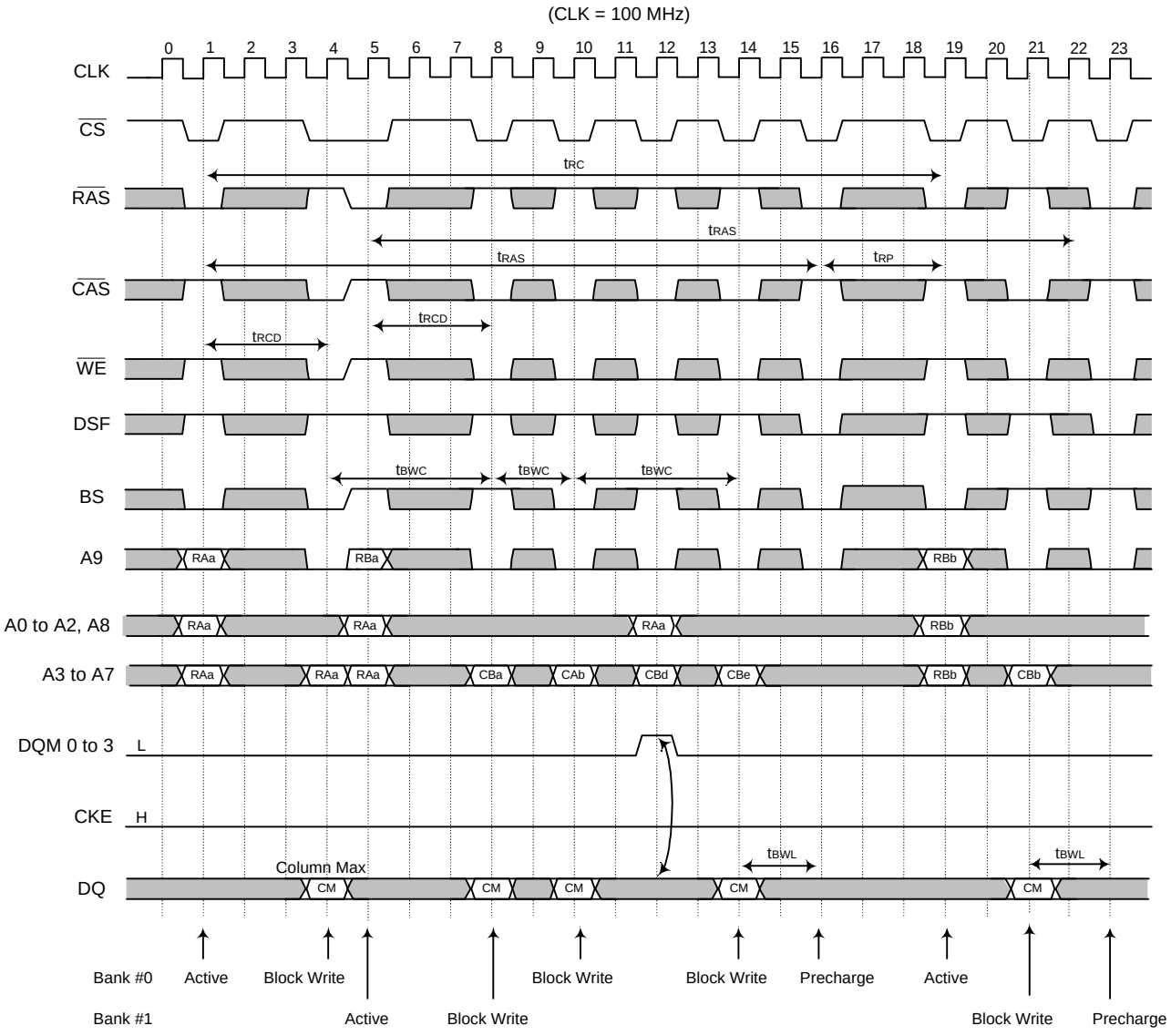


Page Mode Block Write($\overline{CAS}$ Latency=3)

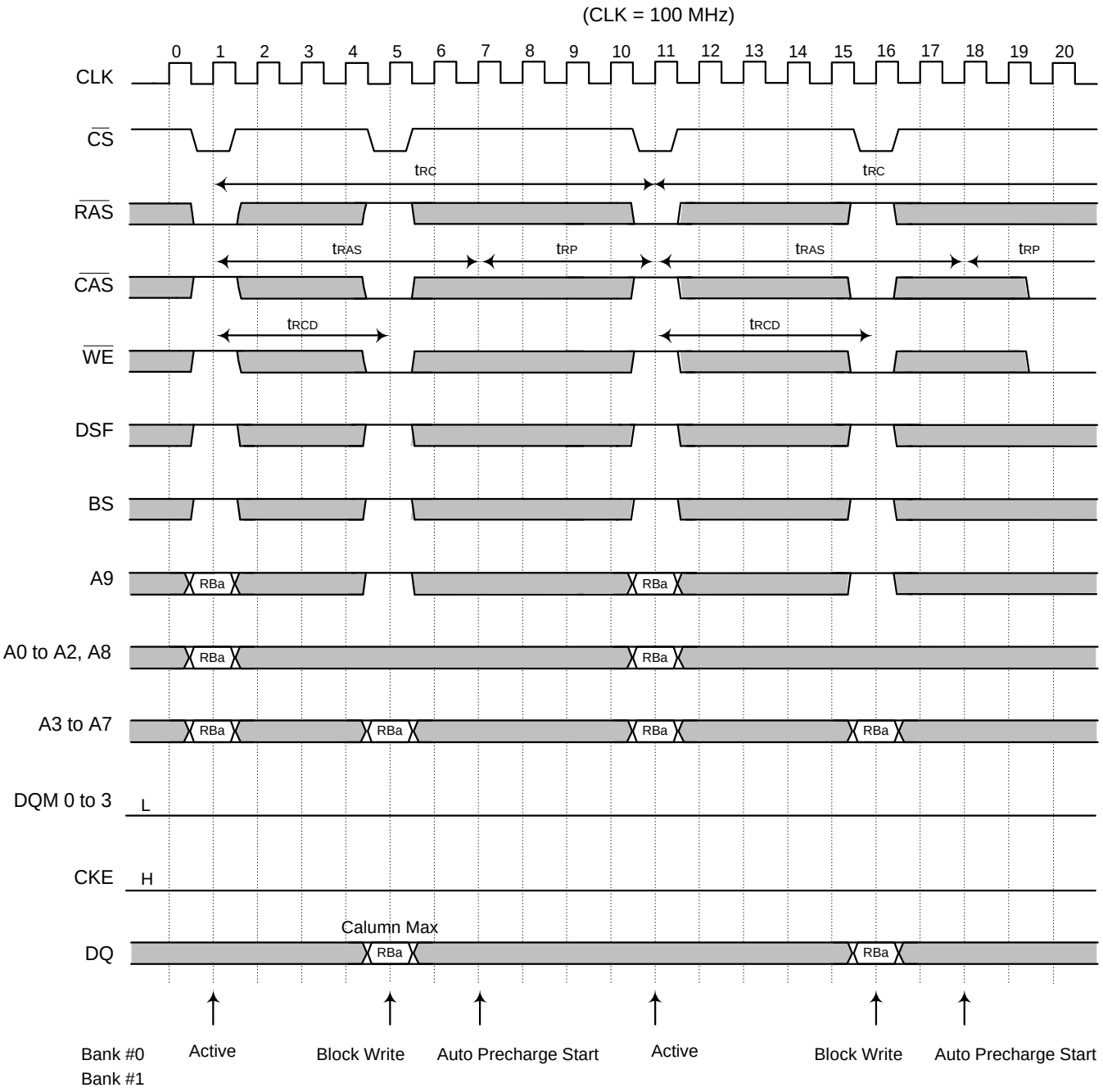
(CLK = 100 MHz)



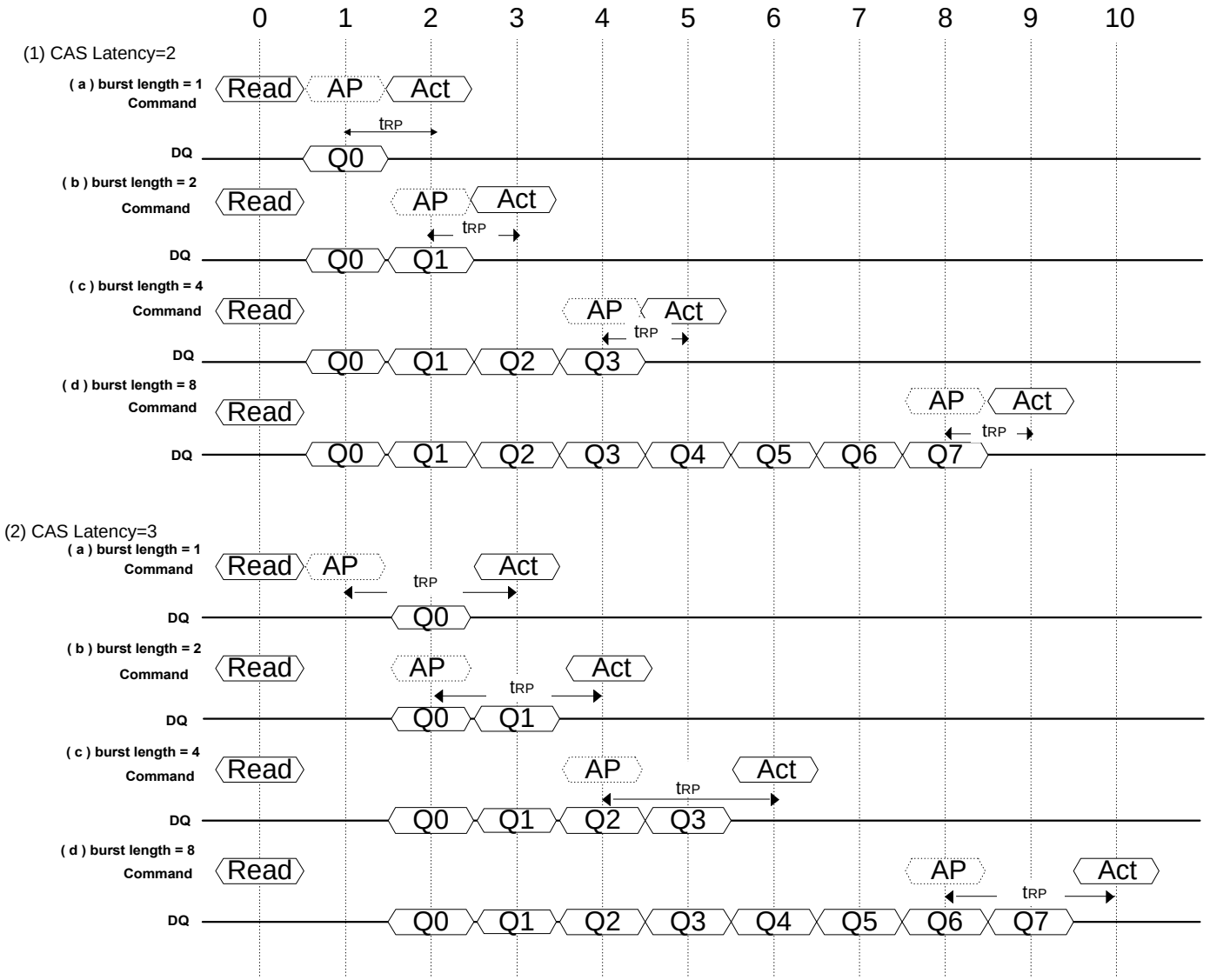
Interleaved Block Write ($\overline{CAS}$ Latency=3)



Auto Precharge Block Write(CAS Latency=3)



Auto Precharge Timing (Read Cycle)

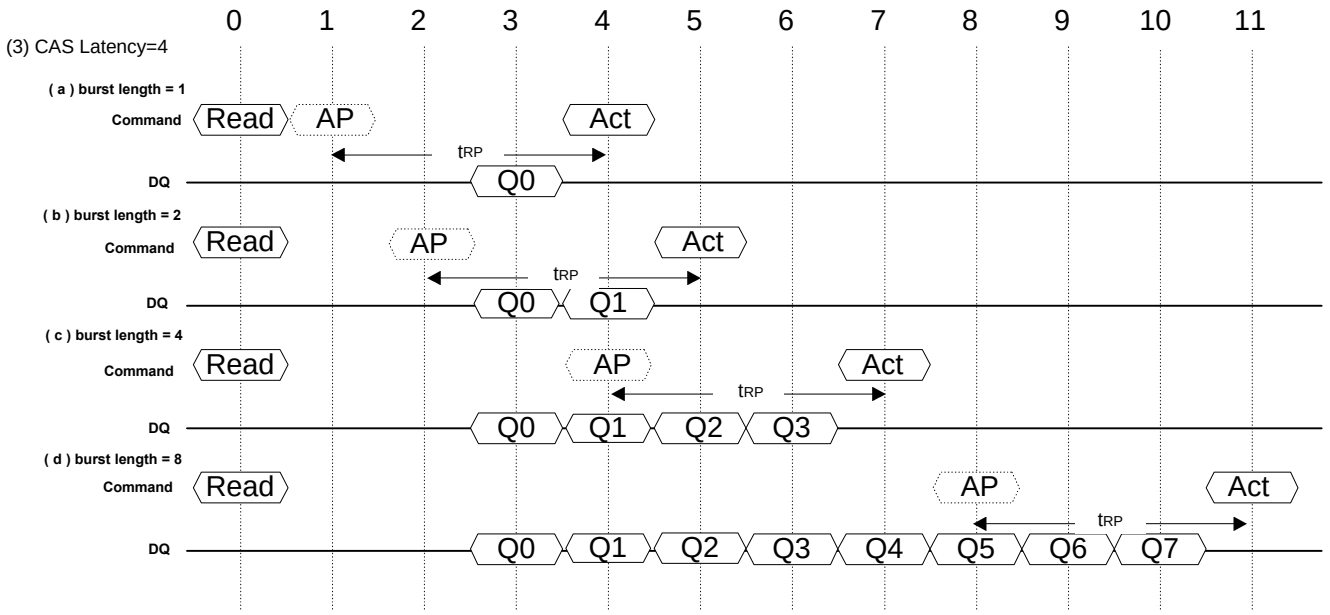


Note)

Read	represents the Read with Auto precharge command.
AP	represents the start of internal precharging.
Act	represents the Bank Activate command.

When the Auto precharge command is asserted, the period from Bank Activate command to the start of internal precgarging must be at least tRAS(min).

Auto Precharge timing (Read Cycle)



Note)

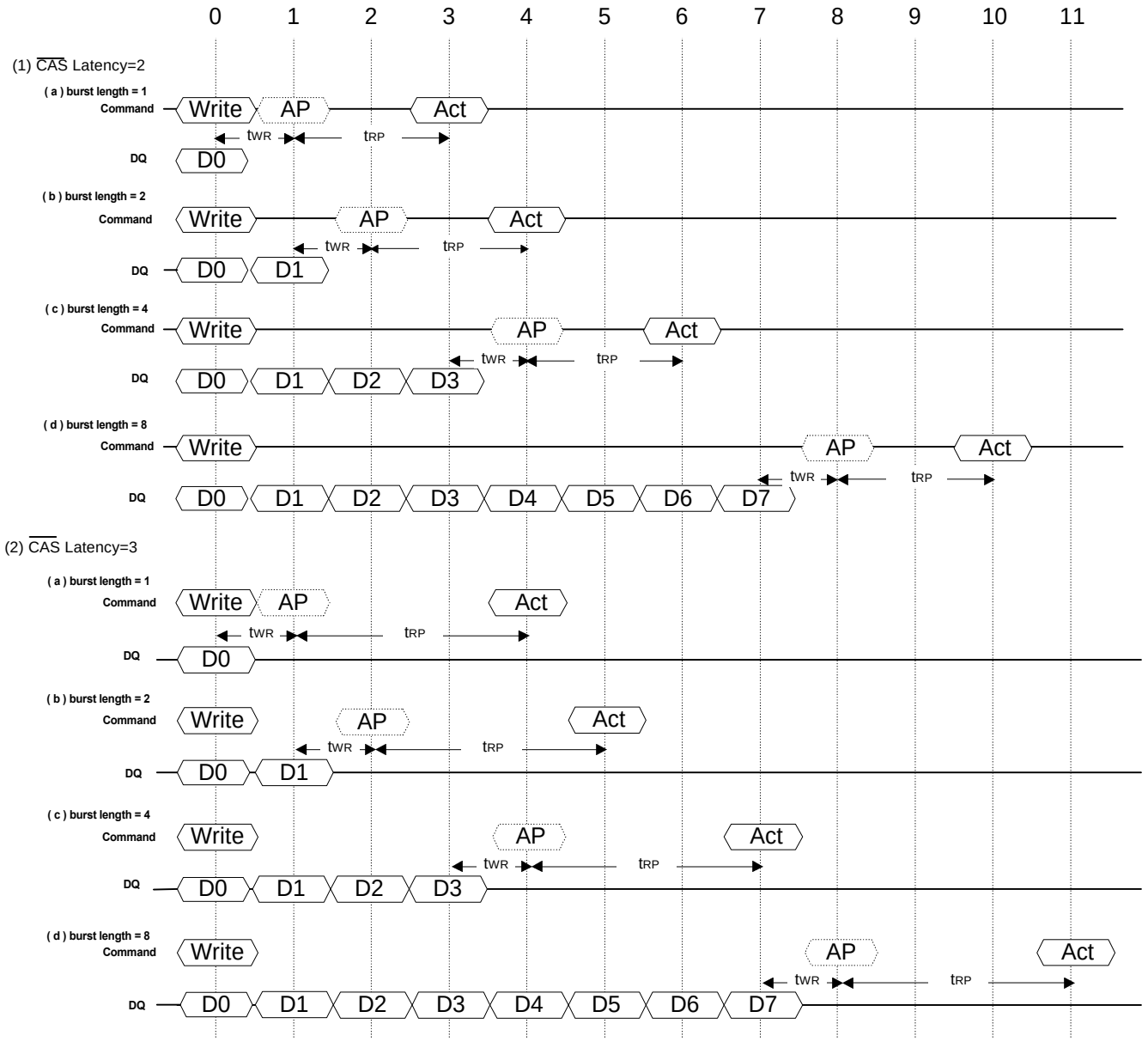
Read represents the Read with Auto precharge command.

AP represents the start of internal precharging.

Act represents the Bank Activate command.

When the Auto precharge command is asserted, the period from Bank Activate command to the start of internal precgarging must be at least tRAS(min).

Auto Precharge timing (Write Cycle)



Note)

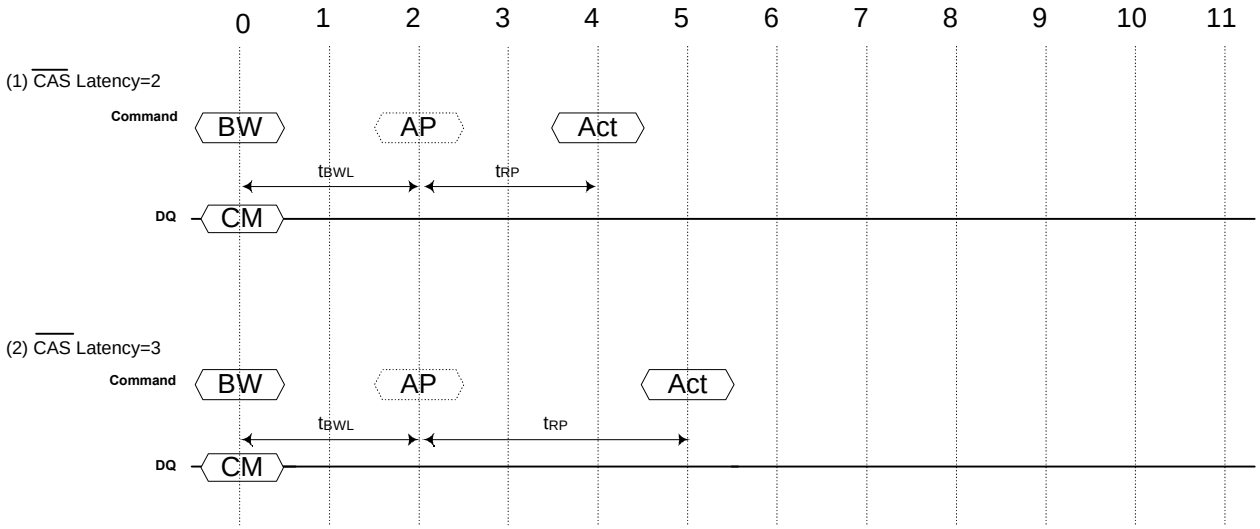
Write represents the Write with Auto precharge command.

AP represents the start of internal precharging.

Act represents the Bank Activate command.

When the Auto precharge command is asserted, the period from Bank Activate command to the start of internal precgarging must be at least t_{RAS}(min) .

Auto Precharge Timing (Block Write cycle)

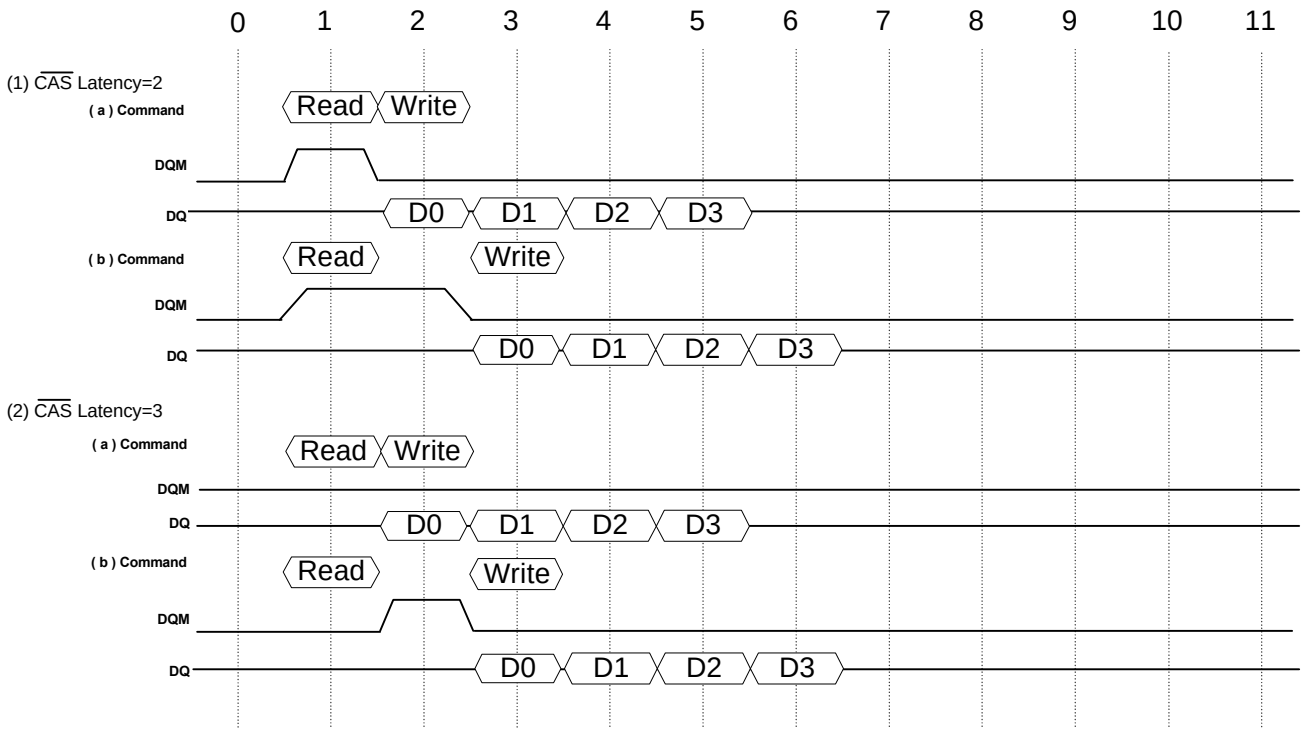


Notes
- BW represents the Read with Auto Precharge command
- AP represents the atart of internal precharging
- Act represents the Bank Activate command

When the Auto precharge command is asserted , the period from the Bank Activate command to the start of internal prechargeing must be at least t_{RAS} (min)

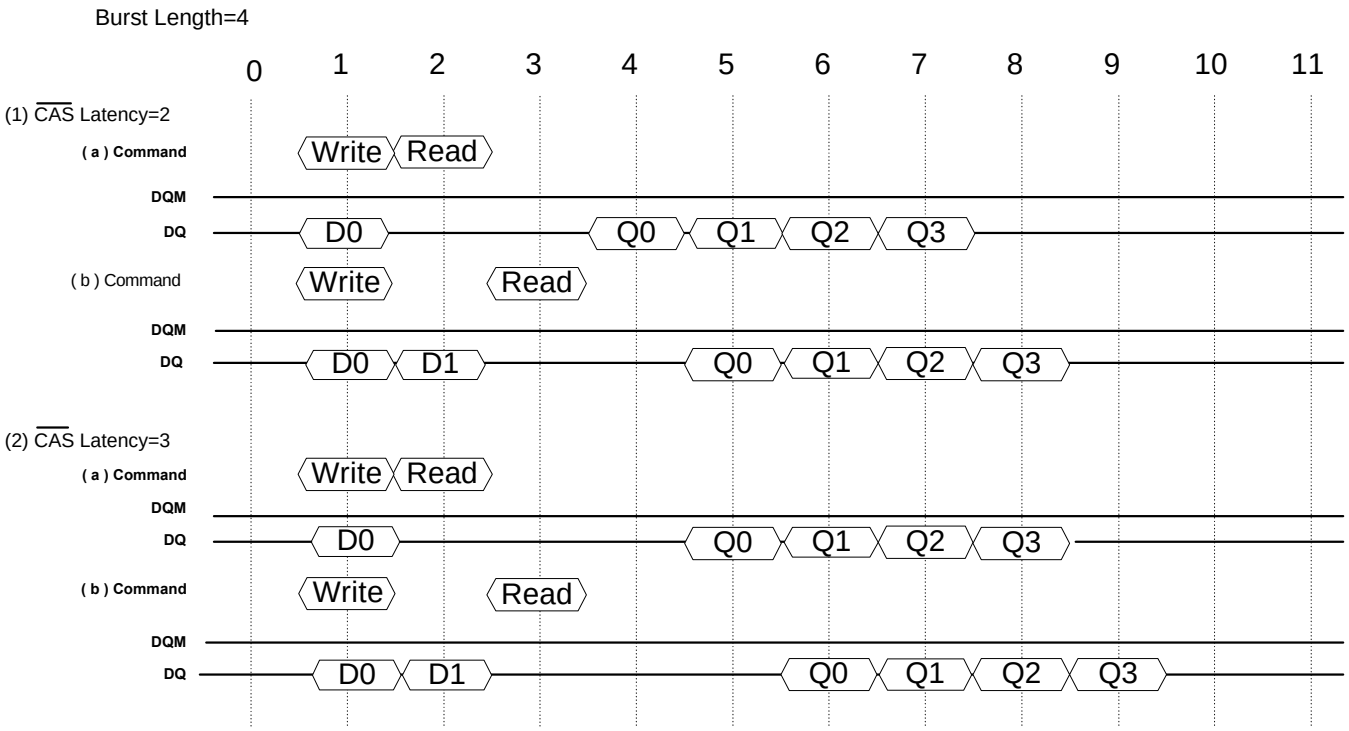
Timing Chart of Read to Write cycle

Burst Length=4

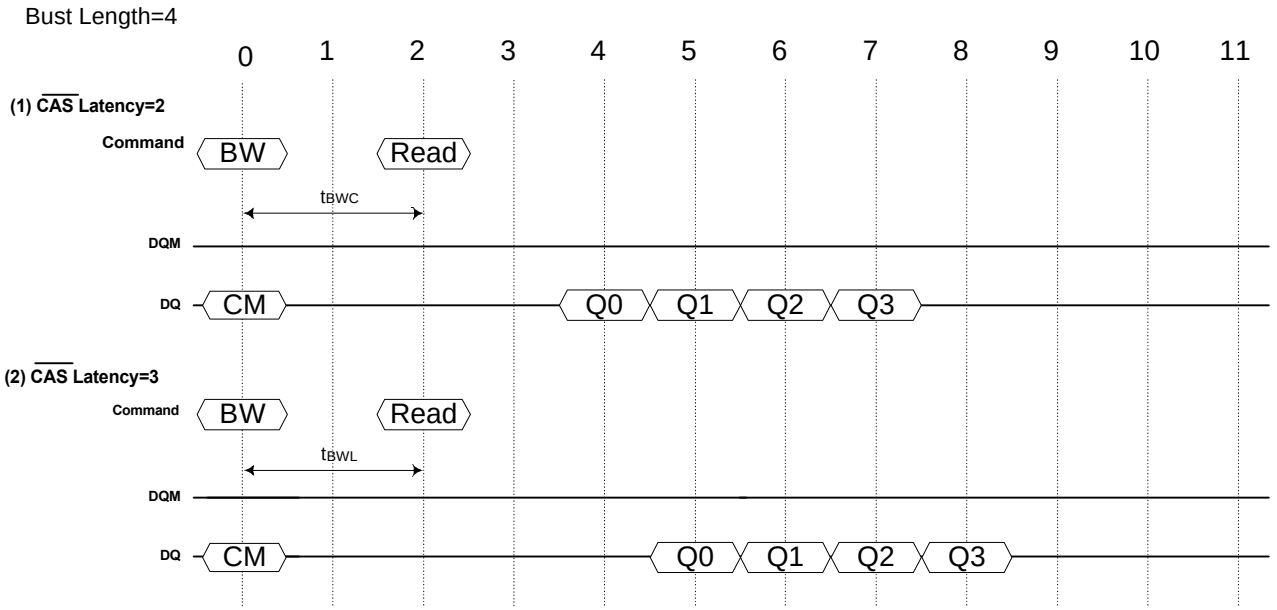


Note: The Output data must be masked by DQM to avoid I/O conflic t

Timing Chart of Write-to-Read cycle



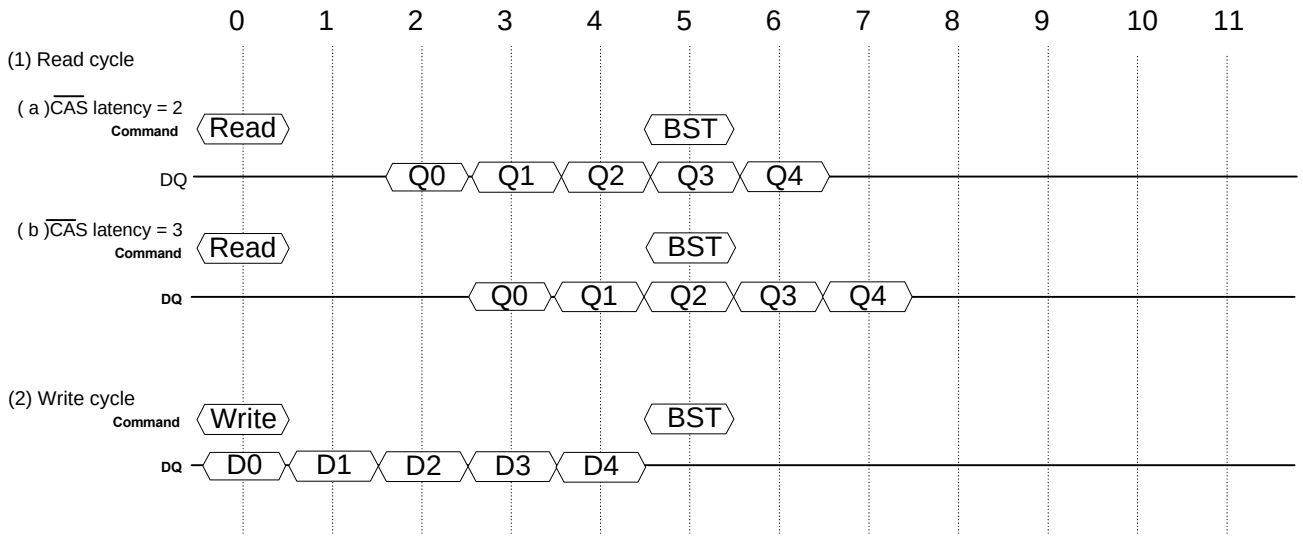
Timing chart for Block Write-to-Read cycle



Notes BW represents the Block Write command

CM represents Column mask command

Timing chart of Burst Stop cycle (Burst Stop Command)

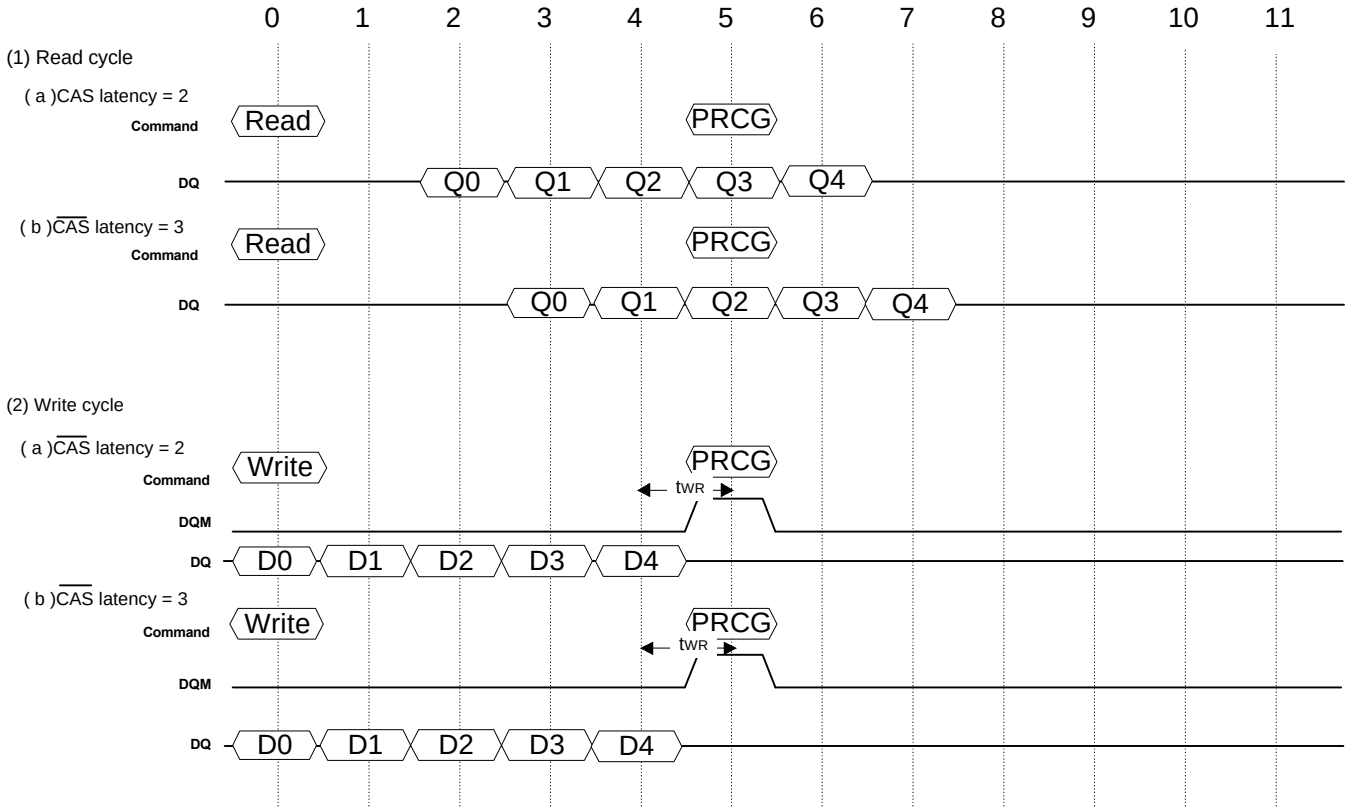


Note: BST represents the Burst stop command

The Burst Stop command is effective in 1-, 2-, 4- and 8-word bursts in a Full Page cycle

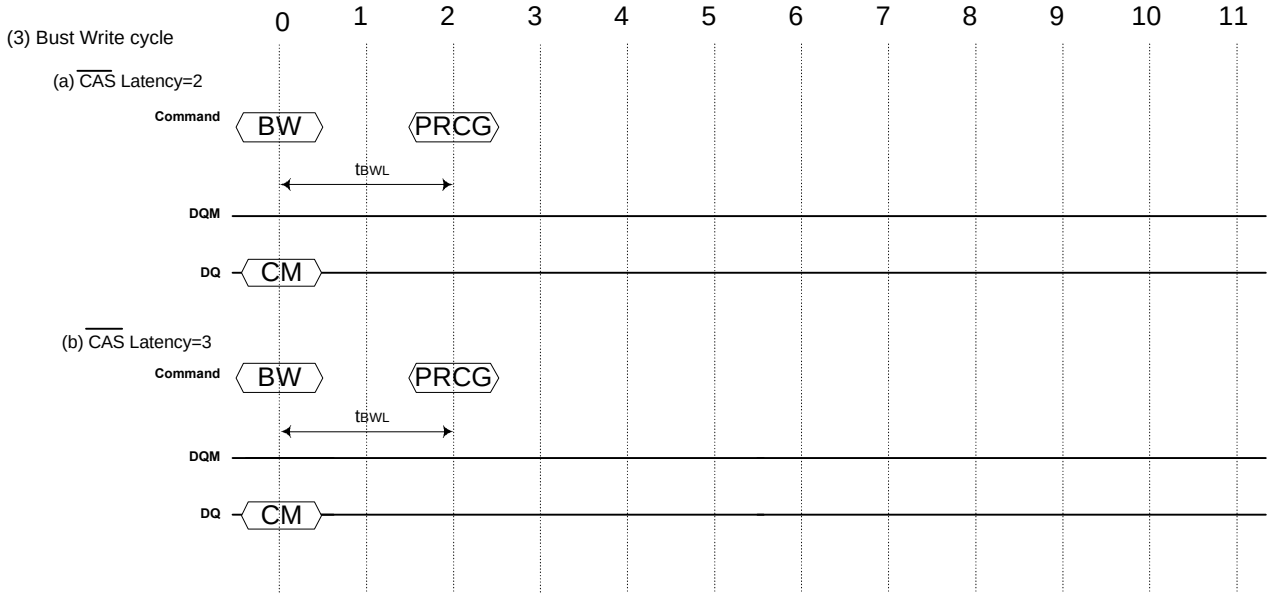
Timing chart of Burst Stop cycle (Precharge Command)

In the case of Burst Lenght = 8



Note : PRCG represents the Precharge command

Timing chart for Block Write to Precharge cycle



Notes: BW represents the Block Write command

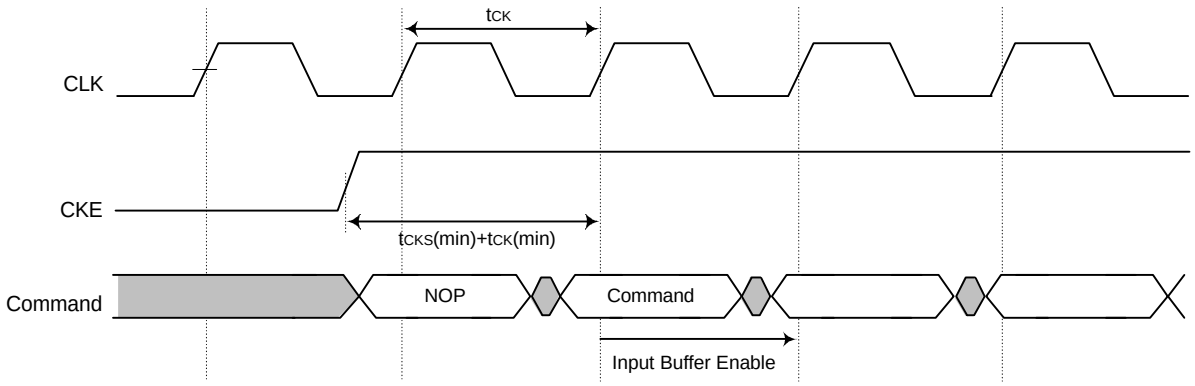
PRCG represents the Precharge command

Self-Refresh/Power-down Mode Exit Timing

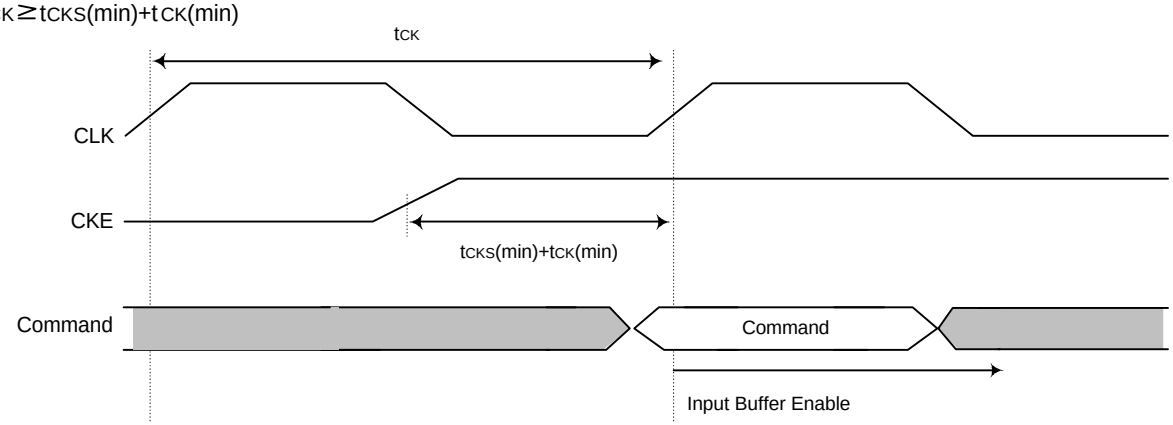
Asynchronous Control

Input Buffer turn-on time (Power-down Mode exit time) is specified by $t_{CKS}(min)+t_{CK}(min)$

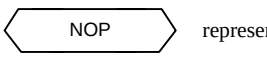
A) $t_{CK}<t_{CKS}(min)+t_{CK}(min)$



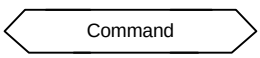
B) $t_{CK} \geq t_{CKS}(min)+t_{CK}(min)$



Notes: All input buffer (including the CLK buffer) are turned off in Power-down mode and Self-Refresh mode

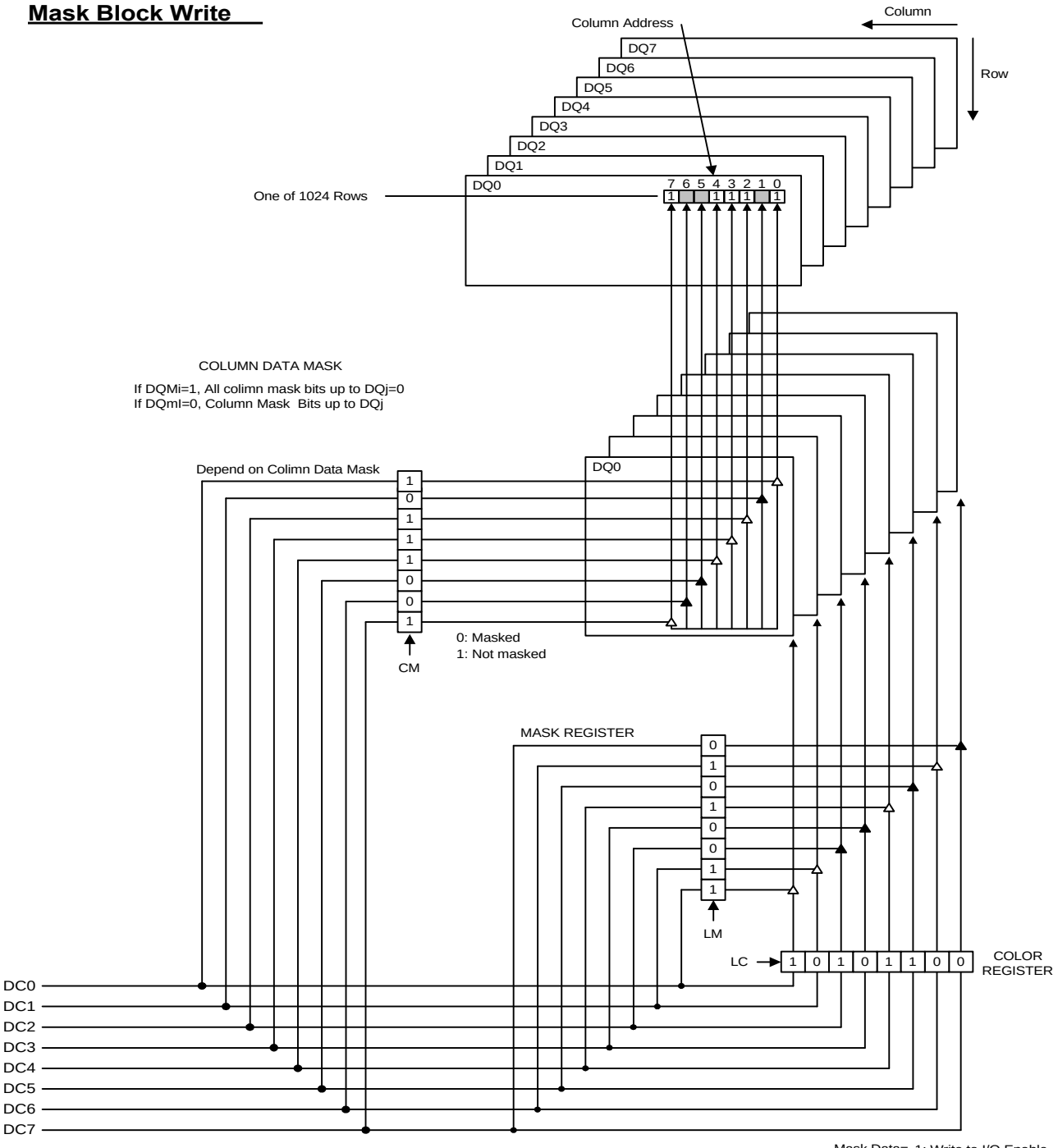


represents the No Operation command



represents a single command

Mask Block Write



Notes: The block write s are non-burswrites
If DSF=L when the Bank Active command is executed, then the I/O Mask is disbled for the active bak
If DSF=H when the Bank Active command is executed, then the I/O Mask is enabled for the active bak
Mask Data=Mask Register + DQMi(i=0 to 3)

Mask Data= 1: Write to I/O Enable
0: Write to I/O Disable

DQMi	0	1	2	3
DQj	0 to 7	8 to 15	16 to 23	24 to 31

Example (Only the least significant byte shown. The operation is identical for all other bytes)

	DQ							
	0	1	2	3	4	5	6	7
Mask Register (LM)	1	1	(0)	(0)	1	(0)	1	(0)
Color Register (LC)	1	0	1	0	1	1	0	0
Column Data Mask (CM)	1	(0)	1	1	1	(0)	(0)	1

Result

	DQ							
	0	1	2	3	4	5	6	7
Column 0	1	0			1		0	
Column 1								
Column 2	1	0			1		0	
Column 3	1	0			1		0	
Column 4	1	0			1		0	
Column 5								
Column 6								
Column 7	1	0			1		0	

Column Mask

Column 0 (A2C=0, A1C=0, A0C=0) ... DQj/IOj=0, 8, 16, 24

Column 1 (A2C=0, A1C=0, A0C=1) ... DQj/IOj=1, 9, 17, 25

Column 2 (A2C=0, A1C=1, A0C=0) ... DQj/IOj=2, 10, 18, 26

Column 3 (A2C=0, A1C=1, A0C=1) ... DQj/IOj=3, 11, 19, 27

Column 4 (A2C=1, A1C=0, A0C=0) ... DQj/IOj=4, 12, 20, 28

Column 5 (A2C=1, A1C=0, A0C=1) ... DQj/IOj=5, 13, 21, 29

Column 6 (A2C=1, A1C=1, A0C=0) ... DQj/IOj=6, 14, 22, 30

Column 7 (A2C=1, A1C=1, A0C=1) ... DQj/IOj=7, 15, 23, 31

Example

If DQ0=1 when the Block Write command is executed, the Column 0 Data Mask is 1 (not masked)

If DQ0=0 when the Block Write command is executed, the Column 0 Data Mask is 0 (masked)

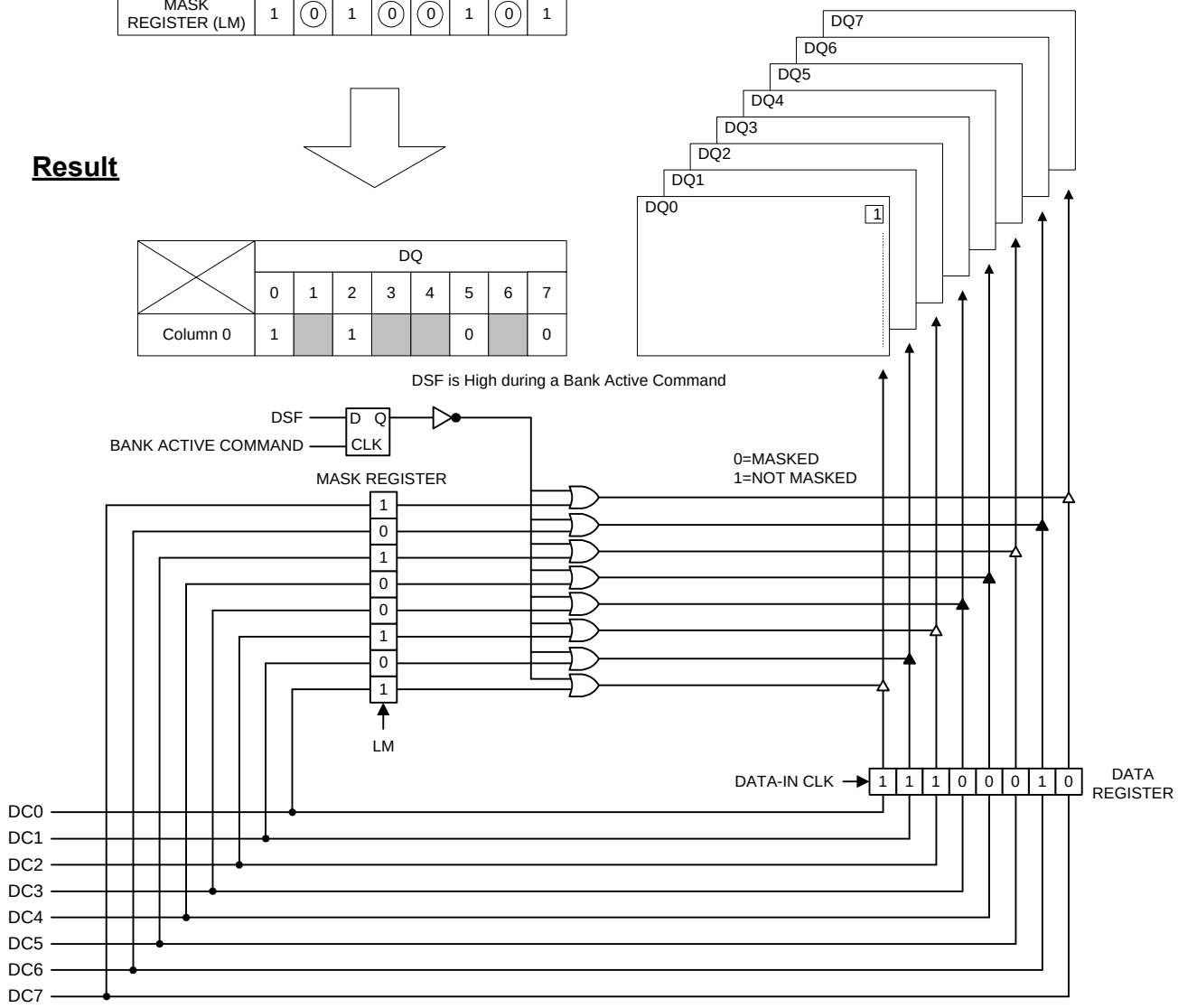
Write-per-Bit

Example (Only the least significant byte shown. The operation is identical for all other bytes)

	DQ							
	0	1	2	3	4	5	6	7
DATA-IN	1	1	1	0	0	0	1	0
MASK REGISTER (LM)	1	(0)	1	(0)	(0)	1	(0)	1

Result

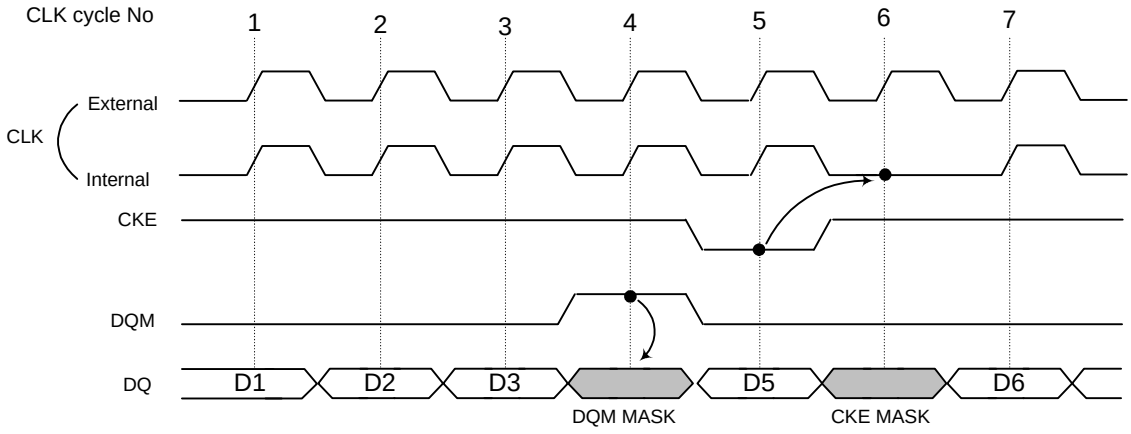
	DQ							
	0	1	2	3	4	5	6	7
Column 0	1		1			0		0



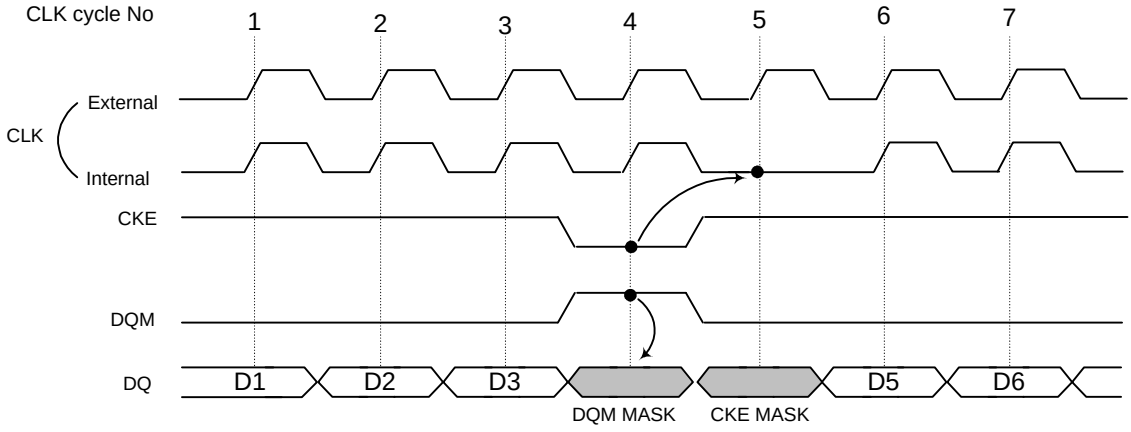
Notes: The Write-per-Bit can be performed in a bust.
If DSF=L when the Bank Active command is executed, then the I/O Mask is disbled for the active bak
If DSF=H when the Bank Active command is executed, then the I/O Mask is enabled for the active bak
Mask Data=Mask Register + DQMi(i=0 to 3)

Mask Data= 1: Write to I/O Enable
0: Write to I/O Disable

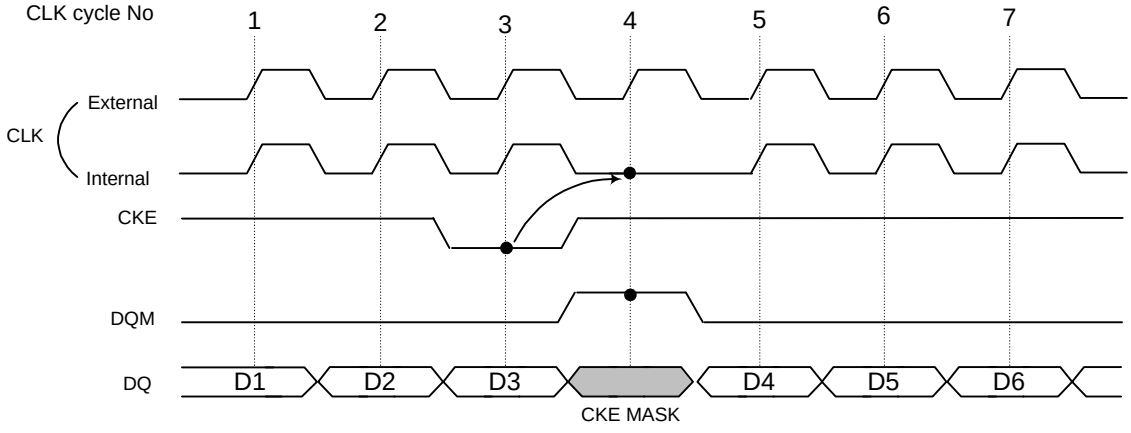
CKE/DQM input timing (Write cycle)



(1)

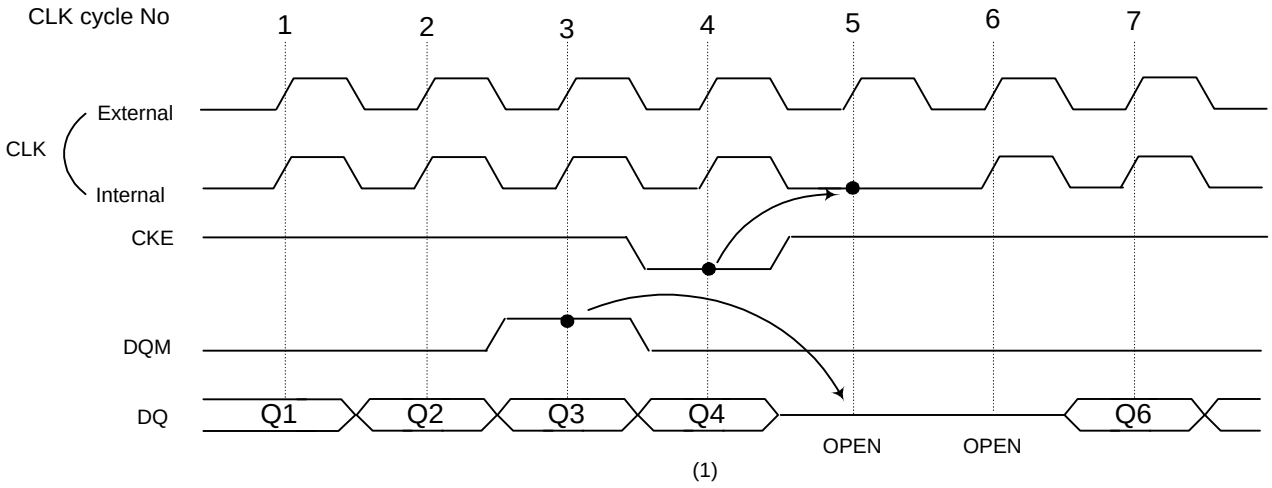


(2)

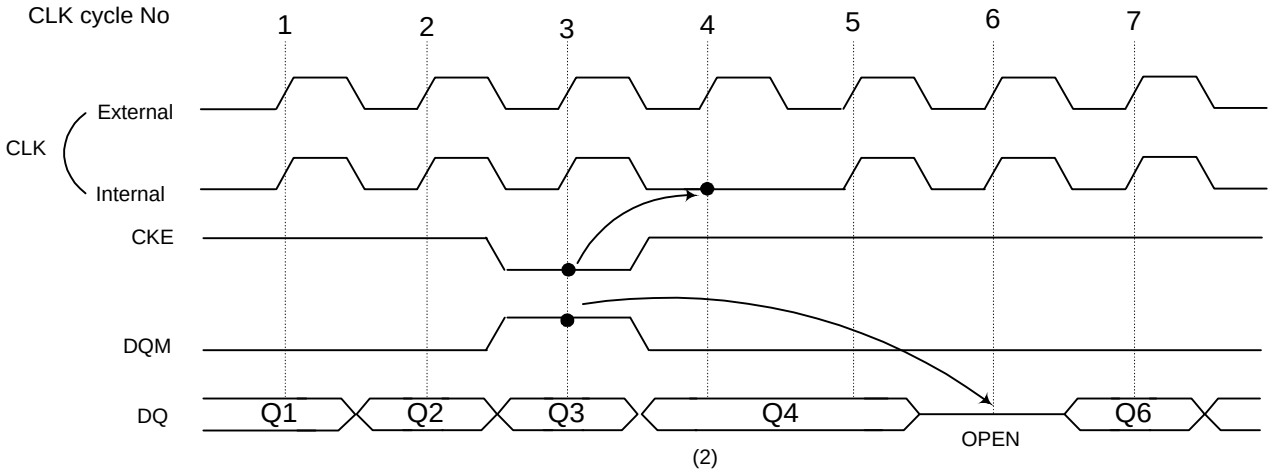


(3)

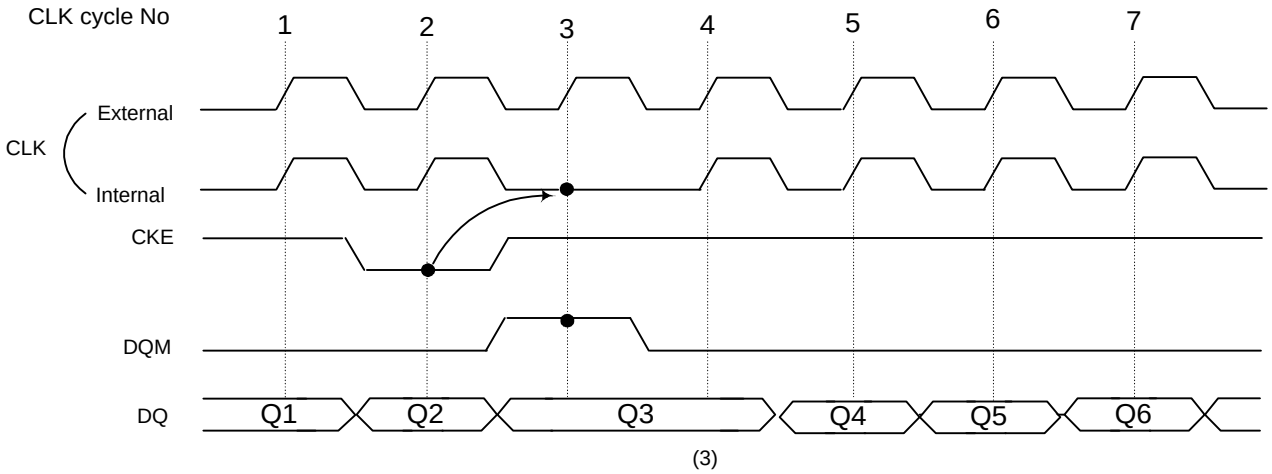
CKE/DQM input timing (Read cycle)



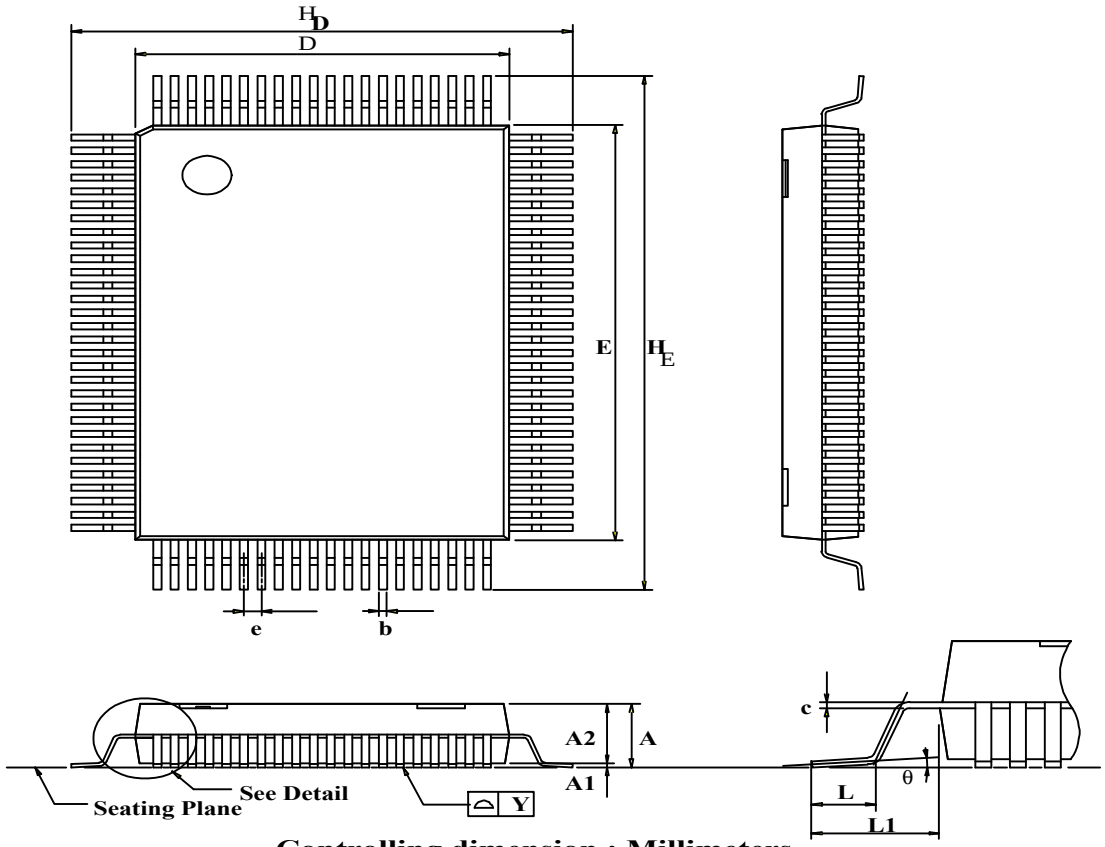
(1)



(2)



(3)



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.130	—	—	3.30
A1	0.010	0.014	0.018	0.25	0.35	0.45
A2	0.101	0.107	0.113	2.57	2.72	2.87
b	0.008	0.012	0.016	0.20	0.30	0.40
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.547	0.551	0.555	13.90	14.00	14.10
E	0.783	0.787	0.791	19.90	20.00	20.10
e	0.020	0.026	0.032	0.50	0.65	0.80
H_D	0.669	0.677	0.685	17.00	17.20	17.40
H_E	0.905	0.913	0.921	23.00	23.20	23.40
L	0.025	0.031	0.037	0.65	0.80	0.95
L1	—	0.063	—	—	1.60	—
Y	—	—	0.003	—	—	0.08
θ	0°	—	7°	0°	—	7°