FT7C964A

VME Interface Component

The FT7C964A is a VME interface component, pin-compatible with the now-discontinued Cypress CY7C964. The FT7C960 VME controller in concert with FT7C964A interface chips provides a simple VME interface solution.

Feature Summary

- High-current drivers for direct connection to VME address and data bus signals
- Cascadable to support multiple VME widths
- VME address matching
- Address counters for block transfers and local bus DMA.
- Supports all standard (Rev. C) VMEbus transactions
- 80-Mbyte-per-second block transfer rates
- Multiplexers for D64 support
- 64 pin PQFP=U / CQFP=F / C2QFP="F2"

Blank-=0oC to +70oC / I=-40oC to +85oC

M-Military -55oC to +100oC (Contact office)

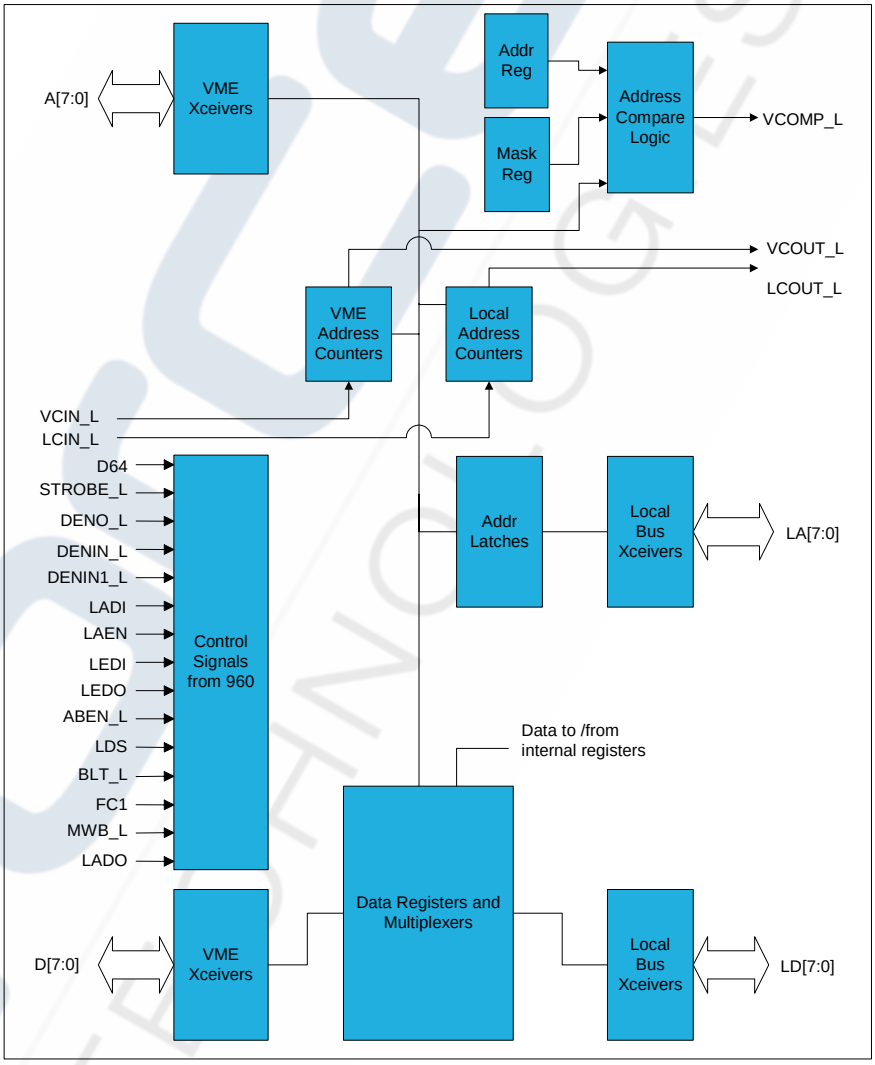
Applications

VME64 has been widely used in industrial and military applications. The FT7C964A with the FT7C960 provides an integrated solution for VME and VME64 Slave devices.

The Force synthesisable core for the FT7C964A has been widely used to generate functional replacements for the Cypress CY7C964. The FT7C964A now provides a direct chip level replacement, requiring no printed circuit board changes.

Example:			
FT7C964	A	XX	X
Part No.	Rev	Pkg	Temp

"Block Diagram



General Description

The FT7C964A is a byte-slice VME address and data interface. Force Technologies also provides the FT7C960, a pin compatible replacement device for the CY7C960 chips. The FT7C964A together with the FT7C960 provide a complete VME slave interface solution.

The FT7C964A is cascadable to support D8, D16, D32, MD32 and D64 data transfers. It can also support A16, A24, A32, A40, A64 addressing modes. Single-cycle and block-transfer read and write cycles, Read-Modify-Write cycles and Address-only cycles are all supported.

General Description

(continued)

The FT7C964A contains three address counters to support both master and slave block transfers. One counter supplies the local address during master block transfer operations, A second counter provides the local address during slave block transfers, and also serves as the address latch for non-block transfer slave operations. The third counter provides the VME address during VME master block transfers.

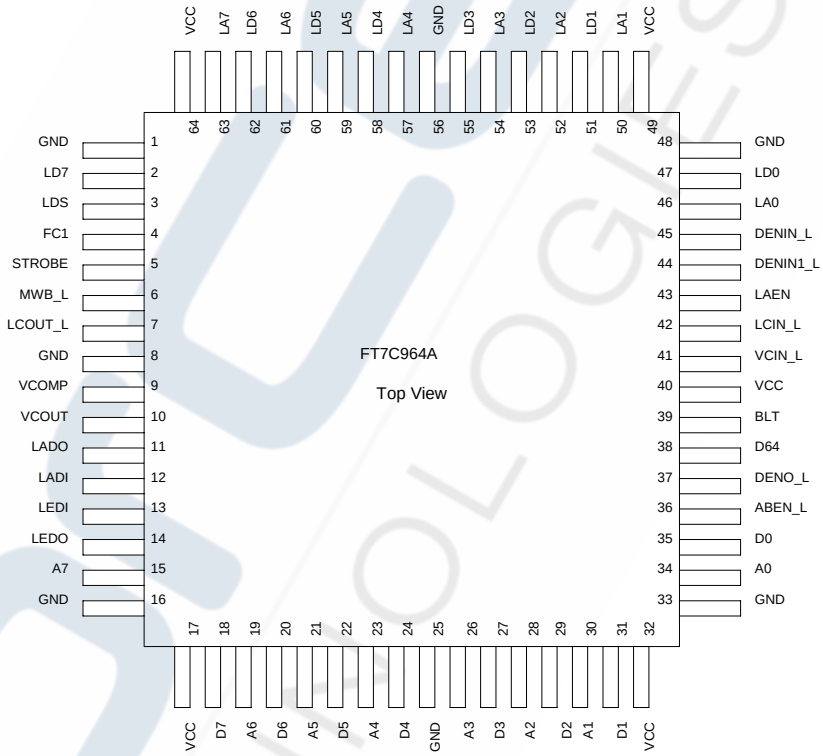
The address comparison logic comprises a base address register, a mask register. The VCOMP_L output is driven low when the VME address bits selected by the mask register match the corresponding bits in the base address register.

In D64 operation, data are transferred over both the VME A and D pins. The FT7C964A handles the sequencing and routing of data between the local data (LD) pins and the A and D pins appropriately.

FT7C964A—CY7C964 A Comparison

Functionally, the FT7C964A and CY7C964 are the equivalent. With the FT7C964A, in D64 mode (when data are driven on both the D and A signals,) the VME drive current limit to is reduced to 20 ma per pin.

Pin Configuration



Package - 64 pin PQFP

Pin Description

Signal	Signal Direction	Description
A(7:0)	Bidir	VME address
D(7:0)	Bidir	VME data
LA	Bidir	Local address bus
LD	Bidir	Local data bus
LCOUT_L	Out	Local address counter enable out
VCOUT_L	Out	VME address counter enable out
VCOMP_L	Out	VME address compare out
D64	Input	FT7C960 interface - Informs external hardware D64 VME block xfer in progress
STROBE_L	Output	FT7C960 interface - Used during INIT to load 964 regs
DENO_L	Input	FT7C960 interface - Data Enable Out - Enables VME data drivers
DENIN_L	Input	FT7C960 interface - Data Enable In; used with DENIN1_L and SWDEN_L
DENIN1_L	Input	FT7C960 interface - Data Enable In; used with DENIN_L and SWDEN_L
LADI	Input	FT7C960 interface - Latch Address In
LAEN	Input	FT7C960 interface - Local Address Enable
LEDI	Input	FT7C960 interface - Latch Enable Data In
LEDO	Input	FT7C960 interface - Latch Enable Data Out
ABEN_L	Input	FT7C960 interface - Address Bus Enable; enables data onto VME address bus for D64 cycles
LDS	Input	Local Data Select; used during mux-ed data VME transactions and INIT
LCIN_L	Input	Local address counter enable in
VCIN_L	Input	VME address counter enable in
BLT_L	Input	Block transfer enable
FC1	Input	Function code 1
MWB_L	Input	Module Wants Bus – local bus requesting VME
LADO	Input	Latch Address Out

See Page 8 For Amendments

Recommended Operating Conditions

Operating Conditions

Parameter	Description	Test Conditions	Value	Units
V_{CC}	Operating power supply		5 +/- 10%	V
T_J	Junction Temperature		-40 to 125	°C

DC Specifications—All Inputs

Parameter	Description	Test Conditions	Value	Units
V_{IH}	Minimum High-level Input Voltage		2.2	V
V_{IL}	Maximum Low-level Input Voltage		0.8	V
$I_{IH\text{-}max}$	Maximum High-level Input Current	V_{IN} = Vcc	10	µA
		V_{IN} = Vcc; 50K pulldown	250	µA
$I_{IH\text{-}min}$	Minimum High-level Input Current	V_{IN} = Vcc; 50K pulldown	20	µA
$I_{IL\text{-}max}$	Maximum Low-level Input Current	V_{IN} = GND	-10	µA
		V_{IN} = GND; 50K pullup	-250	µA
$I_{IL\text{-}min}$	Minimum Low-level Input Current	V_{IN} = GND; 50K pullup	-20	µA

DC Specifications—VME D Outputs

Parameter	Description	Test Conditions	Value	Units
V_{OH}	Minimum High-level Output Voltage	Vcc = Min, I_{OH} = -3ma	2.4	V
V_{OL}	Maximum Low-level Output Voltage	Vcc = Min, I_{OH} = 40ma	0.6	V

DC Specifications—VME A Outputs (D64 mode)

Parameter	Description	Test Conditions	Value	Units
V_{OH}	Minimum High-level Output Voltage	Vcc = Min, I_{OH} = -3ma	2.4	V
V_{OL}	Maximum Low-level Output Voltage	Vcc = Min, I_{OH} = 20ma	0.6	V

DC Specifications—All Other Outputs

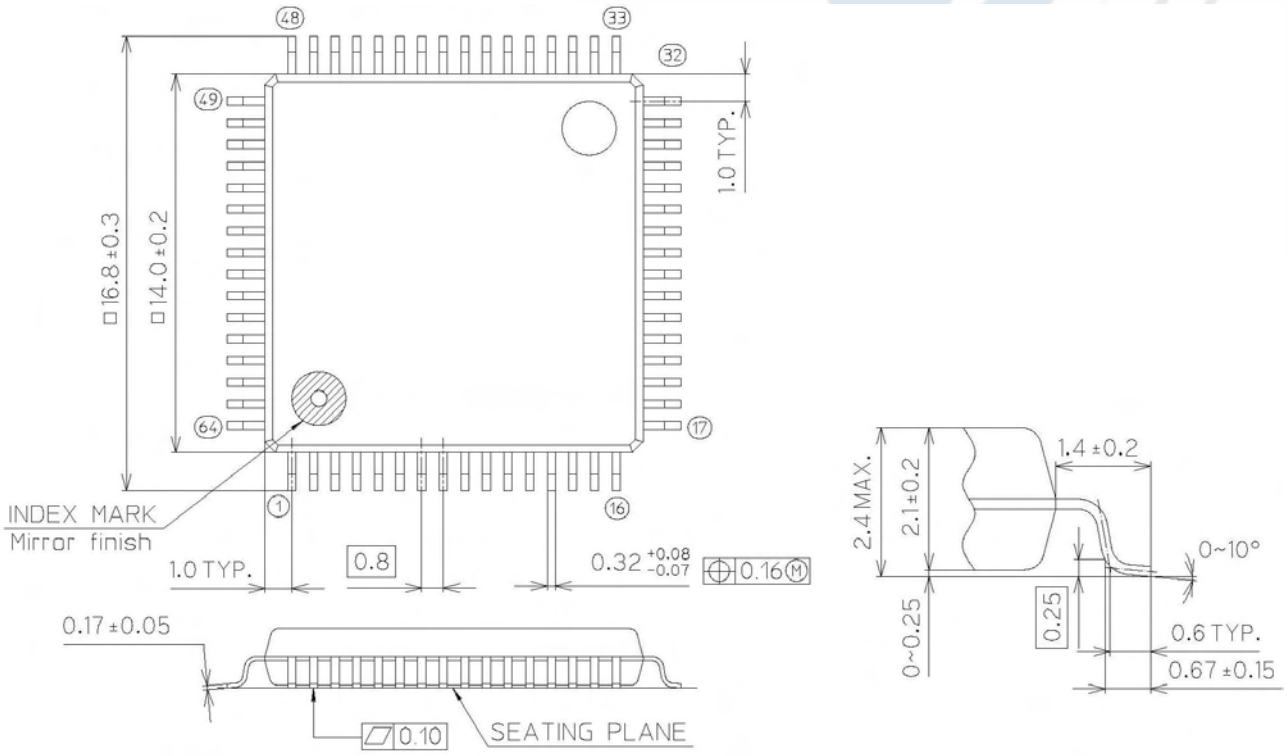
Parameter	Description	Test Conditions	Value	Units
V_{OH}	Minimum High-level Output Voltage	Vcc = Min, I_{OH} = -8ma	2.8	V
V_{OL}	Maximum Low-level Output Voltage	Vcc = Min, I_{OH} = 8ma	0.4	V

DC Specifications—All Tristate Outputs—Leakage currents

Parameter	Description	Test Conditions	Value	Units
$I_{OZH\text{-}max}$	Max high-level leakage current	V_{IN} = Vcc	10	µA
		V_{IN} = Vcc; 50K pulldown	250	µA
$I_{OZH\text{-}min}$	Minimum pulldown current	V_{IN} = Vcc; 50K pulldown	20	µA
$I_{OZL\text{-}max}$	Max low-level leakage current	V_{IN} = GND	-10	µA
		V_{IN} = GND; 50K pullup	-250	µA
$I_{OZL\text{-}min}$	Minimum pullup current	V_{IN} = GND; 50K pullup	-20	µA

Package Outline

PQFP "U" PKG



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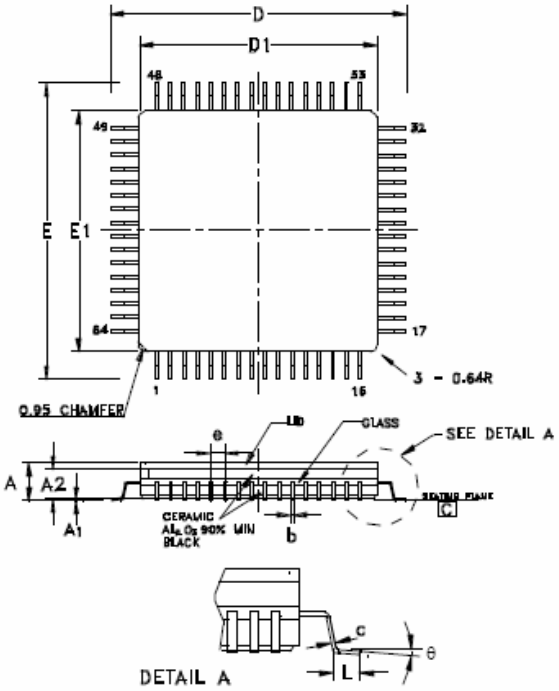
CerQuad Package CQFP="F" PKG

64 CERQUAD (Square) Marketing Outline Drawing



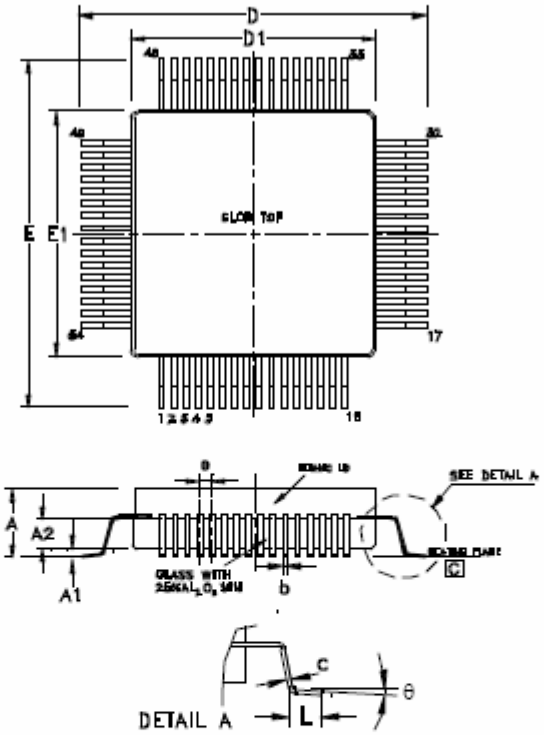
64 CERQUAD Square, (14x14x2.2mm), 2.6mm FP, CXI Part No. 1107

Symbol	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A			4.00			0.157
A1		0.50	TYP		0.020	
A2	1.92	2.22	2.52	0.076	0.087	0.099
b		0.35			0.014	
c		0.15			0.006	
D		16.60	BSC		0.654	
E		16.60	BSC		0.654	
e		0.80	BSC		0.031	
D1	13.82	13.97	14.12	0.544	0.550	0.556
E1	13.82	13.97	14.12	0.544	0.550	0.556
L		0.80	BSC		0.031	
θ	0°	5°	10°	0°	5°	10°

Controlling dimensions are in millimeters

CerQuad2 package C2QFP="F2" PKG

64 CERQUAD (Square) Marketing Outline Drawing



64 CERQUAD, (10.2x10.2x0.76mm), 2.25mm FP, CXI Part No. 1094

Symbol	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A			2.54			0.100
A1			0.18			0.007
A2	0.64	0.76	0.89	0.025	0.030	0.035
b		0.25	Typ		0.010	Typ
c	0.10	0.13	0.15	0.004	0.005	0.006
D		12.45			0.490	
E		12.45			0.490	
e		0.50	Typ		0.0197	Typ
D1	10.03	10.16	10.29	0.395	0.400	0.405
E1	10.03	10.16	10.29	0.395	0.400	0.405
L	0.38			0.015		
θ	0°		5°	0°		5°

Controlling dimensions are in inches

Revision NO	Amendment Made	Date	Signature
REV 1.0	Original Data Sheet	N/A	N/A
REV 2.0	Added 64 Cerquad Package	Mar 2007	M.S
REV 3.0	Reduced maximum operating temperature	Aug 2007	B.S
REV 4.0	**Changes to FT7C964(nowA) in ASIC Respin** **1:Clear Mask Register when loading Compare Register** When Strobe_L is asserted (LOW) and LDS=1, the compare register is loaded on the value with the LD bus. At this time, the mask register is cleared to ZERO **2:Load C3 Counter from S5 instead of LA bus** In the original version, the C3 counter was erroneously loaded with the value on the LA bus. In the respin, the C3 counter is loaded with a value from the S5 multiplexer. **This is an issue only in master operation.** **3:LA bus output enable is asserted when LAEN is TRUE** In the original version, the LA bus output enable was a function of FC1 and the internal BLT STATE LATCH, as well as LAEN. In the respin, the BLT STATE LATCH and FC1 terms are removed from the equation; LA bus output enable is a function only of LAEN. This is and issue only during master operations.	Nov 2007	B.S

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