FUJITSU

262144 BIT CMOS STATIC COLUMN DYNAMIC RAM

MB 81C466-10
MB 81C466-12
MB 81C466-15

March 1987
Edition 2.0

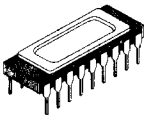
65,536 x 4 BIT CMOS STATIC COLUMN DYNAMIC RANDOM ACCESS MEMORY

The Fujitsu MB 81C466 is static column dynamic random access memory, SC-DRAM, which is organized as 65536 word by 4 bits. This SC-DRAM is designed for high speed, high performance applications such as main frame memory, buffer memory, and video memory, and for applications to battery backed-up systems where very low power dissipation and compact layout is required.

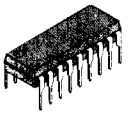
The advantage of SC-DRAM is achieving the static mode operation such as read, write and read-modify-write cycles in spite of dynamic RAM and the fast read and write operation can be performed by this mode.

The MB 81C466 is fabricated using silicon gate CMOS process. Since the CMOS circuit dissipates very small power, it can be easily used in battery backed-up application system such as hand held computer.
The MB 81C466 is pin compatible with Intel's 51C259.
All inputs and outputs are TTL compatible.

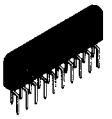
- 65536 x 4 SC-DRAM, 18-pin DIP/ 20-pin ZIP
- Silicon-gate, CMOS, single transistor cell
- Row Access Time (t_{RAC}),
  100 ns max. (MB 81C466-10)
  120 ns max. (MB 81C466-12)
  150 ns max. (MB 81C466-15)
- Random Cycle Time (t_{RC}),
  200 ns min. (MB 81C466-10)
  230 ns min. (MB 81C466-12)
  260 ns min. (MB 81C466-15)
- Address Access Time (t_{AA}),
  45 ns max. (MB 81C466-10)
  55 ns max. (MB 81C466-12)
  70 ns max. (MB 81C466-15)
- Static Mode Cycle Time (t_{SC}),
  50 ns min. (MB 81C466-10)
  60 ns min. (MB 81C466-12)
  75 ns min. (MB 81C466-15)
- Low Power Dissipation
  385 mW max. (MB 81C466-10)
  330 mW max. (MB 81C466-12)
  275 mW max. (MB 81C466-15)
  11 mW max. at standby with TTL level input
  1.65 mW max. at standby with CMOS level input
- Single 5V supply ±10% tolerance
- Internal write period control
- On chip latches for address and data inputs
- 32ms/256 refresh cycle
- $\overline{RAS}$-Only, $\overline{CAS}$-before-$\overline{RAS}$, and Hidden refresh capability
- Standard 18-pin ceramic (Metal seal) DIP (Suffix: -C)
- Standard 18-pin Plastic DIP (Suffix: -P)
- Standard 20-Pin Plastic ZIP (Suffix: -PSZ)



CERAMIC PACKAGE
DIP-18C-A01

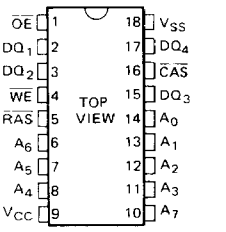


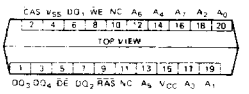
PLASTIC PACKAGE
DIP-18P-M01



PLASTIC PACKAGE
ZIP-20P-M01

PIN ASSIGNMENT





ABSOLUTE MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} relative to V_{SS}		V_{CC}	−1 to +7	V
Storage Temperature	Ceramic	T_{STG}	−55 to +150	°C
	Plastic		−55 to +125	
Power Dissipation		P_D	1.0	W
Short Circuit output current			50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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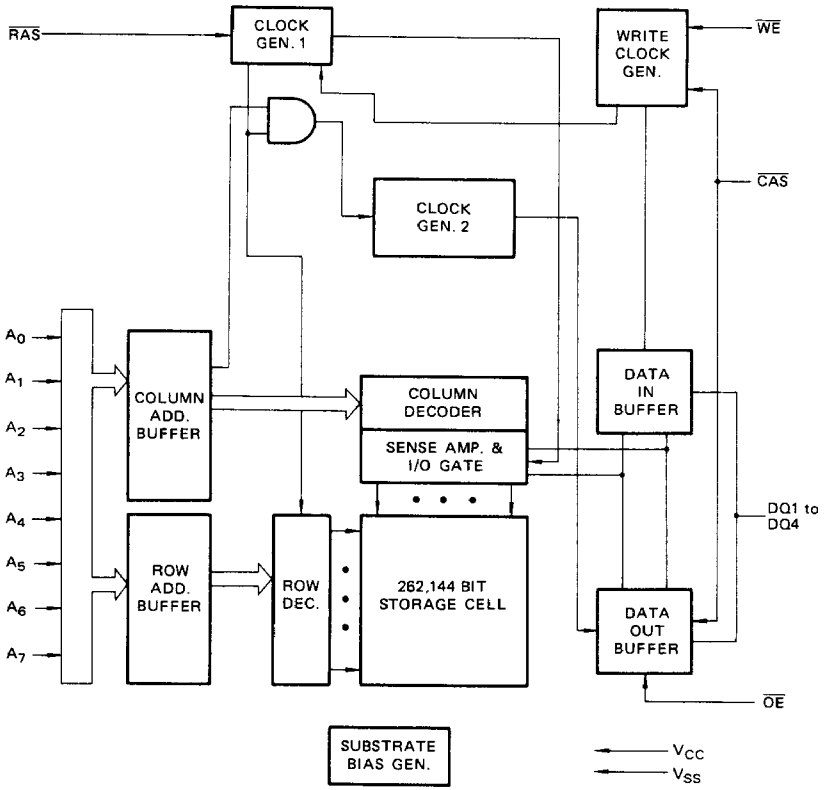
BLOCK DIAGRAM



CAPACITANCE (T_A = 0°C to +70°C, V_{CC} = 5V ± 10%, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A_0 to A_7	C_{IN1}		7	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{IN2}		10	pF
Input/Output Capacitance, DQ_1 to DQ_4	C_{IO}		7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V	0°C to +70°C
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IN}	-1.0		0.8	V	

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DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
OPERATING/REFRESH CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 81C466-10	I_{CC1}			70	mA
	MB 81C466-12				60	
	MB 81C466-15				50	
STANDBY CURRENT Standby Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})	TTL Level	I_{CC2}			2	mA
	CMOS Level				0.3	
STATIC MODE OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, $\overline{WE}$ or Address = cycling; t_{SC} = min)	MB 81C466-10	I_{CC3}			50	mA
	MB 81C466-12				40	
	MB 81C466-15				35	
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT* Average Power Supply Current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min)	MB 81C466-10	I_{CC4}			65	mA
	MB 81C466-12				55	
	MB 81C466-15				45	
INPUT LEAKAGE CURRENT, ALL INPUTS (V_{IN} = 0V to 5.5V, V_{CC} = 5V, V_{SS} = 0V, all other inputs not under test = 0V)		$I_{I(L)}$	-10		10	μA
INPUT/OUTPUT LEAKAGE CURRENT (Data is disabled, V_{OUT} = 0V to 5.5V)		$I_{DQ(L)}$	-10		10	μA
OUTPUT LEVEL, OUTPUT LOW VOLTAGE (I_{OL} = 4.2mA)		V_{OL}			0.4	V
OUTPUT LEVEL, OUTPUT HIGH VOLTAGE (I_{OH} = -5.0 mA)		V_{OH}	2.4			V

NOTE *; I_{CC} is depended on the output loading and cycle rate. The specified values are obtained with the output open.

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AC CHARACTERISTICS

(At Recommended operating conditions unless otherwise noted) NOTE 1, 2

Parameter NOTE	Symbol	MB 81C466-10		MB 81C466-12		MB 81C466-15		Unit
		Min	Max	Min	Max	Min	Max	
Time Between Refresh	t_{REF}		32		32		32	ms
Random Read/Write Cycle Time	t_{RC}	200		230		260		ns
Read-Modify-Write Cycle Time	t_{RWC}	270		315		360		ns
Access Time from $\overline{RAS}$ 3 5	t_{RAC}		100		120		150	ns
Access Time from $\overline{CAS}$ 5	t_{CAC}		25		30		35	ns
Output Buffer Turn off Delay Time	t_{OFF}	0	25	0	25	0	30	ns
Transition Time	t_T	3	50	3	50	3	50	ns
Column Address Access Time 5	t_{AA}		45		55		70	ns
Output Hold Time from Column Address Change	t_{AOH}	5		5		5		ns
Access Time from $\overline{WE}$ Precharge	t_{WPA}		25		30		35	ns
Access Time Relative to Last Write 6	t_{ALW}		90		110		140	ns
$\overline{RAS}$ Precharge Time	t_{RP}	90		100		100		ns
$\overline{RAS}$ Pulse Width	t_{RAS}	65	100000	75	100000	95	100000	ns
$\overline{RAS}$ Hold Time	t_{RSH}	25		30		35		ns
$\overline{CAS}$ Pulse Width (Read)	t_{CAS}	25	100000	30	100000	35	100000	ns
$\overline{CAS}$ Pulse Width (Write)	t_{CAS}	15	100000	20	100000	25	100000	ns
$\overline{CAS}$ Hold Time (Read)	t_{CSH}	100		120		150		ns
$\overline{CAS}$ Hold Time (Write)	t_{CSH}	80		95		115		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	75	25	90	30	115	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time	t_{CRS}	20		25		30		ns
Row Address Set Up Time	t_{ASR}	0		0		0		ns
Row Address Hold Time	t_{RAH}	15		15		20		ns
Column Address Set Up Time 7	t_{ASC}	0		0		0		ns
Column Address Hold Time 7	t_{CAH}	20		25		30		ns
$\overline{RAS}$ to Column Address Delay Time 8 9	t_{RAD}	20	55	20	65	25	80	ns
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	100		120		150		ns
Write Address Hold Time Referenced to $\overline{RAS}$	t_{AWR}	80		90		110		ns
Read Address to $\overline{RAS}$ Lead Time	t_{RAL}	45		55		70		ns
Column Address Hold Time Reference to $\overline{RAS}$ Rising Time 10	t_{AHR}	15		15		20		ns
Last Write to Column Address Delay Time 11 12	t_{LWAD}	20	45	20	55	25	70	ns
Column Address Hold Time Reference to Last Write	t_{AHLW}	90		110		140		ns

AC CHARACTERISTICS (Cont'd)

(At Recommended operating conditions unless otherwise noted) NOTE 1,2

Parameter NOTE	Symbol	MB 81C466-10		MB 81C466-12		MB 81C466-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Command Set Up Time Referenced to $\overline{CAS}$	t_{RCS}	0		0		0		ns
Read Command Hold Time Referenced to $\overline{RAS}$ 13	t_{RRH}	10		10		10		ns
Read Command Hold Time Referenced to $\overline{CAS}$ 13	t_{RCH}	0		0		0		ns
$\overline{WE}$ Pulse Width	t_{WP}	15		20		25		ns
$\overline{WE}$ Inactive Time	t_{WI}	15		20		25		ns
Write Command Hold Time	t_{WCH}	15		20		25		ns
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	25		30		35		ns
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	25		30		35		ns
$\overline{RAS}$ to $\overline{WE}$ Delay Time 14	t_{RWD}	125		150		185		ns
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	50		60		70		ns
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	70		85		100		ns
$\overline{RAS}$ to Second Write Delay Time	t_{RSWD}	105		125		155		ns
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	80		95		115		ns
$\overline{RAS}$ Precharge Time from Last Write	t_{RPLW}	135		155		165		ns
Write Set Up Time for Output Disable 14	t_{WS}	0		0		0		ns
Write Hold Time for Output Disable 14	t_{WH}	0		0		0		ns
D_{IN} Set Up Time	t_{DS}	0		0		0		ns
D_{IN} Hold Time	t_{DH}	20		25		30		ns
D_{IN} Hold Time Referenced to $\overline{RAS}$	t_{DHR}	80		90		110		ns
Access Time from $\overline{OE}$	t_{OEA}		25		30		35	ns
OE to Data In Delay Time	t_{OED}	20		25		30		ns
Output Buffer Turn off Delay Time from $\overline{OE}$	t_{OEZ}	0	20	0	25	0	30	ns
$\overline{OE}$ Hold Time Referenced to $\overline{RAS}$ 15	t_{OEHR}	20		20		20		ns
$\overline{OE}$ Hold Time Referenced to $\overline{CAS}$ 15	t_{OEHC}	20		20		20		ns
Refresh Set Up Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{FCS}	20		25		30		ns
Refresh Hold Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{FCH}	20		25		30		ns
$\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CPR}	20		25		30		ns
$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh cycles)	t_{RPC}	20		20		20		ns

AC CHARACTERISTICS (Cont'd)

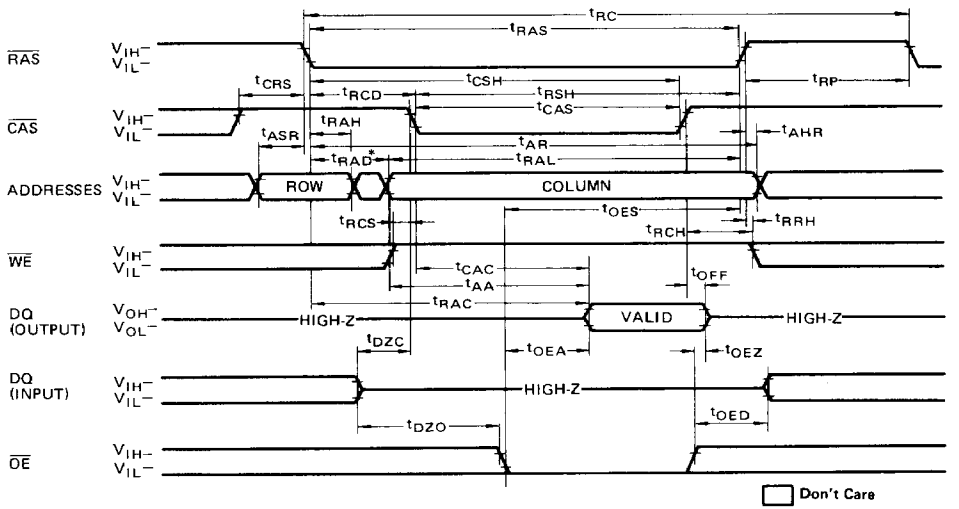
(At Recommended operating conditions unless otherwise noted) NOTE 1, 2

Parameter	NOTE	Symbol	MB 81C466-10		MB 81C466-12		MB 81C466-15		Unit
			Min	Max	Min	Max	Min	Max	
Static Mode Read/Write Cycle Time		t_{SC}	50		60		75		ns
Static Mode Read-Modify-Write Cycle Time		t_{SRWC}	120		145		180		ns
Static Mode $\overline{CAS}$ Precharge Time		t_{CP}	15		20		25		ns
$\overline{OE}$ to $\overline{RAS}$ Inactive Set Up Time		t_{OES}	25		30		35		ns
D_{IN} to $\overline{CAS}$ Delay Time	16	t_{DZC}	0		0		0		ns
D_{IN} to $\overline{OE}$ Delay Time	16	t_{DZO}	0		0		0		ns
Refresh Counter Test Cycle Time	17	t_{RTC}	465		550		645		ns
Refresh Counter Test $\overline{RAS}$ Pulse Width	17	t_{TRAS}	365	10000	440	10000	535	10000	ns
Refresh Counter Test $\overline{CAS}$ Precharge Time	17	t_{CPT}	50		60		70		ns
Refresh Counter Test $\overline{CAS}$ to Column Address Delay Time	17	t_{CADT}		100		120		150	ns
Refresh Counter Test Access Time from $\overline{CAS}$	17	t_{CACT}		135		165		205	ns
Refresh Counter Test $\overline{CAS}$ to $\overline{WE}$ Delay Time	17	t_{CWDT}	135		165		205		ns

NOTES:

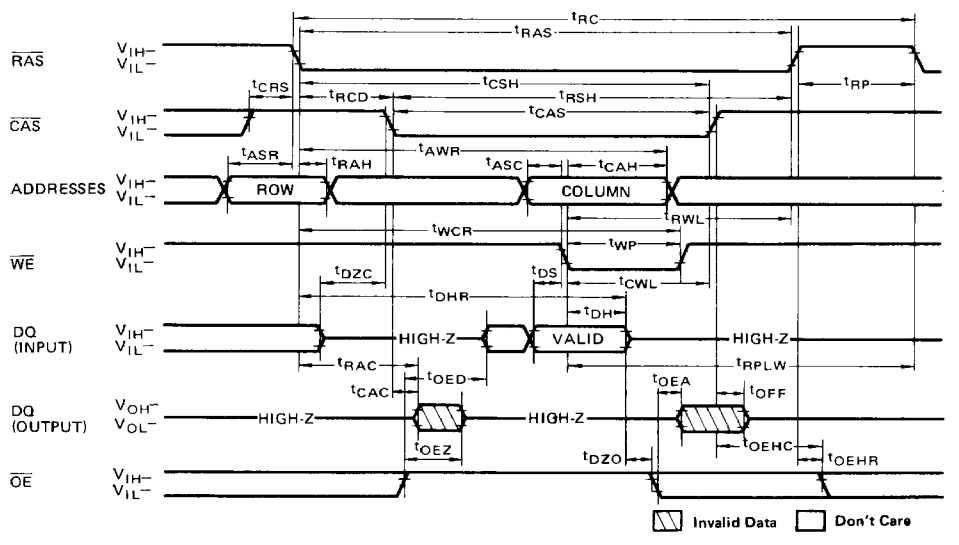
1. An Initial pause ($\overline{RAS}$=$\overline{CAS}$=V_{IH}) of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC characteristics assume t_T = 5ns, V_{IN} = 0V to 3V, V_{IH} = 2.4V, V_{IL} = 0.8, V_{OH} = 2.4V, and V_{OL} = 0.4V.
3. Assumes that $t_{RAD} \leqq t_{RAD}$ (max). If t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RAD} exceeds the value shown.
4. Assumes that $t_{RAD} \geqq t_{RAD}$ (max).
5. Measured with a load equivalent to 2 TTL loads and 100pF.
6. Assumes that $t_{LWAD} \leqq t_{LWAD}$ (max). If t_{LWAD} is greater than the maximum recommended value shown in this table, t_{ALW} will be increased by the amount that t_{LWAD} exceeds the value shown.
7. Write Cycle only.
8. Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
9. t_{RAD} (min) = t_{RAH} (min) + t_T (t_T = 5ns)
10. t_{AHR} is specified to latch column address by the rising edge of $\overline{RAS}$.
11. Operation within the t_{LWAD} (max) limit insures that t_{ALW} (max) can be met. t_{LWAD} (max) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, then access time is controlled by t_{AA}.
12. t_{LWAD} (min) = t_{CAH} (min) + t_T (t_T = 5ns).
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. t_{WS}, t_{WH}, and t_{RWD} are specified as a reference point only. If $t_{WS} \geqq t_{WS}$ (min) and $t_{WH} \geqq t_{WH}$ (min), the data output pin will remain High-Z state throughout entire cycle. It $t_{RWD} \geqq t_{RWD}$ (min). The data output will contain data read from the selected cell.
15. Either t_{OEHR} or t_{OEHC} is satisfied, output is disabled.
16. Either t_{DZC} or t_{DZO} must be satisfied.
17. $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle only.

Read Cycle



*; If $t_{RAD} \geqq t_{RAD}$ (max), access time is t_{AA}.

Write Cycle (WE Controlled)



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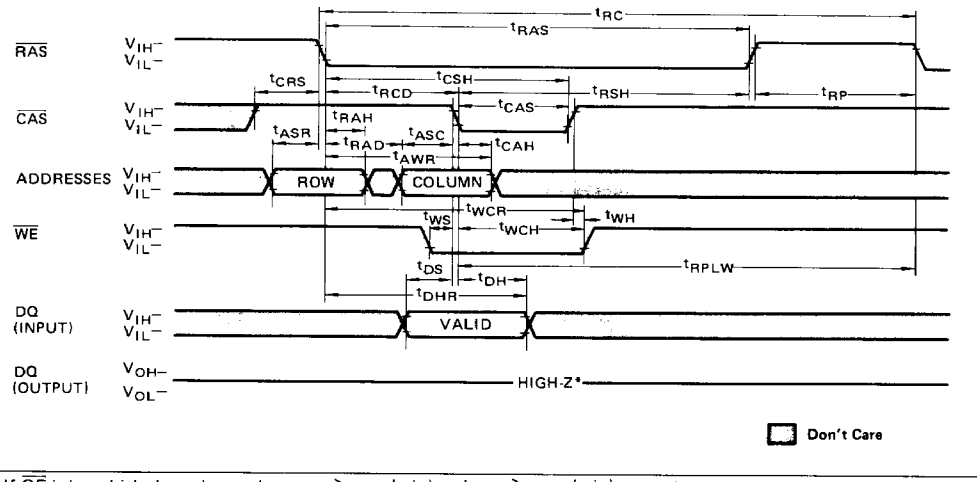
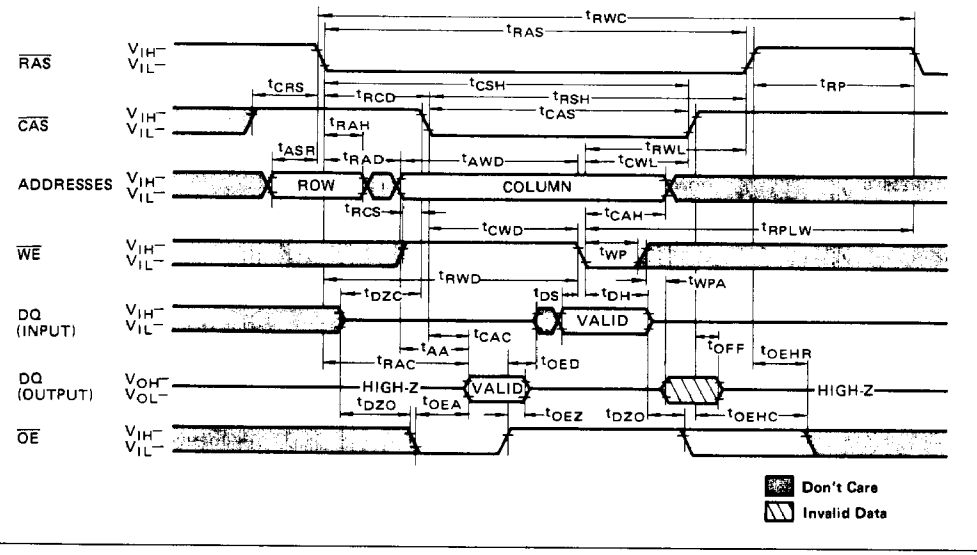
Write Cycle ($\overline{CAS}$ Controlled)
$\overline{OE}$; Don't Care



*; If $\overline{OE}$ is kept high through a cycle or $t_{WS} \geqq t_{WS}$ (min) and $t_{WH} \geqq t_{WH}$ (min) are met, DQ pins are kept high impedance state.

Read-Modify-Write Cycle



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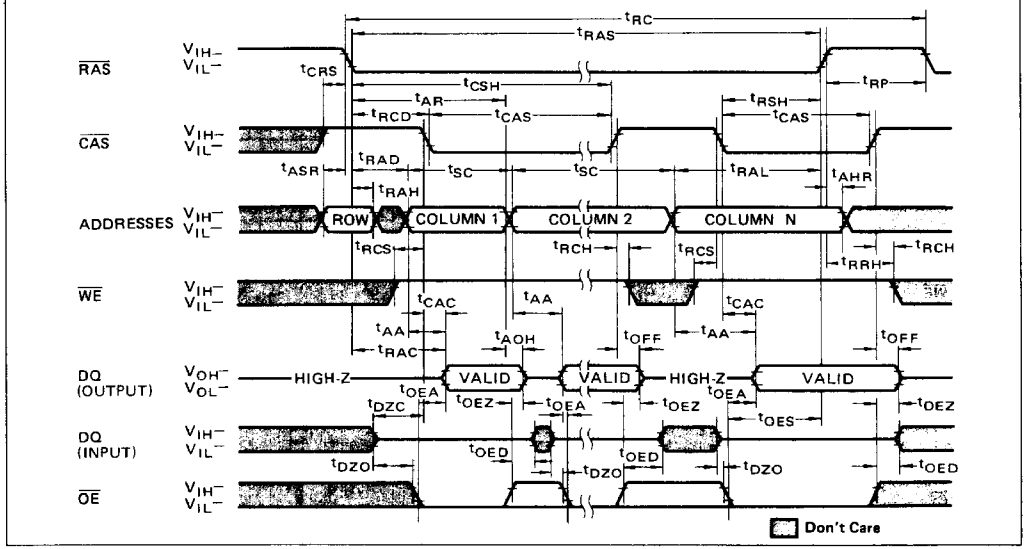
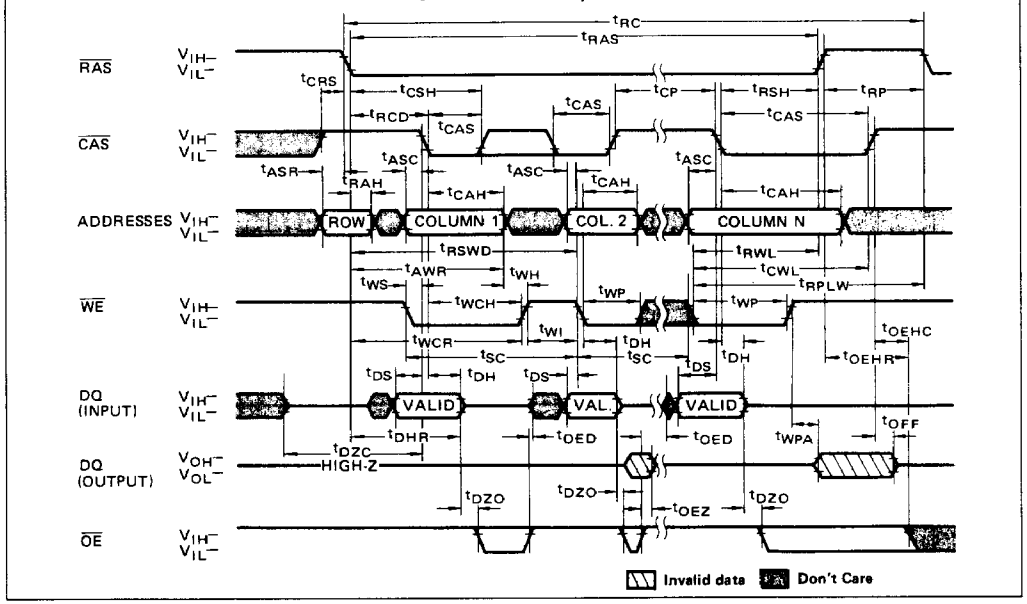
Static Mode Read Cycle



Static Mode Write Cycle



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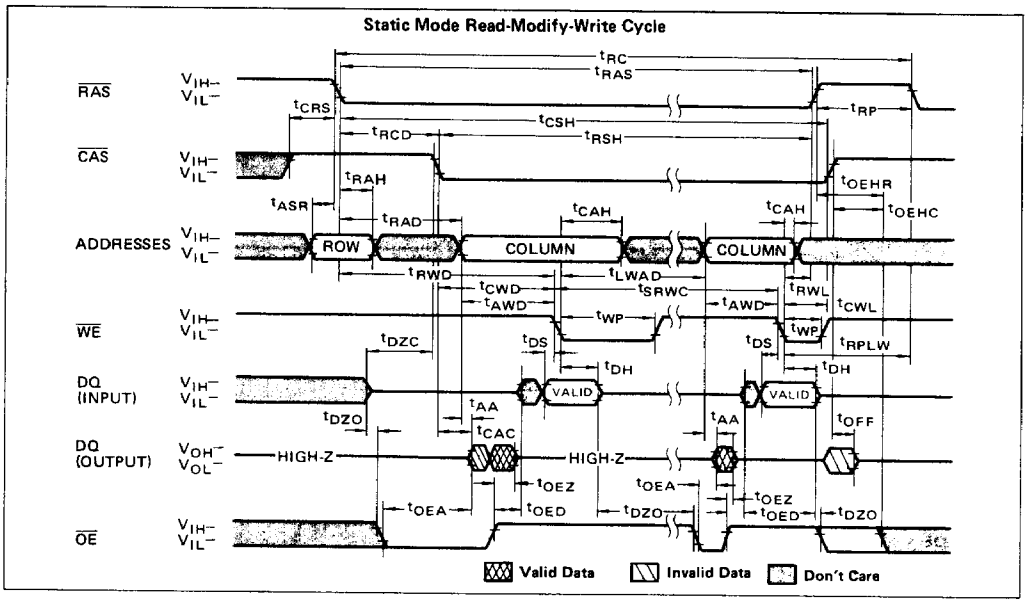
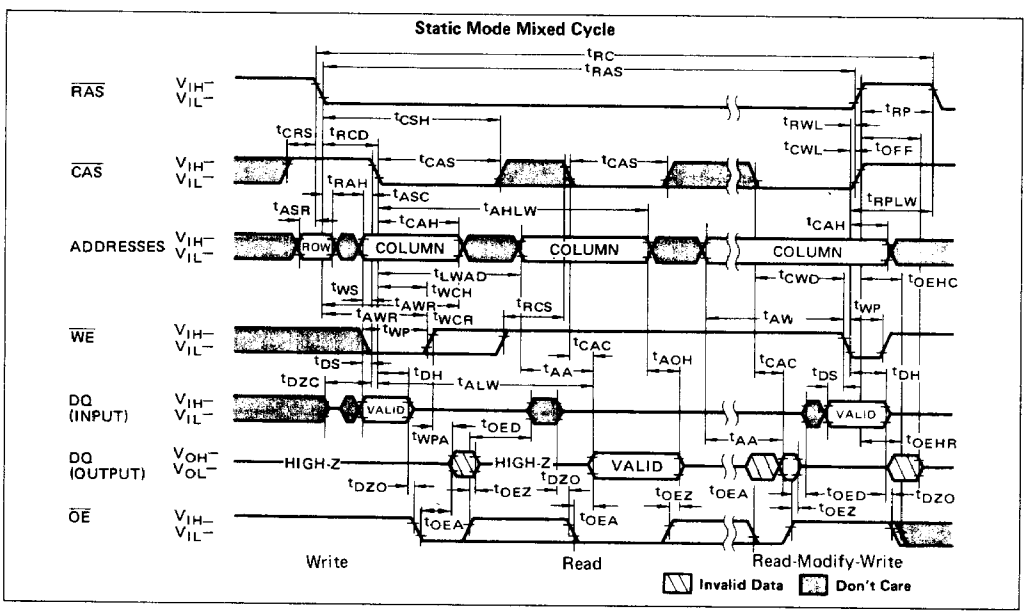

Static Mode Read-Modify-Write Cycle
RAS
CAS
ADDRESSES
WE
DQ (INPUT)
DQ (OUTPUT)
OE
ROW
COLUMN
COLUMN
VALID
VALID
HIGH-Z
HIGH-Z
Valid Data
Invalid Data
Don't Care


Static Mode Mixed Cycle
RAS
CAS
ADDRESSES
WE
DQ (INPUT)
DQ (OUTPUT)
OE
ROW
COLUMN
COLUMN
COLUMN
VALID
VALID
HIGH-Z
HIGH-Z
VALID
Write
Read
Read-Modify-Write
Invalid Data
Don't Care

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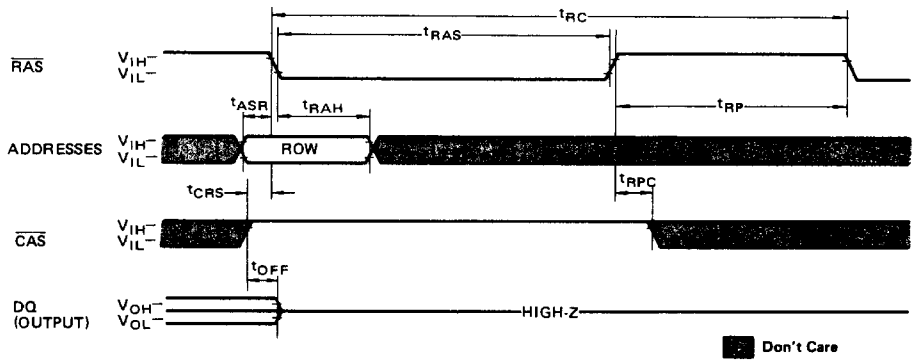
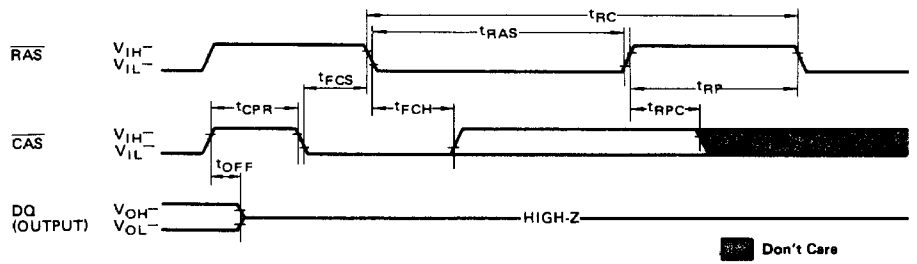
$\overline{RAS}$-Only Refresh Cycle
(Note; $\overline{WE}$, $\overline{OE}$, D_{IN} = Don't Care)



$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)
(Note; Address, $\overline{WE}$, $\overline{OE}$, D_{IN} = Don't Care)



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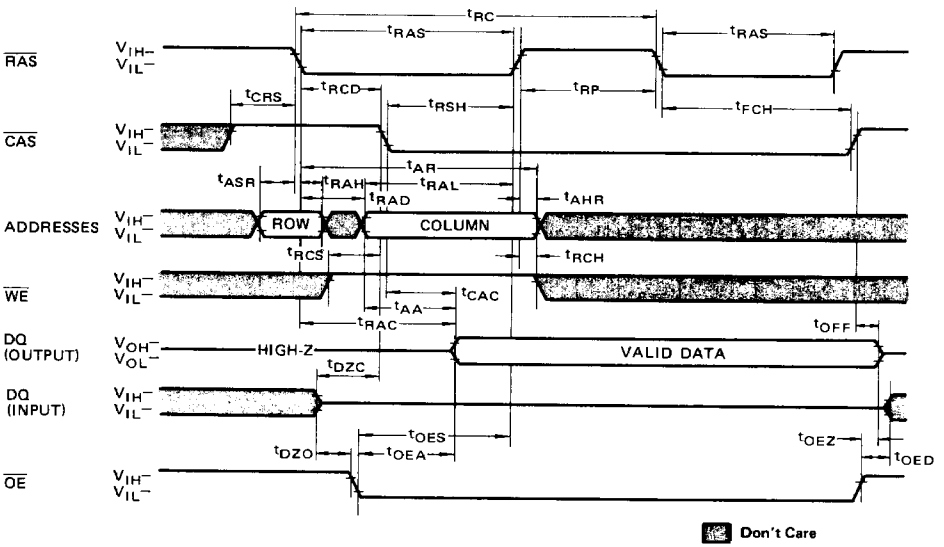
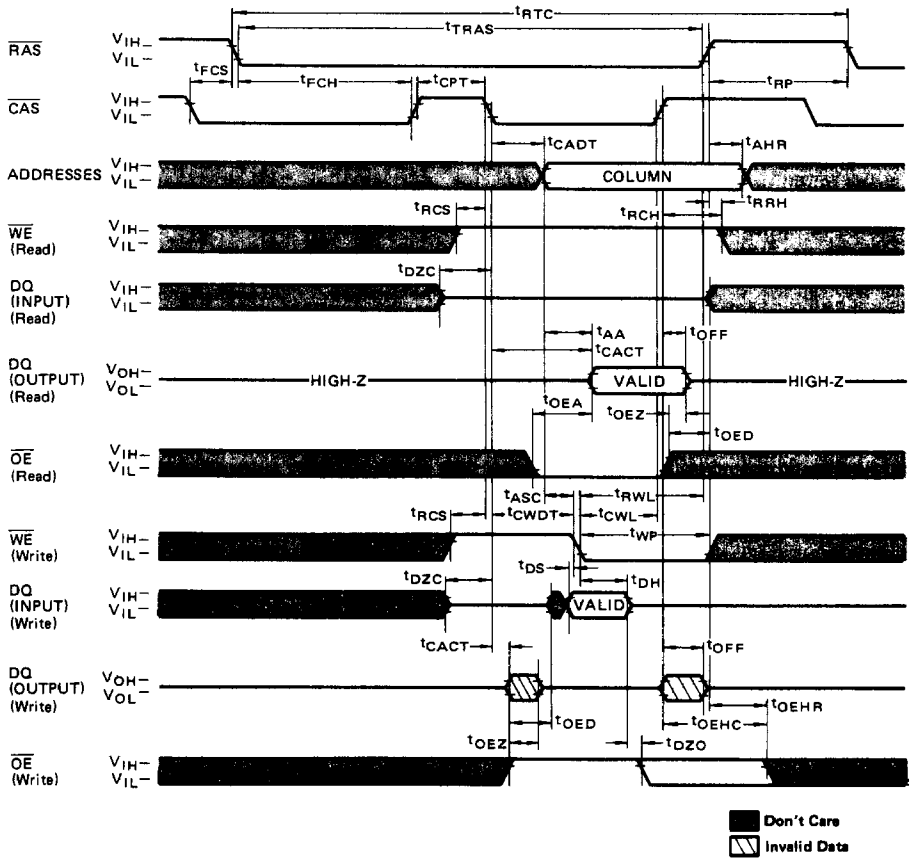
Hidden Refresh Cycle



$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle



DESCRIPTION

Address Inputs:
A total of sixteen binary input address bits are required to decode parallel 4 bits of the 262,144 storage cells within the MB 81C466. Eight row address bits are established on the address input pins (A_0 to A_7) and latched with the Row Address Strobe ($\overline{RAS}$). The eight column address bits are established on the address input pins (A_0 to A_7) after the Row Address Hold Time has been satisfied. In read cycle, the column addresses are not latched by the Column Address Strobe ($\overline{CAS}$), so the column address must be stable until the output becomes valid. In write cycle, the column addresses are latched by the later falling edge of $\overline{CAS}$ or $\overline{WE}$.

Write Enable:
Read or Write cycle is selected with the $\overline{WE}$ inputs. A high on $\overline{WE}$ selects read cycle and low selects write cycle. The write operation is asserted on the later falling edge of $\overline{CAS}$ or $\overline{WE}$ (Both $\overline{CAS}$ and $\overline{WE}$ are low). The time period of the write operation is determined by internal circuit, thus the next write operation will be inhibited during the write operation.

Data Pins:
Data Inputs;
Data are written into the MB 81C466 during write or read-modify-write cycle. The input data is strobed and latched by the later falling edge of $\overline{CAS}$ or $\overline{WE}$.

Data Output:
The output buffer is three state TTL compatible with a fan out of two standard TTL loads. Data out has the same porality as data in. The output is in high impedance state until $\overline{CAS}$ is brought low. In a read cycle, the access time is determined by the following conditions:
1. t_{RAC} from the falling edge of $\overline{RAS}$.
2. t_{AA} from the column address inputs.
3. t_{CAC} from the falling edge of $\overline{CAS}$.
4. t_{OEA} from the falling edge of $\overline{OE}$.

When both t_{RCD} and t_{RAD} satisfy their maximum limits, $t_{RAC}=t_{RCD}+t_{CAC}$ or $t_{RAC}=t_{RAD}+t_{AA}$.
Data output remains valid while the column address inputs are kept constant. However, when either $\overline{CAS}$ or $\overline{OE}$ goes high, the output returns to a high impedance state. In the static write cycle ($\overline{CAS}$ controlled), if both $t_{WS} \geqq t_{WS}$(min) and $t_{WH} \geqq t_{WH}$(min) are met, data pins are input mode regardless of the state of $\overline{OE}$.

Output Enable:
The $\overline{OE}$ controls the impedance of the output buffers. In the high state on $\overline{OE}$, the output buffers are high impedance state. In the low state on $\overline{OE}$, the output buffers are low impedance state. In the write cycle ($\overline{WE}$ controlled), the $\overline{OE}$ must be high before the data applied to DQ pins. When $\overline{WE}$ controlled write cycles is not used, $\overline{OE}$ can be low throughout the operation.

Static Mode:
The static mode operation allows continuous read, write, or read-modify-write cycle within a row by applying new column address. In the static mode, $\overline{CAS}$ can be kept low throughout static mode operation. The following four cycles are allowed in the static mode.
1. Static mode read cycle,
   In a static mode read cycle, the access time is t_{RAC} from the falling edge of $\overline{RAS}$ or t_{AA} from the column address input or t_{OEA} from the falling edge of $\overline{OE}$. The data remains valid for a time t_{AOH} after the column address is changed.
2. Static mode write cycle;
   In a static mode write cycle, the data is written into the cell triggered by the later falling edge of $\overline{CAS}$ or $\overline{WE}$. If both t_{WS} and t_{WH} are greater than their minimum limits, the data output pin is kept high impedance state through the static mode write cycle. The $\overline{OE}$ must be high before the data are applied to DQ pins.
3. Static mode read-modify-write cycle;
   In the static mode read-modify-write cycle, $\overline{WE}$ goes low after t_{AWD} from the column address inputs and t_{CWD} from the falling edge of $\overline{CAS}$. The data and column address inputs are strobed and latched by the falling edge of $\overline{WE}$. The $\overline{OE}$ must be high before the data are applied to DQ pins.
4. Static mode mixed cycle;
   In the static mode, read, write, and read-modify-write cycles can be mixed in any order.

In the next read cycle of static mode write cycle or read-modify-write cycle, the access time is determined by the following conditions.
1. t_{ALW} from the falling edge of $\overline{WE}$ at previous write cycle.
2. t_{AA} from the column address inputs.
3. t_{WPA} from the rising edge of $\overline{WE}$ at the read cycle.
4. t_{CAC} from the falling edge of $\overline{CAS}$.
5. t_{OEA} from the falling edge of $\overline{OE}$.

Refresh:
Refresh of dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row addresses (A_0 to A_7) at least every 4ms.
The MB 81C466 offers the following three types of refresh.
1. $\overline{RAS}$ only refresh;
   The $\overline{RAS}$-only refresh avoids any outputs during refresh because the outputs buffers are high impedance state due to $\overline{CAS}$-high. Strobing of each 256 row address (A_0 to A_7) with $\overline{RAS}$ will cause all bits in each row to be refreshed.
2. $\overline{CAS}$-before-$\overline{RAS}$ refresh;
   $\overline{CAS}$-before-$\overline{RAS}$ refreshing available on the MB 81C466 offers an alternate refresh method. If $\overline{CAS}$ is held low for the specified period (t_{FCS}) before $\overline{RAS}$ goes low, on chip refresh control clock generator and the internal refresh address counter are enabled, and an internal refresh operation is executed. After the refresh operation, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh.
3. Hidden refresh;
   A hidden refresh cycle will be executed while maintaining latest valid data at the output pin by extending the $\overline{CAS}$ low time. For the MB 81C466, a hidden refresh cycle is $\overline{CAS}$-before-$\overline{RAS}$ refresh. The internal refresh address counter provides the refresh address, as in a normal $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter Test:
A special timing sequence using $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter test cycle provides a convenient method of verifying the function of $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh activated circuitry. After the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle, if $\overline{\text{CAS}}$ goes to high and goes to low again while $\overline{\text{RAS}}$ is held low, the read and read-modify-write cycles are enabled according to the state of $\overline{\text{WE}}$. This is shown in the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ counter test cycle timing diagram. A memory cell address, consisting of a row address (8 bits) and a column address (8 bits), to be accessed is shown below.

ROW ADDRESS – All bits A_0 to A_7 are provided by the refresh counter.

COLUMN ADDRESS – All the bits A_0 to A_7 are provided by externally after t_{CADT}.

The recommended procedure of $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter test is shown below. The timing of $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter test cycle should be used.

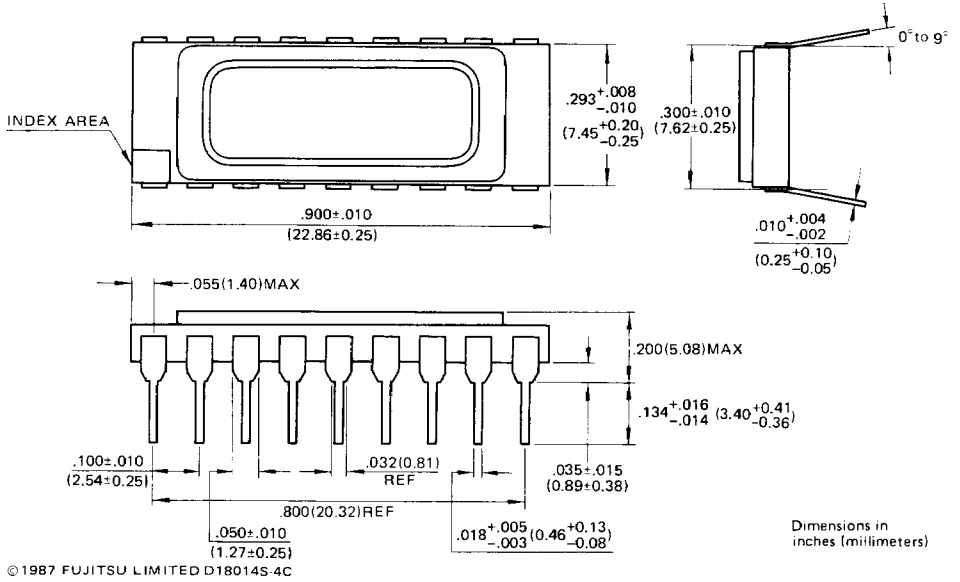
1) Initialize the internal refresh address counter by using eight $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycles.
2) Throughout the test, use the same column address.
3) Using a write cycle, write 0s to all 256 row addresses.
4) Using $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter test cycle in read-modify-write mode, read the 0 written in step 3), and simultaneously write a 1 to the same cell. This step is repeated 256 row address generated by internal refresh address counter.
5) Using a normal read cycle, read back the 1s written in step 4), from all 256 locations.
6) Complement the test pattern and repeat step 3), 4), and 5).

2

PACKAGE DIMENSIONS

(Suffix: -C)

18-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-18C-A01)

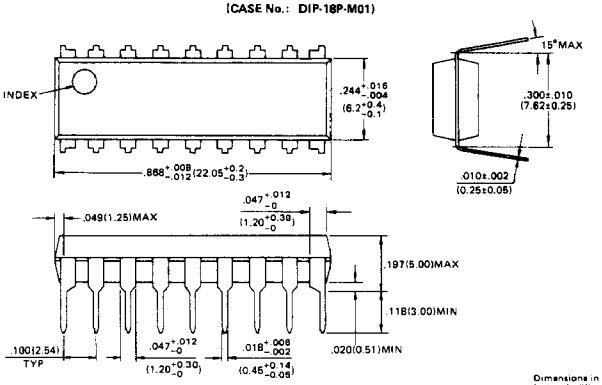


2

PACKAGE DIMENSIONS

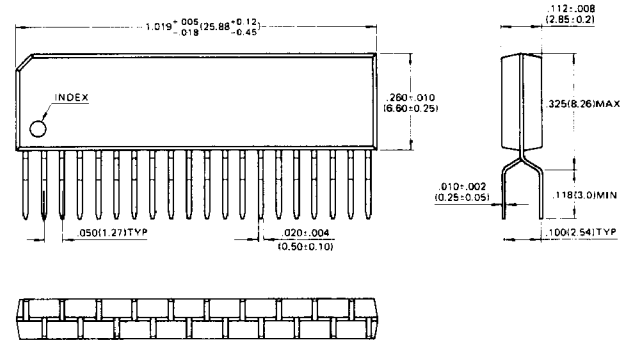
(Suffix: -P) (Suffix: -PSZ)

18-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-18P-M01)



Dimensions in inches (millimeters)

20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE
(CASE NO.: ZIP-20P-M01)



Dimensions in inches (millimeters)