Dual 2-Wide 2-3-Input "OR-AND/OR-AND-INVERT" Gate

Military 10H517

ELECTRICALLY TESTED PER:
MPG 10H517

2

The 10H517 is a general purpose logic element designed for use in data control, such as digital multiplexing or data distribution. Pin 9 is common to both gates. This MECL 10H part is a functional pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

- Propagation Delay, 1.0 ns Typical
- 160 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

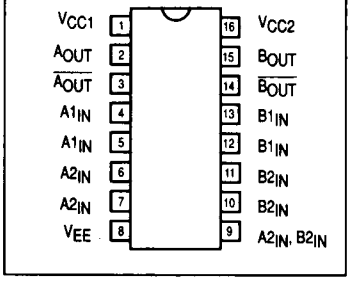
AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: 10H517/BXAJC
X = CASE OUTLINE AS FOLLOWS:

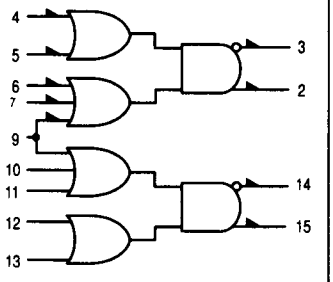
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

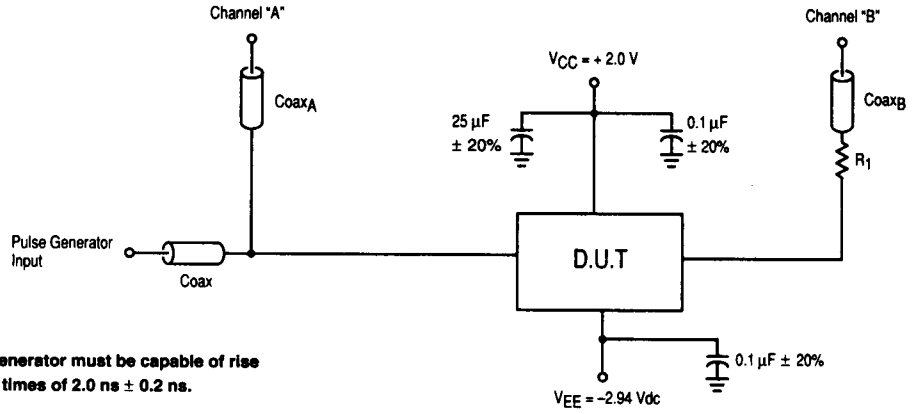
	PIN ASSIGNMENTS			
FUNCTION	**DIL**	**FLATS**	**LCC**	**BURN-IN (CONDITION C)**
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
$\overline{A_{OUT}}$	3	7	4	51 Ω to V_{TT}
$A1_{IN}$	4	8	5	OPEN
$A1_{IN}$	5	9	7	OPEN
$A2_{IN}$	6	10	8	OPEN
$A2_{IN}$	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
$A2_{IN}$, $B2_{IN}$	9	13	12	OPEN
$B2_{IN}$	10	14	13	OPEN
$B2_{IN}$	11	15	14	OPEN
$B1_{IN}$	12	16	15	OPEN
$B1_{IN}$	13	1	17	OPEN
$\overline{B_{OUT}}$	14	2	18	51 Ω to V_{TT}
B_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND



LOGIC DIAGRAM



BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN



Pulse generator must be capable of rise and fall times of 2.0 ns ± 0.2 ns.

NOTES
1. Length of $Coax_A$ and $Coax_B$ should be equal for equal time delay.
2. Unused outputs should be loaded 100 Ω to ground.
3. 2:1 divider may be used.
4. $t_r = t_f$ = 1.0 ns ± 0.1 ns measured at (20% - 80%).
5. $P_W \geq$ 20 ns.
6. P_{RF} = 1.00 MHz.
7. R_1 = 50 Ω resistor in series with 50 Ω coax constituting the 100 Ω load.

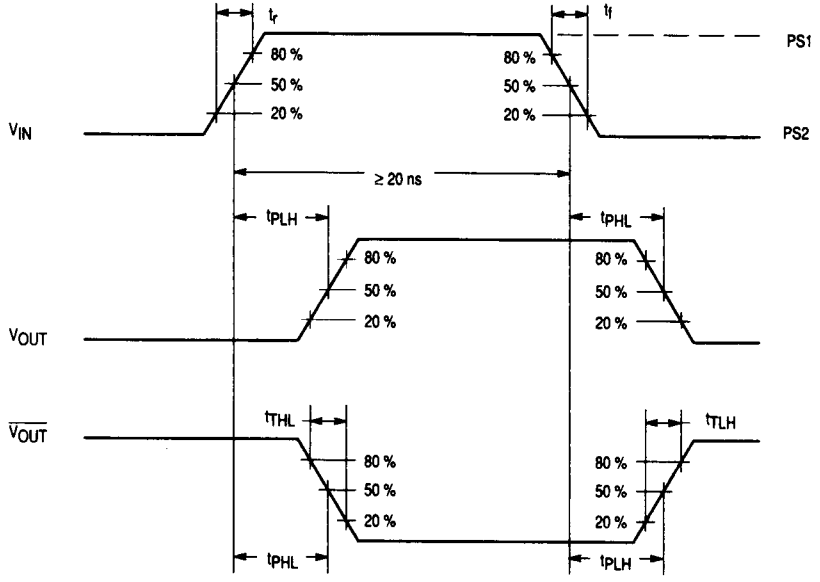


Figure 1. Switching Test Circuit and Waveforms

10H517
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.13	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.63	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125°C		- 55°C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{EE1}	V_{EE2}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	4 - 7 9 - 13				8		1, 16	2, 3, 14, 15
V_{OL}	Low Output Voltage	-1.95	-1.58	-1.95	-1.565	-1.95	-1.61	V	4 - 7 9 - 13				8		1, 16	2, 3, 14, 15
V_{OHA}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	4 - 7 9 - 13		4 - 7 9 - 13	4 - 7 9 - 13	8	8	1, 16	2, 3, 14, 15
V_{OLA}	Low Output Voltage	-1.95	-1.58	-1.95	-1.565	-1.95	-1.61	V	4 - 7 9 - 13		4 - 7 9 - 13	4 - 7 9 - 13	8	8	1, 16	2, 3, 14, 15
I_{EE}	Power Supply Current	-26		-29		-29		mA					8		1, 16	8
I_{IH1}	Input Current High		320		510		510	µA	4, 5, 12, 13				8		1, 16	4, 5, 12, 13
I_{IH2}	Input Current High		365		590		590	µA	6, 7 10, 11				8		1, 16	6, 7, 10, 11
I_{IH3}	Input Current High		460		755		755	µA	9				8		1, 16	9
I_{IL}	Input Current Low	0.3		0.3		0.5		µA		4 - 7 9 - 13			8		1, 16	7, 9 - 13

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Test Temperature	Test Voltage Values (Volts)								
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T_A = 125 °C	-0.63	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P.U.T.
t_{TLH}	Rise Time	0.5	1.6	0.5	1.7	0.5	1.5	ns	4, 6, 11 12	2, 14, 15	1, 16	8	4, 6 11, 12	2, 3, 14, 15
t_{THL}	Fall Time	0.5	1.6	0.5	1.7	0.5	1.5	ns	4, 6, 11 12	2, 14, 15	1, 16	8	4, 6 11, 12	2, 3, 14, 15
t_{PHL}	Propagation Delay High to Low	0.54	1.62	0.6	1.8	0.54	1.62	ns	4, 6, 11 12	2, 14, 15	1, 16	8	4, 6 11, 12	2, 3, 14, 15
t_{PLH}	Propagation Delay Low to High	0.54	1.62	0.6	1.8	0.54	1.62	ns	4, 6, 11 12	2, 14, 15	1, 16	8	4, 6 11, 12	2, 3, 14, 15