# Datasheet

December 1997 Version 1.1

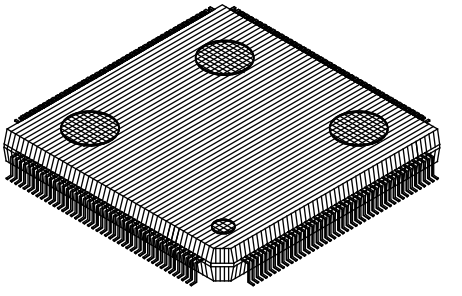
# MB86681

## ATM Switch Element (SRE-L)

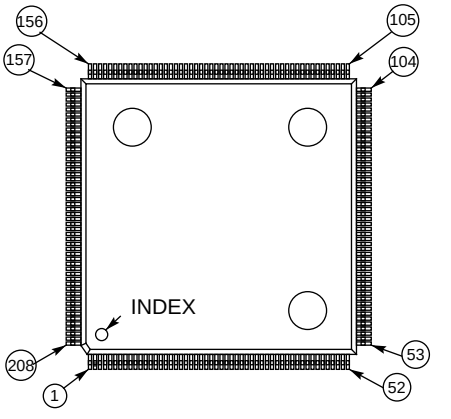
FML/NPD/SRE-L/DS/1223

The FUJITSU MB86681 is a Self-Routing switch Element (SRE-L) for use in ATM switch fabrics. It is ideally suited to applications in a variety of customer premises equipment such as ATM hubs and network access controllers. The device is organized as a 4 x 4 switch with separate input and output ports for matrix expansion. The main features of the device are listed below:-

**PLASTIC PACKAGE**
**SQFP208**



**PIN ASSIGNMENT**




### Features

- Highly integrated 4x4 structure.
- Active matrix expansion ports for row and column interconnect.
- Selectable high and low priority output queues.
- Output port buffer capacity of 146 cells, which can be divided into a 121 cell low priority queue and a 25 cell high priority queue.
- Multicast support.
- Selective cell discard based on CLP bit and selectable queue level.
- Selectable Explicit Forward Congestion Indication (EFCI) function.
- Selectable Per VC EFCI marking.
- Selectable per Output queue Vertical Flow Control (VFC).
- Early Packet Discard (EPD) notification capability.
- Flexible tag processing to allow a variety of switch fabric architectures to be realized.
- All input / output ports operate at up to 40MHz using an 8-bit data format.
- JTAG pins compatible with IEEE1149.1 are provided.
- Fabricated in sub-micron CMOS technology incorporating a 5V CMOS compatible I/O with a low power 3.3V logic core.

## TABLE OF CONTENTS

## TABLE OF CONTENTS (Continued)

## APPENDICES



## LIST OF FIGURES

## LIST OF FIGURES (Continued)



## LIST OF TABLES



# 1 Introduction

## 1.1 Outline

The Fujitsu MB86681 is a Self-Routing ATM cell switch Element (SRE-L) which can be used as a basic building block for a variety of 155 to 300Mb/s ATM switch fabrics.

The device provides 4 output data queues, one for each output port and each with an aggregate storage capacity of 146 cells per output port. A 24 bit routing tag is used to decide into which output queue a particular cell will be loaded.

Each output queue is divided into a high and low priority section. A control bit in the routing tag determines the cell priority. High priority cells will always be forwarded in preference to low priority cells. Hence cells using the high priority queues will suffer less queueing delay and will have a lower cell loss rate than cells using the low priority queues (assuming that high priority traffic only forms a small portion of total traffic).

The switch element includes four expansion inputs, which are provided to facilitate easy expansion in the form of a matrix. Cells received via the expansion inputs are directed into the attached output data queue.

## 1.2 Matrix Configuration

Various interconnection topologies can be applied to the SRE-L. However, the device is ideally suited to interconnection in the form of a matrix. In this case the SRE-L provides re-timed active outputs which allow direct connection to nearest neighbours. This eliminates the need for passive buses and reduces device interconnect problems at the board level. A matrix architecture is illustrated in Figure 1.

The number of switch elements required for an N x N switch is proportional to $N^2$ and hence is only appropriate for relatively small switch fabrics (e.g. 32 X 32). For larger switches, individual matrices can be interconnected using a multi-path delta arrangement.

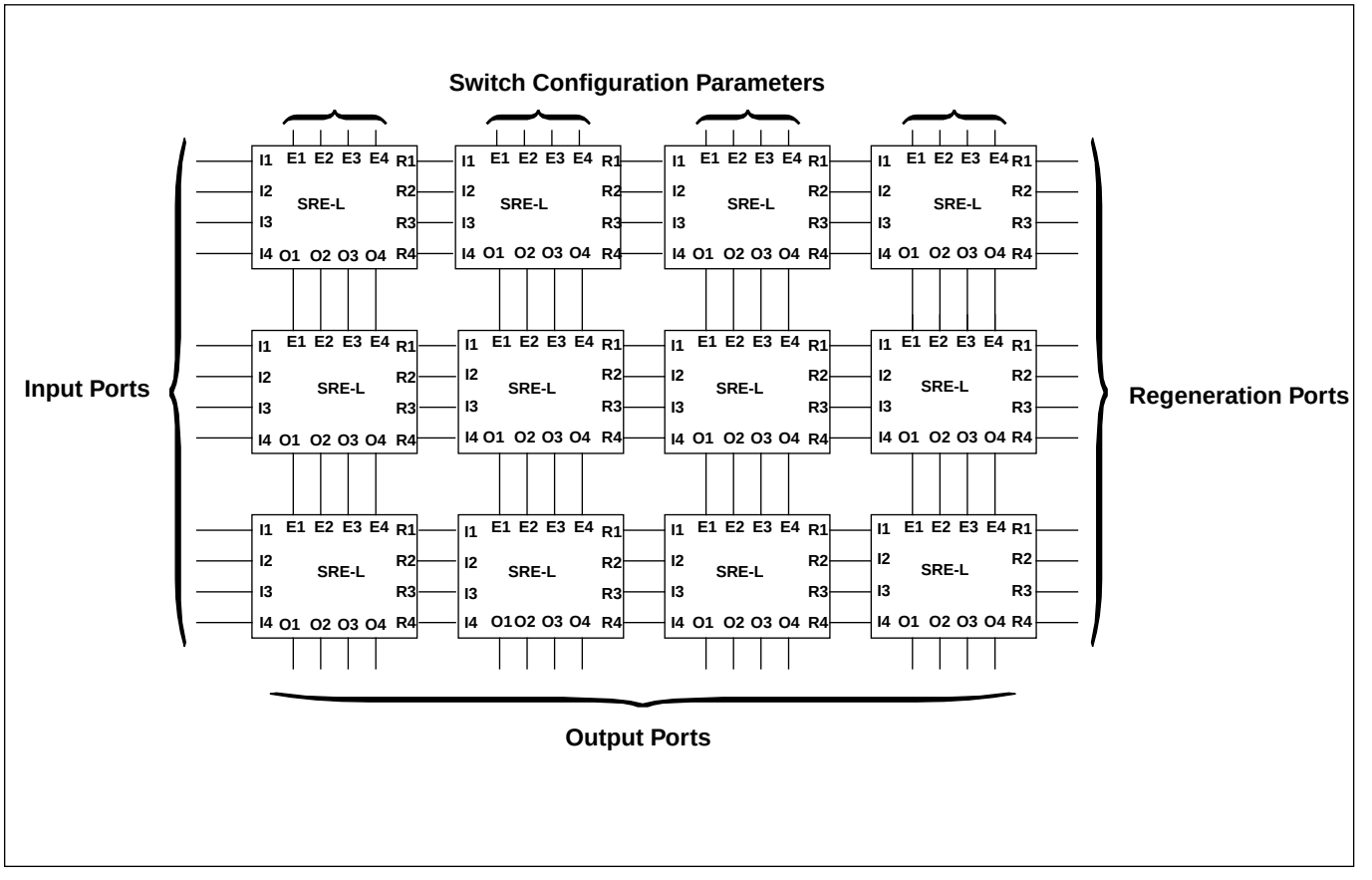



**Figure 1 SRE-L Matrix Interconnect**

## 1.3 Delta Configuration

Larger switches may be realized by connecting SRE-L matrices into switch topologies similar to the two stage delta configuration as illustrated in Figure 2.

Each switch element allows a selectable region of the tag field to be used for address filtering.
This is illustrated in Figure 2 where SRE-L elements in stages 1 and 2 are configured with different Address Location Fields. Consequently, stage 2, SRE-L switch elements are configured to examine a different portion of the ATM cell's routing tag from that examined by SRE-L elements in stage 1.

As a consequence of the selectable address field multi-path, delta switches can be constructed without the need for intermediate address translation/tag generation.

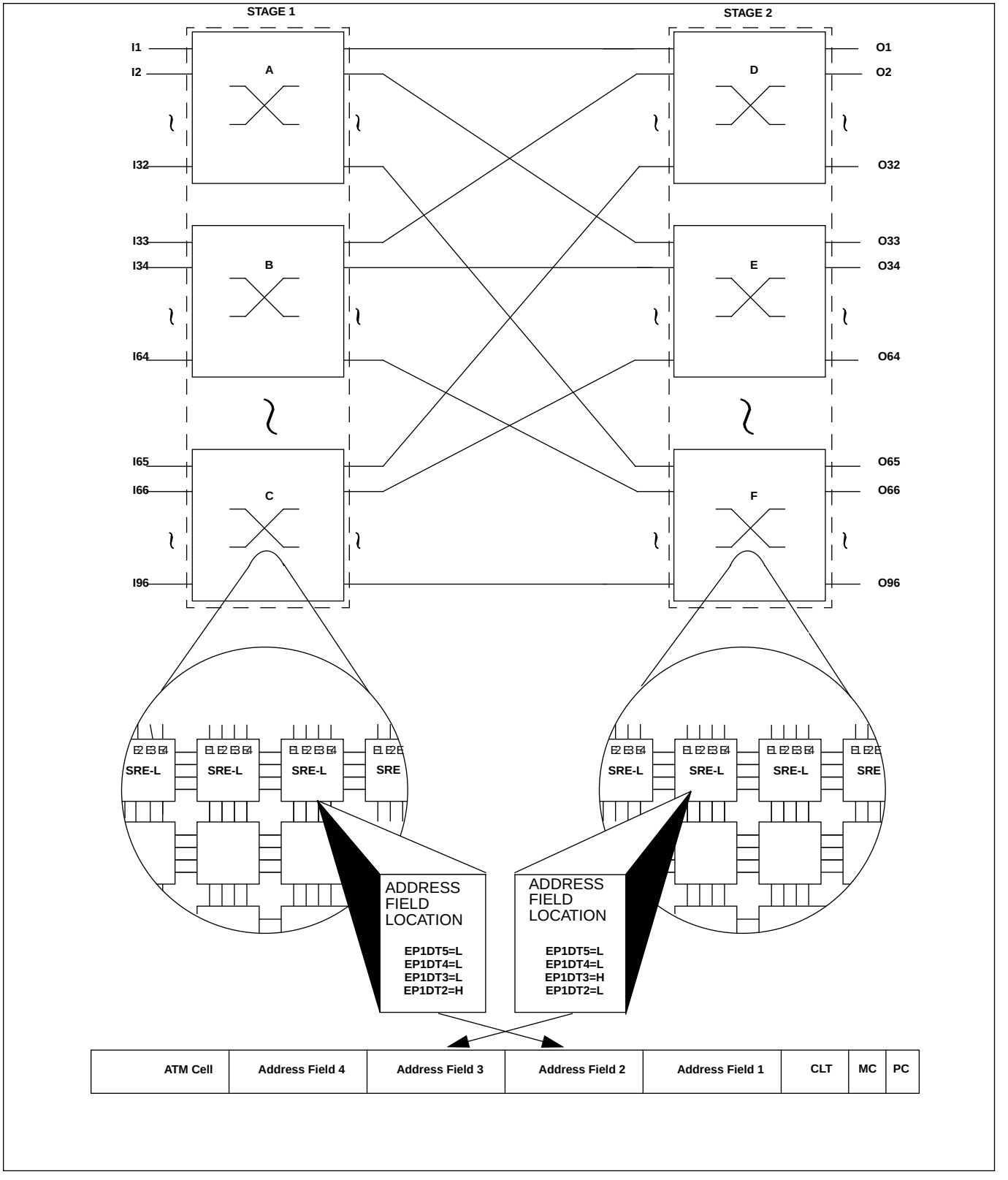



**Figure 2 Delta Switch Configuration**

# 2 External Interfaces

## 2.1 Logical Outline

A logical view of the MB86681's external pins is illustrated in Figure 3 and a physical pin assignment is shown in Appendix D.

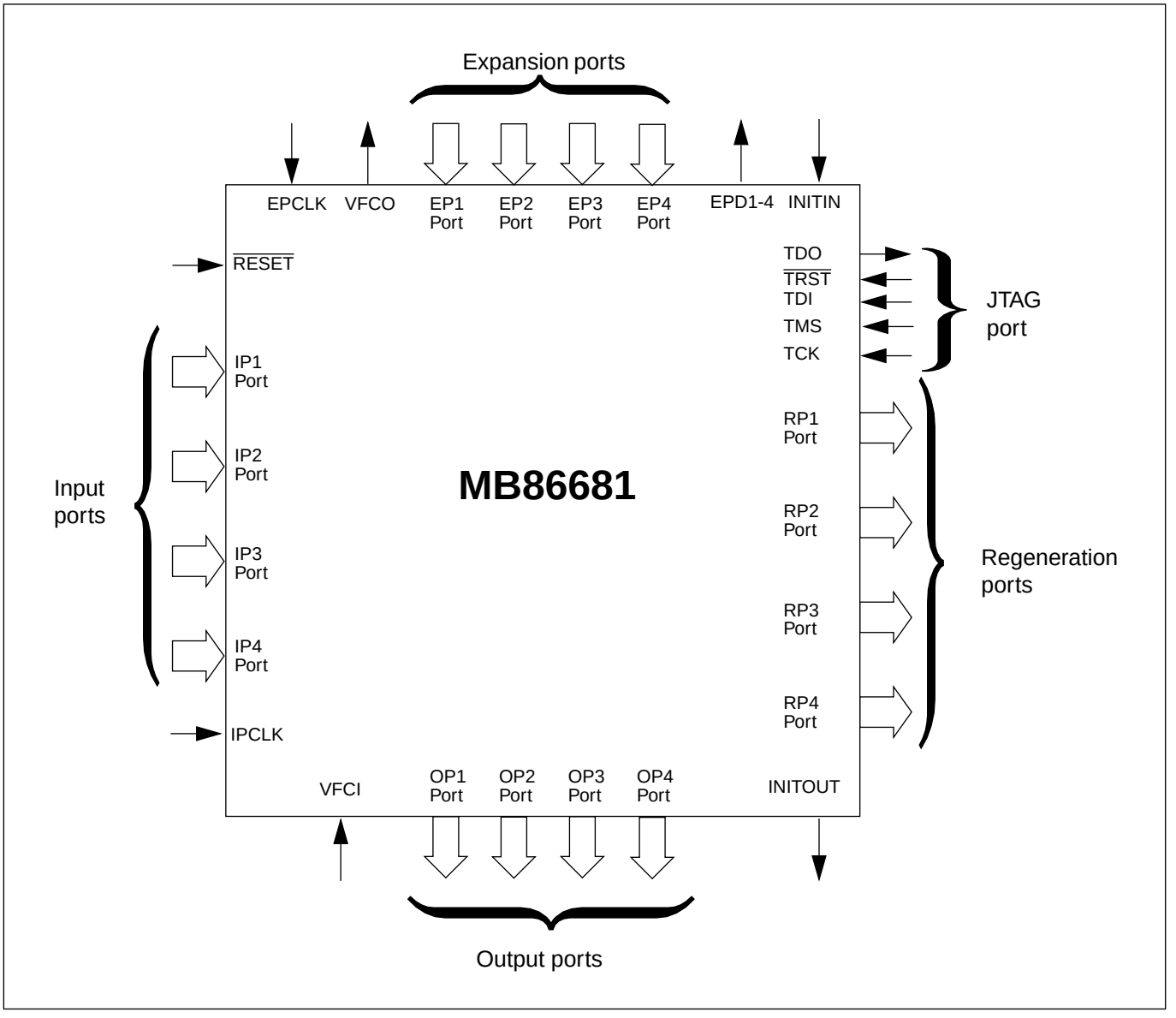



**Figure 3 MB86681 I/O Block Diagram**

## 2.2 Detailed Description

A brief description of each of the MB86681's input and output pins shall now be given.

**$\overline{\text{RESET}}$**
An active low pulse applied to the MB86681's $\overline{\text{RESET}}$ pin will cause an MB86681 switch element to execute an internal Reset instruction cycle. The instruction will only be executed when a clock signal is applied to the IPCLK pin. A minimum of 2 IPCLK clock cycles will be required to complete the Reset instruction cycle.

**IPCLK**
Data present on the input ports IP1DTx to IP4DTx is sampled on the rising edge of this clock. This clock needs to be present if a complete Reset instruction cycle is to be executed following an active low transition on the $\overline{\text{RESET}}$ pin.

**EPCLK**
Data present on the input ports EP1DTx to EP4DTx is sampled on the rising edge of this clock.

The EPCLK input pin can also be used by an MB86681 switch element to determine whether the switch element should act as **Master** or as a **Slave**. If the EPCLK input pin is permanently tied to $V_{SS}$ then the switch element is deemed to be a Master switch element.

If however a clock is present on the EPCLK input pin then the MB86681 switch element is deemed to be a Slave switch element.

**Note:**
It is recommended that for general usage the IPCLK and EPCLK input ports are connected together as shown in SRE-L Clocking Strategy (Master/Slave Configuration).

**Input Ports (IPxSOC, IPxDTx)**
The device comprises four primary input ports, (IP1SOC, IP1DTx) to (IP4SOC, IP4DTx), each of which is organized as 8-bit parallel data together with a start of cell (IPxSOC) bit. All primary input data is sampled on the rising edge of an input clock signal (IPCLK). Incoming data comprises a 3 byte routing tag followed by a 53 byte ATM cell.

Any unused I-input ports should have their unused IPxSOC pin tied to $V_{SS}$.

**Expansion Ports (EPxSOC, EPxDTx)**
The four expansion ports, (EP1SOC, EP1DTx) to (EP4SOC, EP4DTx), are provided for column interconnect in a matrix architecture. The data format on the expansion ports is similar to the primary input port format, except that data is synchronized to an expansion port clock (EPCLK), which is usually provided by the vertically opposite nearest neighbour switch element.

Master Switch elements at the top of each column do not need their expansion ports, in this case, the input pins will take on different functions in order to allow the routing tag characteristics to be defined. Pin functions are described in Section Configuration Registers.

The alternative functions are selected by connecting the EPCLK input signal to $V_{SS}$.

Any unused Expansion ports should have their unused EPxSOC pin tied to $V_{SS}$.

**VFCI**
The VFCI, Vertical Flow Control Input port, permits per queue flow control to be carried out when programmed High and Low priority queue thresholds are exceeded.

When enabled, the MB86681 switch element synchronizes to the VFCI serial highway by detecting the SYN character as defined in International Alphabet No.5.
When not in use the VFCI pin should be tied to either $V_{SS}$ or $V_{D5.}$

**VFCO**
The VFCO, Vertical Flow Control Output port, is used by the MB86681 switch element to transmit flow control data to the switch element's vertically opposite neighbour.

The active high flow control data present on this serial highway permits vertical flow control on cell boundaries, thereby no cell loss is guaranteed once a cell has been routed.

**INITIN**
The INITIN is used by Slave MB86681 switch elements to acquire configuration data immediately following a RESET instruction cycle.

The configuration data may be supplied via the INITOUT pin of a Master switch element or from a device emulating the configuration capability of a Master switch element.

When the MB86681 switch element is deemed to be Master i.e its EPCLK input is tied to $V_{SS}$, the INITIN pin is not used and should be tied to $V_{D5.}$

**INITOUT**
The INITOUT pin is used by Master switch elements to convey the configuration data, acquired through their Expansion port pins, in a serial format to the attached Slave elements.

Slave switch elements do not use their INITOUT pin. When a switch element is configured as a Slave, the INITOUT pin is driven permanently high.

Following an active low transition on the $\overline{\text{RESET}}$ pin the INITOUT pin shall be driven to it's logic "1" state.

**Regeneration Ports (RPxSOC, RPxDTx)**
Four regeneration ports, (RP1SOC, RP1DTx) to (RP4SOC, RP4DTx), are provided for matrix interconnection.

The Flexible Transmission Mode (FTM) feature of the SRE-L permits the synchronous transmission of the Regeneration-Port data to take place on either the rising or falling edge of the IPCLK.

Following a $\overline{\text{RESET}}$ instruction cycle the Regeneration-Port pins are driven to their logic "0" state.

**Output Ports (OPxSOC, OPxDT)**
Four output ports, (OP1SOC, OP1DTx) to (OP4SOC, OP4DTx), provide the primary switch output data. The data format is identical to all other ports.

As in the case of the Regeneration-Port data, the Flexible Transmission Mode (FTM) feature of the SRE permits the synchronous transmission of the Output-Port data to take place on either the rising or falling edge of the IPCLK.

Following a $\overline{\text{RESET}}$ instruction cycle the Output-Port pins are driven to their logic “0” state.

When no data is being output the SRE shall drive these outputs to their logic “0” state.

**EPD1 - EPD4**
The 4 pseudo open collector Early Packet Discard (EPD) notification ports, EPD1 to EPD4, are active low tristate output ports. The 4 EPD ports permit early notification that a cell currently being received has been discarded by the MB86681 switch element.

**TCK**
The TCK input pin provides the clock signal for the JTAG internal test logic. Data received on the TDI input pin shall be sampled on the rising edge of TCK clock signal.

**$\overline{\text{TRST}}$**
The TRST input pin provides an asynchronous reset signal for the JTAG internal test logic. An active low transition on this pin will force the JTAG TAP Controller into it’s Test-Logic-Reset state.

An External pull-up should be connected to this input to ensure that when this input is not driven, a response identical to the application of a logical 1 results.

**TMS**
The TMS input pin shall be sampled on the rising edge of the TCK clock and decoded by the JTAG internal test logic to control test operations.

An External pull-up should be connected to this input to ensure that when this input is not driven, a response identical to the application of a logical 1 results.

**TDI**
The TDI input pin shall provide a port through which JTAG serial test data and instructions may be received by the internal test logic.

An External pull-up should be connected to this input to ensure that when this input is not driven, a response identical to the application of a logical “1” results.

**TDO**
The TDO output pin represents a tristate serial output JTAG port through which test instructions and data from the internal test logic may be conveyed. Changes in the state of the signal driven through TDO shall only occur following the falling edge of TCK. When no signal is being driven through the TDO port the output pin should revert to its tristate condition.

Immediately following power-up the TDO output pin shall remain in its undriven tristate state.

**TST1..TST4**
Four test pins are provided for internal use only. It is recommended that test pins TST1, TST2 and TST3 are connected to $V_{SS.}$

# 3 Initialization and Configuration

## 3.1 Overview

A block diagram of the switch element is illustrated in Figure 5. From this, it can be seen that each of the I-input ports is connected in parallel to an address filter via a high speed multiplexer. The address filter processes the address bits contained in a 24 bit routing tag and if appropriate, the associated cell will be routed through to the desired FIFO buffer. The MB86681 switch element permits each output FIFO to be sub-divided into a high and low priority section. The address filter examines each received cell's routing tag to determine its priority level.

Each output port is serviced by a High/Low priority multiplexer which removes cells from the high and low priority queues. The multiplexer will always give preference to high priority cells.
The above functions are described in more detail in the following paragraphs.

## 3.2 Recommended Clocking Strategy

The recommended SRE-L matrix clocking strategy for a Master / Slave configuration is shown in SRE-L Clocking Strategy (Master/Slave Configuration). Note that the recommendation requires both the IPCLK and EPCLK ports within the Column of a matrix to be connected together.

Use of INITIN and INITOUT pins for Initialization illustrates how a pure Slave SRE-L matrix may be clocked.

## 3.3 Reset Operation

The MB86681 provides an active low $\overline{\text{RESET}}$ pin. Asynchronous transitions on this pin are captured internally by the MB86681 and synchronized to the IPCLK clock. The internal synchronous $\overline{\text{RESET}}$ operation of the MB86681 is deemed to be complete 2 IPCLK clock periods after the removal of the active low $\overline{\text{RESET}}$ signal.

All outputs shall be reset to their inactive states within 2 IPCLK clock periods after an active low pulse has been applied to the $\overline{\text{RESET}}$ pin.

The MB86681 requires the presence of the IPCLK clock signal to complete a $\overline{\text{RESET}}$ operation.

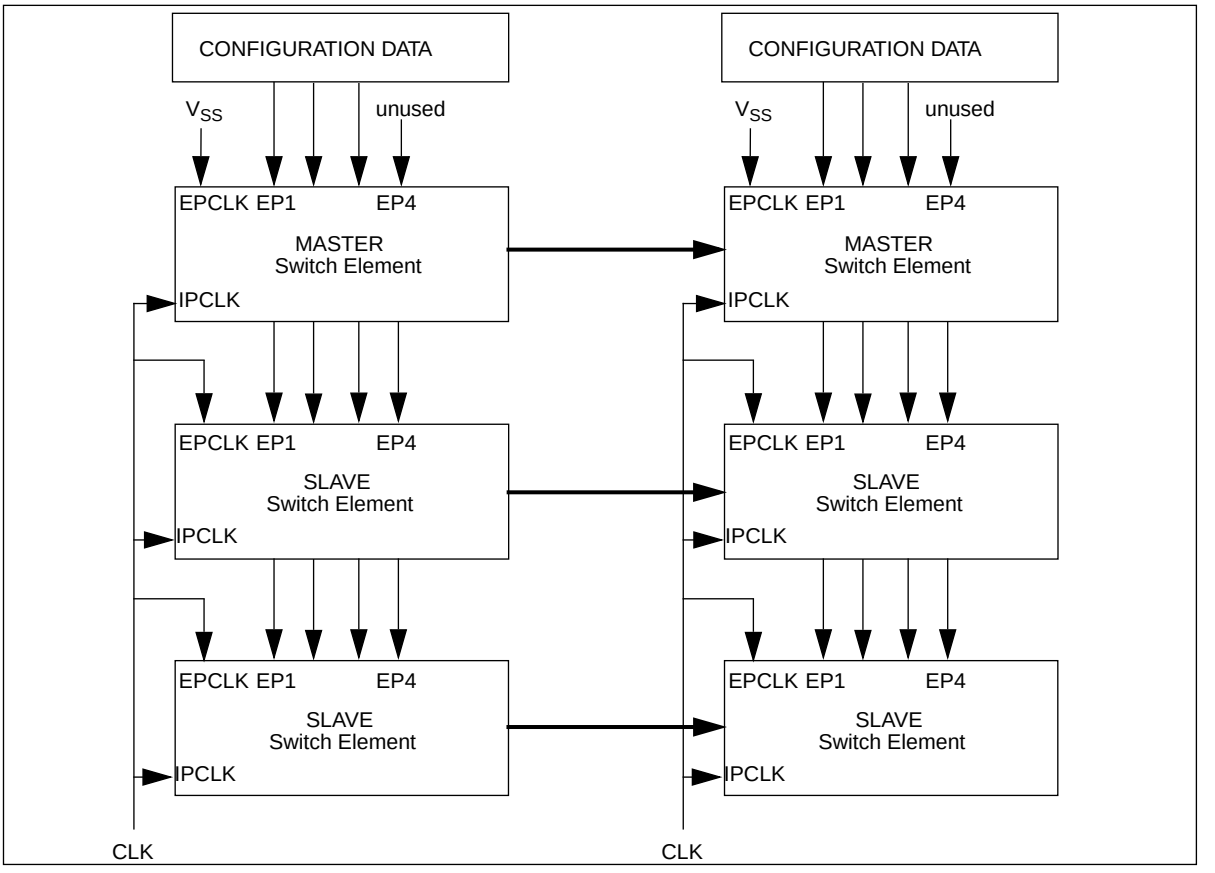



**Figure 4 SRE-L Clocking Strategy (Master/Slave Configuration)**

## 3.4 Initialization.

The Configuration Manager block illustrated in Figure 5 is responsible for initialising an MB86681 switch element. An MB86681 switch element may be initialised/configured by one of two mechanisms depending on whether the element is a Master or a Slave element.

Figure 6 illustrates how the INITIN and INITOUT pins of Master and Slave elements may be connected in order to allow initialisation of the respective elements.

Master MB86681 switch elements obtain their configuration data from the unused Expansion port pins as shown in Figure 6a, while Slave elements may obtain their configuration data from either the INITOUT pin of a Master element (as in Figure 6a) or from a Programmable Logic Device (PLD), such as that shown in Figure 6b, capable of transferring a serial data stream identical to that shown in Figure 9.

MB86681 elements enter their Initialization phase when the $\overline{\text{RESET}}$ operation described above is complete.

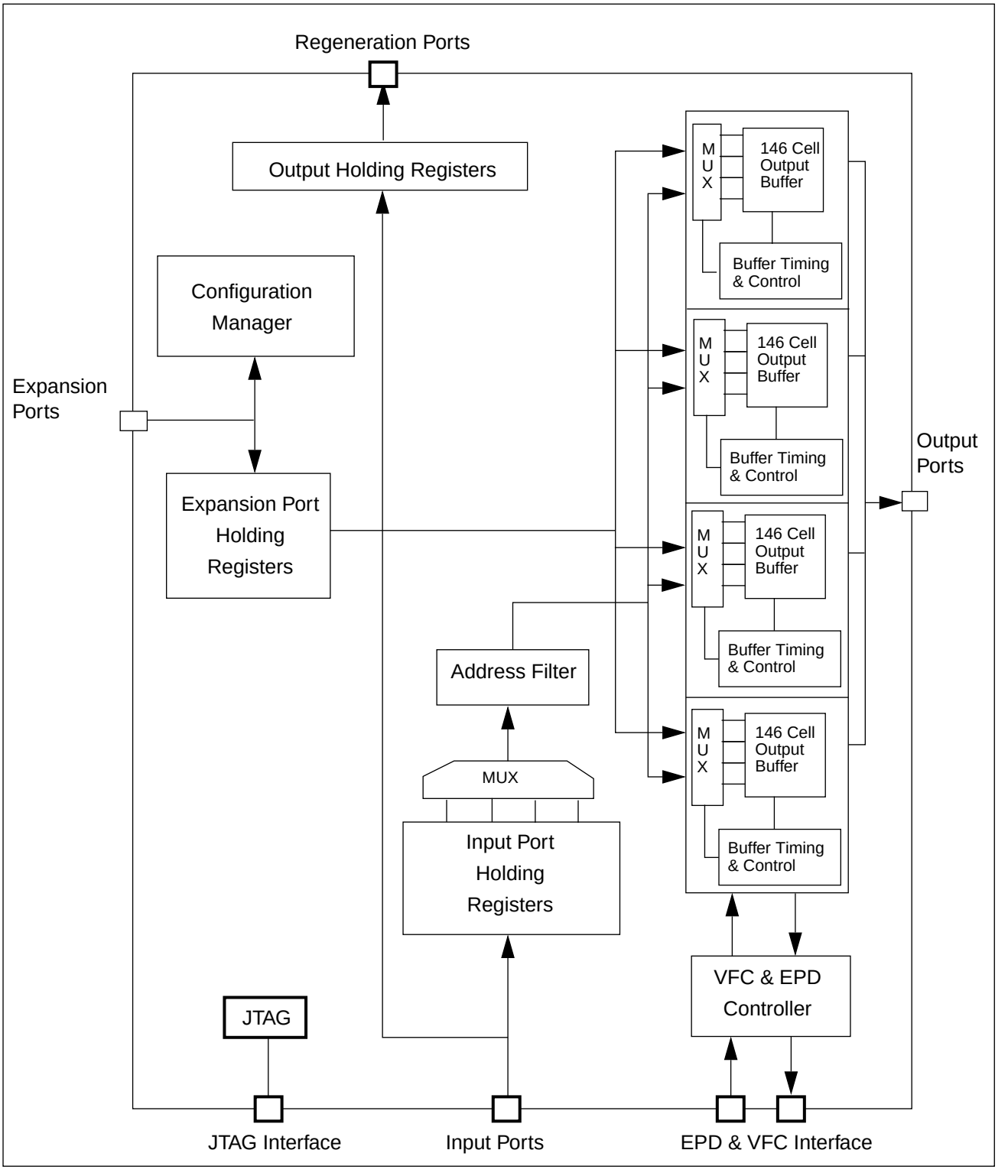



**Figure 5 MB86681 Block Diagram**

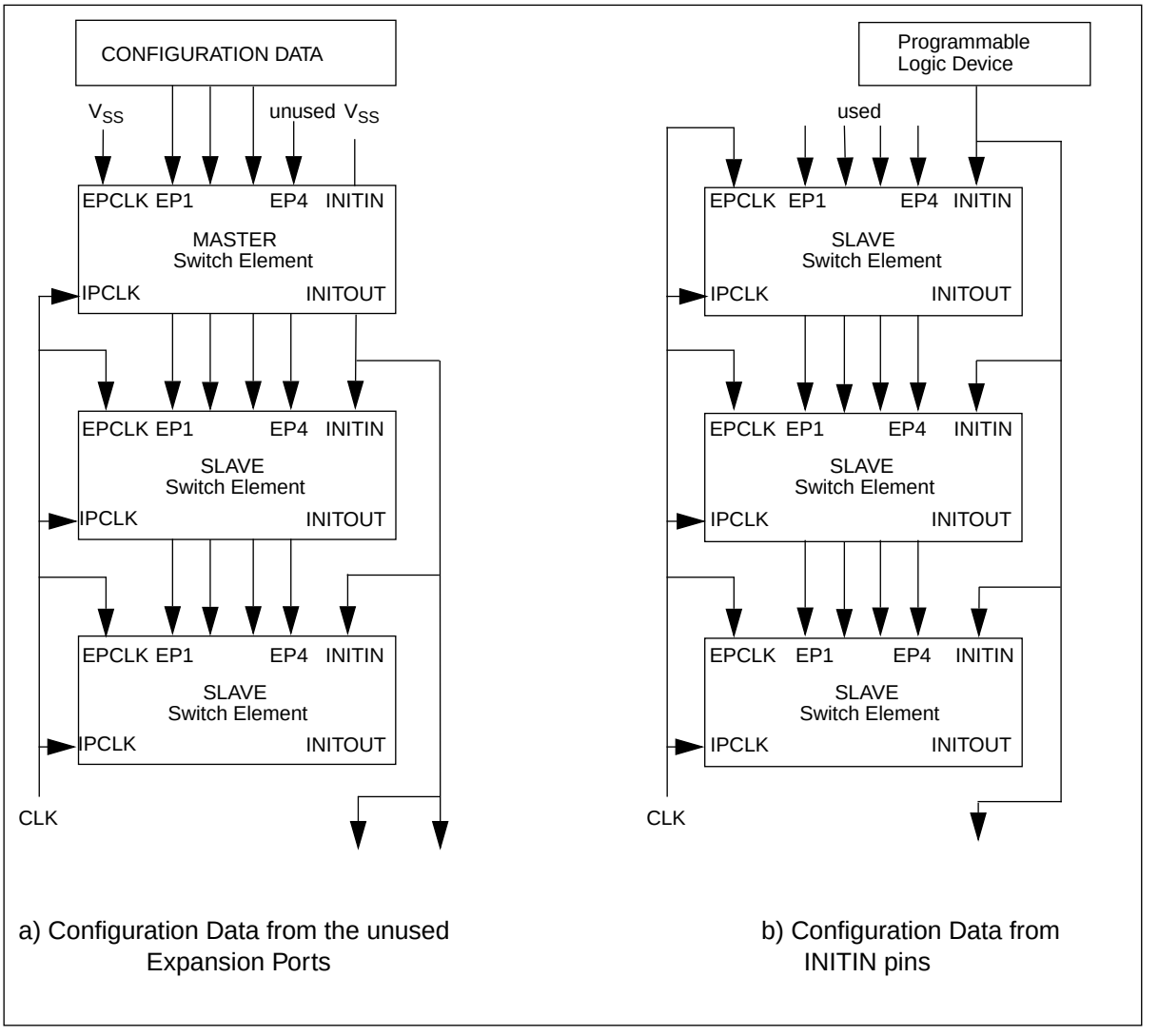



**Figure 6 Use of INITIN and INITOUT pins for Initialization**

## 3.5 Initialization of a Master SRE-L Switch Element.

An MB86681 switch element shall be deemed to be a Master when its EPCLK pin is permanently tied to Vss. In such a configuration, the SRE-L switch element may be internally configured via the data present on Expansion ports EP1DTx, EP2DTx & EP3DTx.

The data present on the three expansion ports is immediately parallel loaded into the eleven Master switch element Configuration registers following a master reset instruction cycle operation.

A total of 20 input pins are used to configure the operating mode of the MB86681. These inputs are shared

with Expansion port inputs and are selected by configuring the switch element as a Master.
Once configured, a Master switch element commences transferring the contents of it's Configuration registers to the connected Slave elements. The transfer of Configuration data between the Master and Slave elements is accomplished by the Master switch element transmitting the contents of it's Configuration registers in a serial format via the INITOUT pin to connected Slave device's INITIN pin, as shown in Figure 6.

## 3.6 Configuration Registers

The MB86681 switch element provides 11 user definable configuration registers. The configuration registers may be configured via the Expansion port pins for Master devices or via the serial input port, INITIN, for the Slave devices.

A list of the eleven Configuration registers together with the associated Expansion port pins used to configure them on a Master device is given below.

1. **Address Field Size**
   AFS1..AFS0(EP1DT7..EP1DT6)

2. **Address Field Location**
   AFL3..AFL0(EP1DT5..EP1DT2)

3. **Column Address**
   CA2..CA0(EP2DT7..EP2DT5)

4. **High Priority Queue Enable**
   HPQE(EP2DT4)

5. **EFCI Enable / Disable control**
   EFCIE(EP2DT3)

6. **EFCI Thresholds**
   EFCIT1..EFCIT0(EP2DT2..EP2DT1)

7. **Flexible Transmission Mode**
   FTM(EP3DT7)

8. **Per VC EFCI Enable / Disable control**
   PEFCIE(EP3DT6)

9. **Per VC EFCI Fixed Thresholds**
   PEFCIT1..PEFCIT0(EP3DT5..EP3DT4)

10. **VFC Enable / Disable**
    VFCE(EP3DT3)

11. **VFC Thresholds**
    VFCT1..VFCT0(EP3DT2..EP3DT1)

A description of the different functions associated with these Configuration registers is now given.

### 3.6.1 Address Field Size / Location Configuration Registers

The Expansion port pins EP1DT7 to EP1DT2 are used by Master MB86681 switch elements to configure their Address Field Size (AFS) and Location (AFL) registers immediately following a master RESET instruction cycle. The Address Field Size and Location registers are two inter-dependent registers, used by the MB86681 device to select a subset of routing tag bits which are to be used for address filtering.

The address field size may vary from 2 bits (for Batcher/Banyan type topologies) to a maximum of 5 bits (for a 32 X 32 matrix).

With a 5-bit address field, there are 4 possible locations within the 24-bit tag (note the upper 4 bits are used for control information). With a 2-bit address field there are 10 possible locations. The relationship between address field size and location within the routing tag is illustrated in Figure 7.

Figure 7 also illustrates how the switch elements shall interpret the Address size/location inter-relationship table to acquire the valid address field within the routing tag, when configured with an address size of four bits and a start address field location of PA8.

**Note:**
**The AFS field in the configuration registers is not applicable to multicast cells.**

| Address Size Pins | | Address size |
|---|---|---|
| EP1DT7 | EP1DT6 | |
| AFS1 | AFS0 | |
| 0 | 0 | 2 bits |
| 0 | 1 | 3 bits |
| 1 | 0 | 4 bits |
| 1 | 1 | 5 bits |

| Address Field Location Pins | | | | Start of Address field location within tag | | | | |
|---|---|---|---|---|---|---|---|---|
| EP1DT5 | EP1DT4 | EP1DT3 | EP1DT2 | | | | | |
| AFL3 | AFL2 | AFL1 | AFL0 | | | | | |
| 0 | 0 | 0 | 0 | PA0 | PA0 | | PA0 | PA0 |
| 0 | 0 | 0 | 1 | PA5 | PA4 | | PA3 | PA2 |
| 0 | 0 | 1 | 0 | PA10 | PA8 | | PA6 | PA4 |
| 0 | 0 | 1 | 1 | PA15 | PA12 | | PA9 | PA6 |
| 0 | 1 | 0 | 0 | | PA16 | | PA12 | PA8 |
| 0 | 1 | 0 | 1 | | | | PA15 | PA10 |
| 0 | 1 | 1 | 0 | | | | | PA12 |
| 0 | 1 | 1 | 1 | | | | | PA14 |
| 1 | 0 | 0 | 0 | | | | | PA16 |
| 1 | 0 | 0 | 1 | | | | | PA18 |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 1st Octet | PC | MC | CLT1 | CLT0 | PA0 | PA1 | PA2 | PA3 |
| 2nd Octet | PA4 | PA5 | PA6 | PA7 | PA8 | PA9 | PA10 | PA11 |
| 3rd Octet | PA12 | PA13 | PA14 | PA15 | PA16 | PA17 | PA18 | PA19 |

**Figure 7 Address Size/Location Inter-relationship**

## 3.6.2 Column Address Configuration Register

The Expansion port pins EP2DT7 to EP1DT5 are used by Master MB86681 switch elements to configure their Column Address register immediately following a master RESET instruction cycle. The 3 bit Column Address Configuration register is used to define the base address for the switch element when it is used in a matrix configuration. The Column Address allows the switch element to determine which of the switch matrix Columns it resides in and hence the group of output ports to which it is attached.

| Column Address | | | Column Group |
|---|---|---|---|
| CA1 EP2DT7 | CA2 EP2DT6 | CA3 EP2DT5 | |
| 0 | 0 | 0 | 1-4 |
| 0 | 0 | 1 | 5-8 |
| 0 | 1 | 0 | 9-12 |
| 0 | 1 | 1 | 13-16 |
| 1 | 0 | 0 | 17-20 |
| 1 | 0 | 1 | 21-24 |
| 1 | 1 | 0 | 25-28 |
| 1 | 1 | 1 | 29-32 |

**Table 1 Column Address Coding**

Table 1 illustrates the valid Column Address permutations whilst Figure 8 illustrates how individual elements may be configured within a switch matrix.

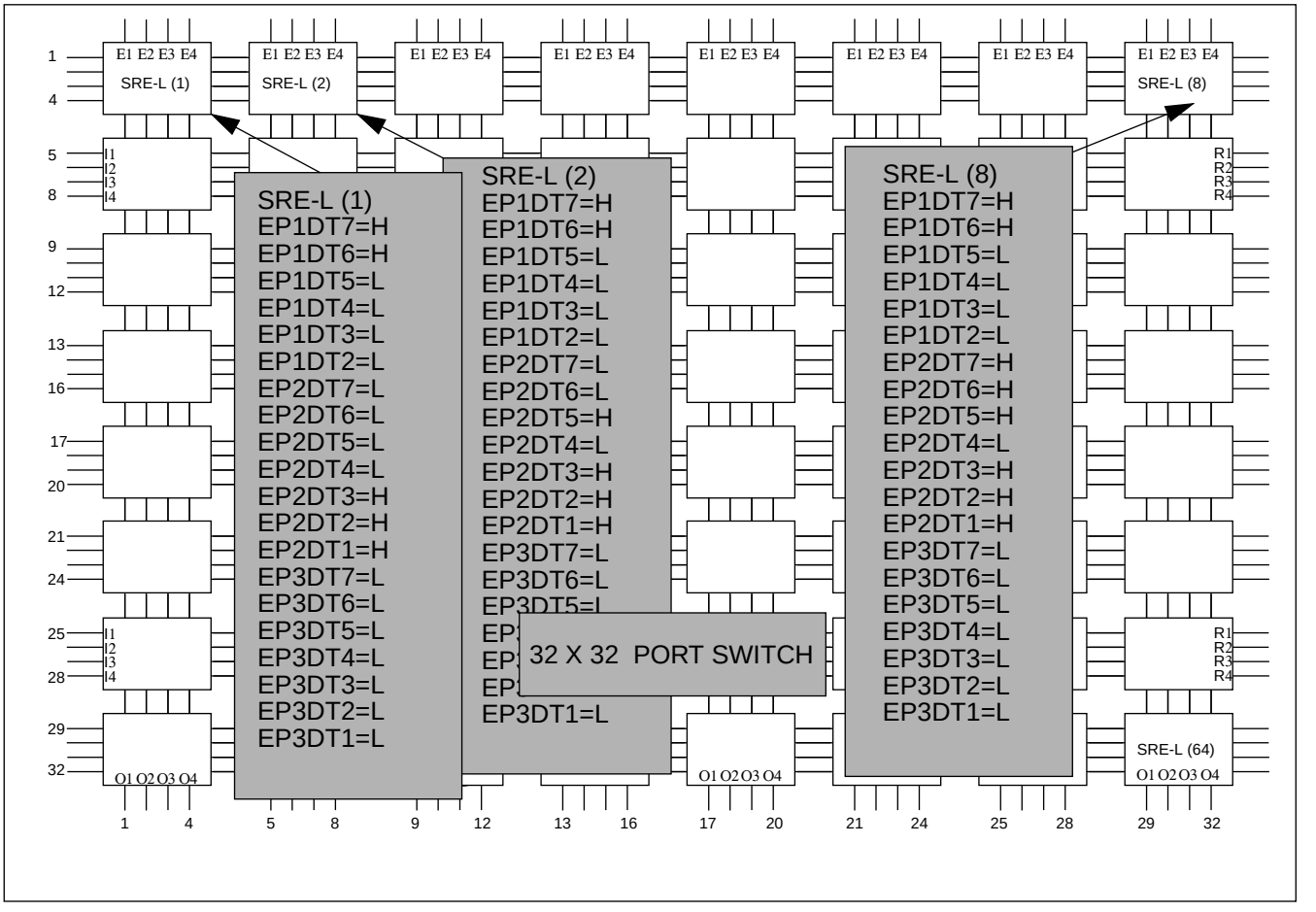



**Figure 8 Column Addressing**

## 3.6.3 High Priority Queue Enable Configuration Register

The Expansion port input pin EP2DT4 is used by Master switch elements, immediately following a master RESET instruction cycle, to enable or disable the high priority queue mechanism associated with each output buffer. When tied to $V_{SS}$, the **Dual queue** per port mode of operation is invoked. In this configuration mode the high priority queue is enabled providing the user with a 25 cell High priority queue and a 121 cell Low priority queue per output port.

When the Expansion port input pin EP2DT4 is tied to $V_{D5}$, for a Master switch element, the **Mono queue** per port mode of operation is invoked. In this operating mode the two output queues are merged to form a single 146 cell output queue per port.

### 3.6.4 EFCI Enable / Disable Configuration Register

On a Master MB86681 switch element, the Expansion port input pin (EP2DT3) may be used to Enable/ Disable the Explicit Forward Congestion Indication (EFCI) function. When this pin is tied to $V_{SS}$ on a Master MB86681 element, the EFCI function will be disabled both on the Master switch element and any attached Slave elements (note Slave elements are configured by the INITIN and INITOUT configuration illustrated in Figure 6a).

When the EP2DT3 pin is tied to $V_{D5}$, on a Master switch element, the EFCI function will be enabled on both the Master element and any attached Slave elements.

### 3.6.5 EFCI Threshold Configuration Register

The Expansion port pins (EP2DT2 and EP2DT1) on a Master switch element may be used to select the Output data queue fill level thresholds at which the EFCI function may be implemented. Table 2 illustrates how the logic levels applied to these pins are interpreted by the Master and attached Slave elements.

| EFCIT 1 EP2DT2 | EFCIT 0 EP2DT1 | EFCI Threshold |
|---|---|---|
| 0 | 0 | Not Used |
| 0 | 1 | 20% full |
| 1 | 0 | 50% full |
| 1 | 1 | 80% full |

**Table 2 EFCI Threshold Coding**

**Note:**
**The terms and conditions permitting EFCI marking as described above may only be superseded by ATM cells permitting Per VC EFCI marking being received by an MB86681 switch element with it's Per VC EFCI marking function enabled.**

### 3.6.6 Flexible Transmission Mode Configuration Register

The Expansion port pin (EP3DT7) on a Master SRE-L may be used to select a transmission edge for the O and R-Port data.

When the EP3DT7 pin is tied to $V_{SS}$ the data present on the O and R-ports is transmitted synchronous to the falling edge of the IPCLK. This transmission mode is referred to as the Fujitsu Cell Stream (FCS) mode of operation.

When the EP3DT7 pin is tied to $V_{DD}$ the data present on the O and R-ports is transmitted synchronous to the rising edge of the IPCLK.This transmission mode is referred to as the Inverse Fujitsu Cell Stream

(IFCS) mode of operation.

When operating in the FCS mode, data present on each input is sampled on the rising edge of its respective clock whilst data transitions on the Output and Regeneration ports take place on the falling edge of the IPCLK signal.

When operating in the IFCS mode, data present on the Inputs will be sampled on the rising edge of their respective clocks whilst data transitions on the Cell Stream Output Ports and Regeneration ports will take place on the rising edge of the IPCLK signal.

**Note:**
**When operating the SRE-L devices at 40Mhz, it is recommended that the IFCS mode is used.**

## 3.6.7 Per VC EFCI Enable / Disable Configuration Register

On a Master switch element, the Expansion port pin (EP3DT6) may be used to Enable/Disable the Per VC Explicit Forward Congestion Indication (EFCI) function. When this pin is tied to $V_{SS}$, the Per VC EFCI function will be disabled both on the Master and any attached Slave MB86681 elements (assuming a configuration as illustrated in Figure 6a).

When the EP3DT6 pin is tied to $V_{D5}$, on a Master MB86681 switch element the Per VC EFCI function will be enabled on both the Master and any attached Slave MB86681 elements.

**Note:**
**When both the MB86681's EFCI and Per VC EFCI functions are enabled, the Per VC EFCI function will take precedence.**
**Consequently, ATM cells permitting Per VC EFCI marking will only be subject to EFCI marking when their programmed EFCI Thresholds are equalled or exceeded.**

## 3.6.8 Per VC EFCI Fixed Threshold Configuration Register

The Expansion port pins (EP3DT5 and EP3DT4) on a Master MB86681 element may be used to select the output data queue fill level thresholds at which the Per VC EFCI function may be implemented. Table 3 illustrates how the logic levels applied to these pins are interpreted by the Master and attached Slave elements.

| EFCIT 1 EP3DT5 | EFCIT 0 EP3DT4 | EFCI Threshold |
|---|---|---|
| 0 | 0 | Not Used |
| 0 | 1 | 20% full |
| 1 | 0 | 50% full |
| 1 | 1 | 80% full |

**Table 3 Per VC EFCI Fixed Threshold Coding**

**Note:**
**The programmable EFCI Fixed Thresholds are only applicable to MB86681 devices configured as Non-multicast servers.**

## 3.6.9 VFC Enable / Disable Configuration Register

On a Master MB86681 element, the Expansion port pin (EP3DT3) may be used to Enable/Disable the Vertical Flow Control (VFC) function.

When the EP3DT3 pin is tied to $V_{D5}$, the Vertical Flow Control function will be enabled on both the Master and attached Slave elements.

## 3.6.10 VFC Threshold Configuration Register

The Expansion port pins (EP3DT2 and EP3DT1) on a Master MB86681 element may be used to select the Vertical Flow Control Thresholds, which when equalled or exceeded cause the MB86681 switch element's vertical queue flow control function to be implemented. Table 4 illustrates how the logic levels applied to these pins are interpreted by the Master and attached Slave elements.

| OQFCT 1 EP3DT2 | OQFCT 0 EP3DT1 | Output Queue Flow Control Threshold (OQFCT) |
|---|---|---|
| 0 | 0 | Not Used |
| 0 | 1 | 50% full |
| 1 | 0 | 80% full |
| 1 | 1 | 95% full |

**Table 4 Output queue Flow Control Threshold Coding**

**Note:**
**When operating in the Dual queue mode, the upper VFC Threshold for the High priority queue is 80% and not 95%.**

## 3.7 Initialization of a Slave SRE-L Switch Element

Immediately following a master RESET instruction cycle, Slave switch elements commence monitoring their INITIN pins. Unlike Master devices, the Slave switch elements use their serial INITIN input port to acquire configuration data.

On detecting the active low Start sync bit, as shown in Figure 9, the Slave switch element uses its IPCLK clock signal to determine the nominal centre bit position of the serial data stream. Multiple sampling of the serial data stream is carried out to eliminate the possible detection of a false start polarity.

On detecting the valid Start sync bit, the Slave switch element shall sample each bit of the received initialization character by counting 5 clock periods from the preceding bit's nominal centre until all the necessary configuration data has been acquired and loaded into the Configuration registers.

On acquiring their configuration data, the Slave switch elements cease to monitor their INITIN pins.
Figure 9 in conjunction with Table 5 illustrates the format of the data on this serial highway together with the order of transmission.

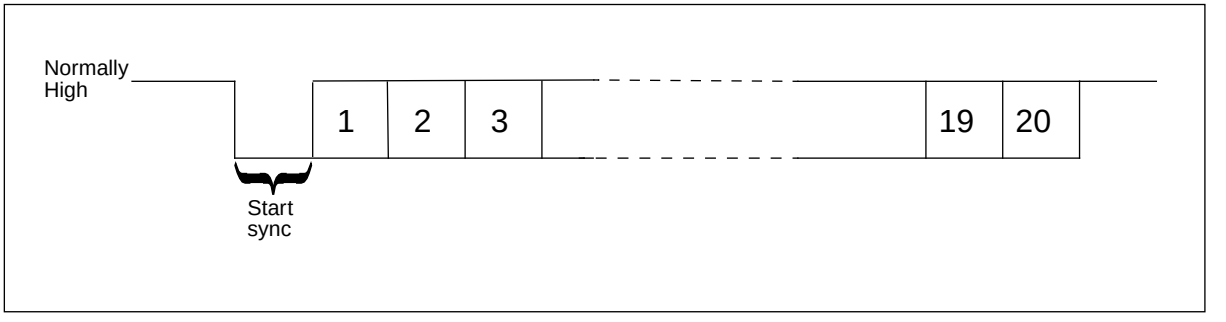



**Figure 9 Init line serial data format**

Transmission of data on the serial INITOUT/INITIN serial highway shall primarily be of an asynchronous format with data bit periods equal to the IPCLK/5. The transmitted data will not necessarily be phase aligned to the IPCLK. The INITOUT port data transitions are synchronised to the falling edge of IPCLK/5 and are sampled by Slave switch elements on the rising edge of their IPCLK.

Master switch elements commence transmission by driving the INITOUT pin low. The configuration data will then be transmitted in the format shown in Figure 9.

Figure 9 shows how the configuration data presented at the Expansion ports of a Master switch element is translated into the serial bit stream illustrated in Figure 9. The data is transmitted serially with the most significant bits occupying the lower bit positions of the INITOUT line.

All other unused Expansion port input pins are reserved for internal use and should be connected to $V_{SS}$.

| Function | Expansion Port Pins (Master Configuration) | Init line Bit Position(s) (Slave Configuration) |
|---|---|---|
| Address Field size | EP1DT7..EP1DT6 | Bits 1..2 |
| Address Field location | EP1DT5..EP1DT2 | Bits 3..6 |
| Column Group | EP2DT7..EP2DT5 | Bits 7..9 |
| High Priority Queue Enable | EP2DT4 | Bit 10 |
| EFCI Enable/Disable control | EP2DT3 | Bit 11 |
| EFCI Thresholds | EP2DT2..EP2DT1 | Bits 12..13 |
| FTM | EP3DT7 | Bit 14 |
| Per VC EFCI Enable/Disable Control | EP3DT6 | Bit 15 |
| Per VC EFCI Fixed Thresholds | EP3DT5..EP3DT4 | Bits 16..17 |
| Output Queue Flow Control Enable/disable | EP3DT3 | Bit 18 |
| Output Queue Flow Control Thresholds | EP3DT2..EP3DT1 | Bits 19..20 |

**Table 5 Master/Slave Configuration table**

# 4 Functional Description

## 4.1 Address Filtering Normal Operation

ATM Cells arriving at the ingress side of the MB86681 element will have a 3 byte routing tag appended to the head of the ATM Cell. The 3 byte routing tag is used by the MB86681 switch elements to carry out Address filtering functions in conjunction with selective cell discard operations on the incoming cell. Figure 10 illustrates the main principles of operation.

The switch elements use the Start Of Cell (IPxSOC) signal to locate the 3 byte routing tag. On acquiring the routing tag the MB86681 switch elements commence the interpretation of the various fields therein. Figure 10 illustrates how the MB86681 switch elements receives ATM Cells 1 and 2 on it's ingress side and then proceeds to route both the Cell and it's associated routing tag to the required output port.
The MB86681 switch element is capable of distinguishing between two types of cells. The two cell types are differentiated by the formats of their routing tags. The two routing tag formats are referred to as:

1. The normal routing tag format
2. The Multicast routing tag format

The normal routing tag format is illustrated in Figure 10 appended to ATM Cells 1 and 2, whilst a more detailed description of the significance of the bits in this routing tag is shown in Figure 11.

### 4.1.1 Normal Routing Tag Control Field Format

A description of the function of the bits within this routing tag shall now be given commencing with the Priority control bit.

#### Priority Control (PC) Bit

The Priority Control (PC) bit determines whether the associated cell is loaded into the high priority queue or the low priority queue. This bit should be set on a per virtual circuit basis in order to guarantee that cell sequence numbering is preserved.

High priority channels should only be used for delay sensitive (or loss sensitive) data, and the total amount of traffic allocated to high priority channels should form a small percentage of the total available output bandwidth.

When the switch elements are configured for single / mono queue mode of operation the PC bit has no significance.

## Cell Loss Threshold Field CLT0,CLT1

Cell Loss Threshold Field CLT0, CLT1
These bits are used to control the treatment of cells which have the CLP bit in their ATM cell header set. They determine the output queue fill level at which the cells will be selectively discarded.

| CLT 1 | CLT 0 | Discard Threshold |
|---|---|---|
| 0 | 0 | No discard |
| 0 | 1 | 20% full |
| 1 | 0 | 50% full |
| 1 | 1 | 80% full |

**Table 6 Discard Threshold Coding**

**Note:**
**When operating in the Dual queue mode, the Cell loss Threshold field is only applicable to ATM Cells with their PC bit set to "0".**

**When operating in the Mono queue mode, all ATM cells are treated as Low priority cells irrespective of the Status of their PC bit and consequently will be subject to selective cell discard if the above criteria are met.**

## Routing Field PA0-PA19

The routing Field PA0 to PA19 is used by the MB86681 switch elements to determine the port destination of the received cell. The validity of the bits in the 20 bit routing field are determined by the programmed Address Field Size and location parameters as specified in section 3.6.1.

In Figure 10, SRE-L's (C) and (D) are configured with the parameters:

1. Address Field Size: 3 bits
2. Address Field Location: PA0
3. Column Address : 5-8

Whilst SRE-L's (A) and (B) are configured with the alternative parameter:

4. Column Address : 1-4

As a result of these configurations ATM Cell 1 passes transparently through SRE-L (A), merely being re-timed at SRE-L (A)'s R-ports prior to being presented at the corresponding ingress port of SRE-L (C).

In Figure 11 the left most justified bits of the routing field are deemed to be most significant.
SRE-L (C) is configured to analyse the routing field PA0 to PA2. As a result ATM Cell 1 is routed to port 8 of SRE-L (C).

On being routed, the ATM Cell 1 traverses the matrix vertically eventually arriving at SRE-L (D)'s output port as shown.
Like SRE-L (C), SRE-L (B) is configured to analyse the routing field PA0 to PA2. As a result ATM Cell 2 is routed to port 3 of SRE-L (B).

The unused routing fields in the 20 bit routing tag may be used to route the cells through numerous stages prior to further address translation operations being required.

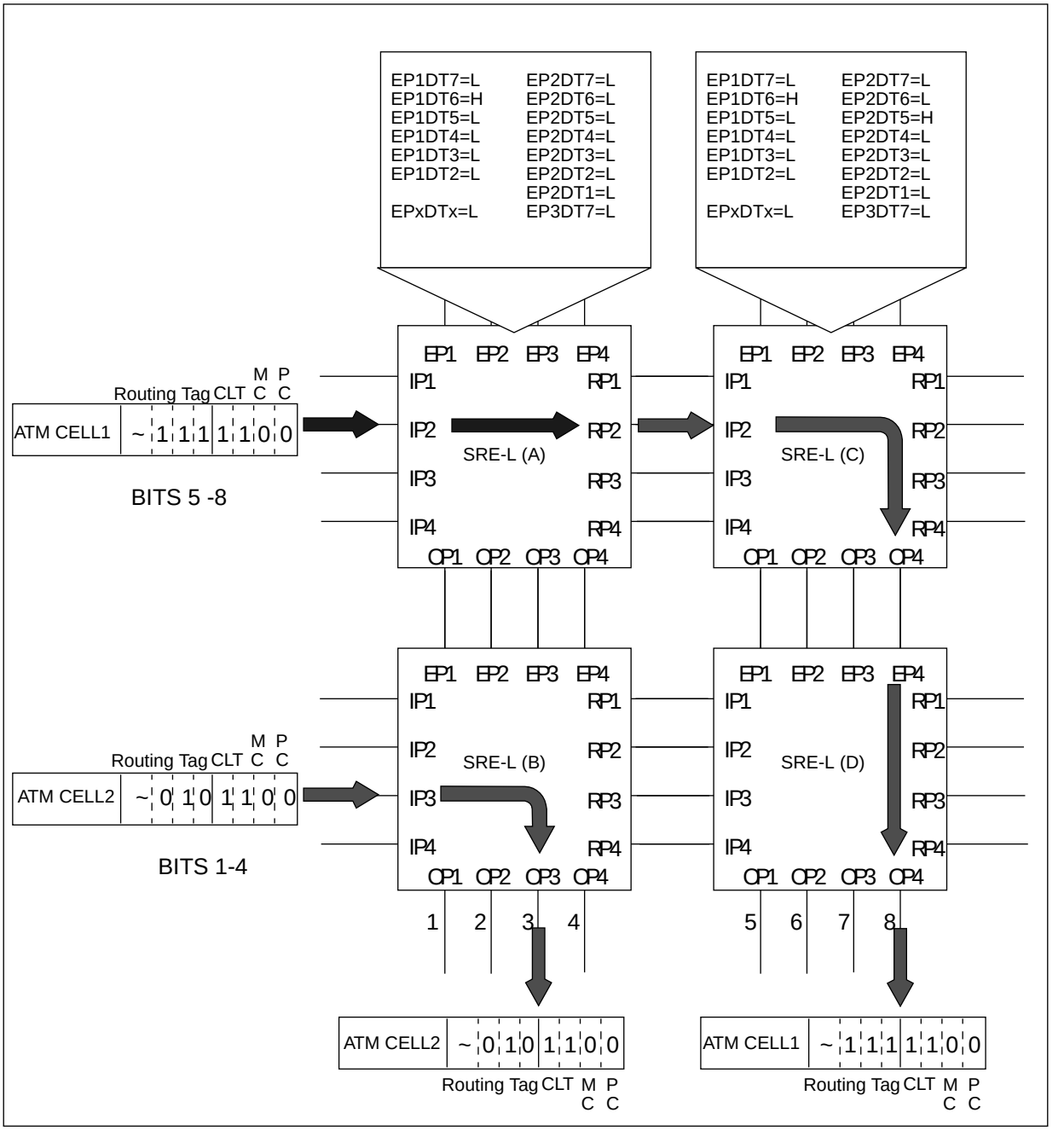



**Figure 10 Address Filtering**

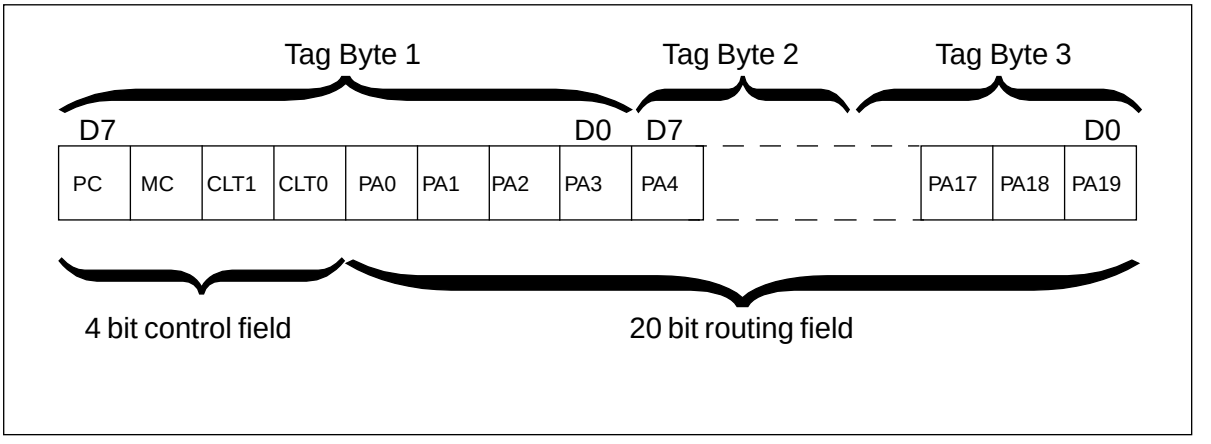



**Figure 11 Normal Routing Tag Format**

## 4.1.2 Multicast Routing Tag Control Field Format

The MB86681 switch elements are capable of performing cell replication. The cell replication operation of the switch elements permits it to transmit a single ATM cell to more than one output port. This operational mode of cell replication is known as Multicasting.

The Multicasting function is invoked by setting the Multicast Control (MC) bit of the Multicast routing tag as shown in Figure 12.

The Multicast routing tag illustrated in Figure 12 is comprised of 5 fields. A brief description of the significance of these fields is now given.

### Priority Control (PC) Bit

The Priority Control (PC) bit has exactly the same definition as that described for the normal routing tag in section 4.1.1.

### Multicast Control (MC) Bit

The Multicast Control (MC) bit is used by the MB86681 switch elements to tag the received ATM Cell as a Multicast cell. This cell will therefore be subject to replication by MB86681 devices configured to carry out this function.

### Relay Link Address Field

The Relay Link Address Field shown in Figure 12 is used as the cell routing field by MB86681 devices not

configured to carry out the cell replication function indicative of Multicasting.
Devices not configured to carry out cell replication will interpret the Relay Link Address Field as a 5 bit routing field, with RL4 representing the most significant bit of the field.
The received cell will therefore be treated like a cell with a normal routing tag format and routed to the port specified in the Relay Link Address Field.

### Output Group Select (OGS) Bit

The Output Group Select (OGS) bit is used by the MB86681 elements to determine the band of output ports over which the received cell may be Multicasted to.
The OGS bit in the Multicast routing tag is only used by MB86681 devices configured to carry out the Multicast operation.

### Multicast Bit mask field

The Multicast bit mask field is used to select the desired ports to which a received cell may be Multicasted. The Multicast bit mask field is only used by MB86681 devices configured to carry out the Multicast operation.

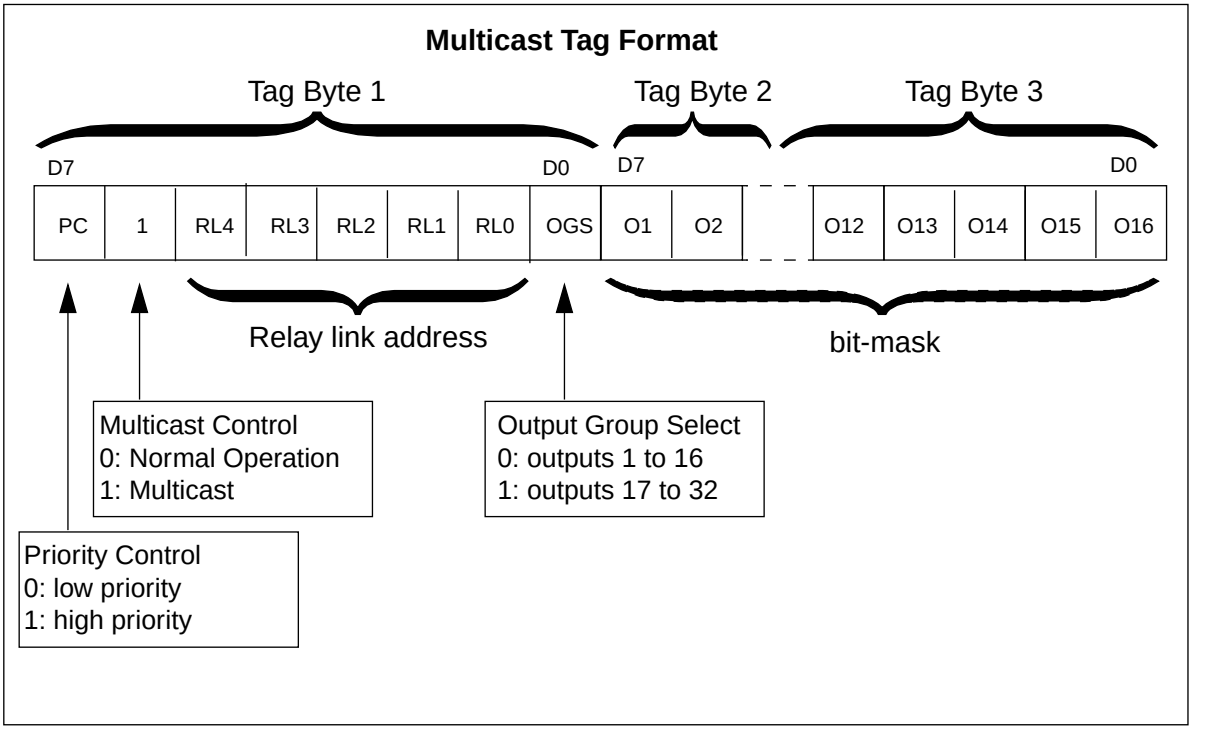



**Figure 12 Routing Tag Format for Multicast operation**

## 4.2 Address Filtering Multicast Operation

The MB86681 Multicast function is invoked by setting the Multicast Control (MC) bit in the received cell's routing tag. When this bit is set it changes the way in which the tag field is interpreted.

In Multicast mode the tag is divided into a 16 bit mask field, an output group select field and a relay link address field. The PC and MC bit positions are unchanged. The multicast routing tag is illustrated in Figure 12.

The following generic description assumes a two stage 64X64 switch comprising four 32X32 matrices, as shown in Figure 13.

For the purposes of this description, a Multicast server is defined as a matrix comprised of MB86681 devices configured to perform the Multicast operation, i.e cell replication.

Multicast server matrices are constructed from MB86681 devices configured with their Address Location Field set to zero. Matrices configured in this manner are assumed to provide the primary outputs as shown in the multi-stage configuration in Figure 13.

In Figure 13 matrices B and D provide the primary outputs and consequently have their Address Location Field set to zero. As a result matrices B and D are referred to as Multicast servers.
Switch Matrices A and C are configured with MB86681 devices whose Address Location Fields are > 0. As a result these matrices are referred to as Non-Multicast servers

A description of the Multicast routing mechanism is now explained using the set-up illustrated in Figure 13. ATM Cell 1 is configured with a Multicast routing tag. This cell is applied to input port 2 of the Non-Multicast server matrix A.
Matrix A analyses the received cell's Relay Link Address Field and routes the cell plus appended routing tag to output port 32.

The routed cell then arrives at input port 1 of the Multicast server matrix D. The receiving MB86681 devices within the switch matrix will interrogate the OGS bit and bit mask fields of the received cell's routing tag to determine if cell replication is necessary.

The bit mask field in conjunction with the OGS bit will determine the outputs to be selected for cell transmission. A logical '1' in the bit mask field will cause the cell to be forwarded on the corresponding output port and a logical '0' will cause the cell to be discarded.

This mechanism allows a single primary input cell to be directed to up to 16 primary outputs associated with a single output group. Hence, for the 64X64 switch illustrated in Figure 13, an input cell may need to be copied up to 4 times in order to achieve full coverage. The copying process may be performed by the Fujitsu Network Termination Controller (MB86683X) which will provide sufficient buffering to absorb the short 4-cell burst.

Thus as shown in Figure 13 ATM Cell 1 is Multicasted to the 16 primary outputs 1 to 16 of the switch matrix D.

On the other hand ATM Cell 2 is applied to input port 31 of the Non-Multicast server matrix C. The cell is routed to output port 1 of matrix C, permitting the cell to enter the Multicast server matrix B via input port 32.

As previously described both the Cell's OGS and Bit mask fields are interrogated by the MB86681 devices within matrix B. In Figure 13, ATM Cell 2's OGS bit is set. This permits the cell to be Multicasted to any of the output ports 17 to 32. As a result of the bit mask status shown the cell is Multicasted to output ports 17, 31 and 32 of matrix B.

During multicast operation, the user does not have control of the cell loss threshold at which Multicast cells may be discarded. A default cell loss threshold of 80% is assumed. If no discard is required then the CLP bit must be set to zero. The user does, however, have control over queue priority. If the PC bit is set to 1 then all relay and multicast operation will use the high priority queues.

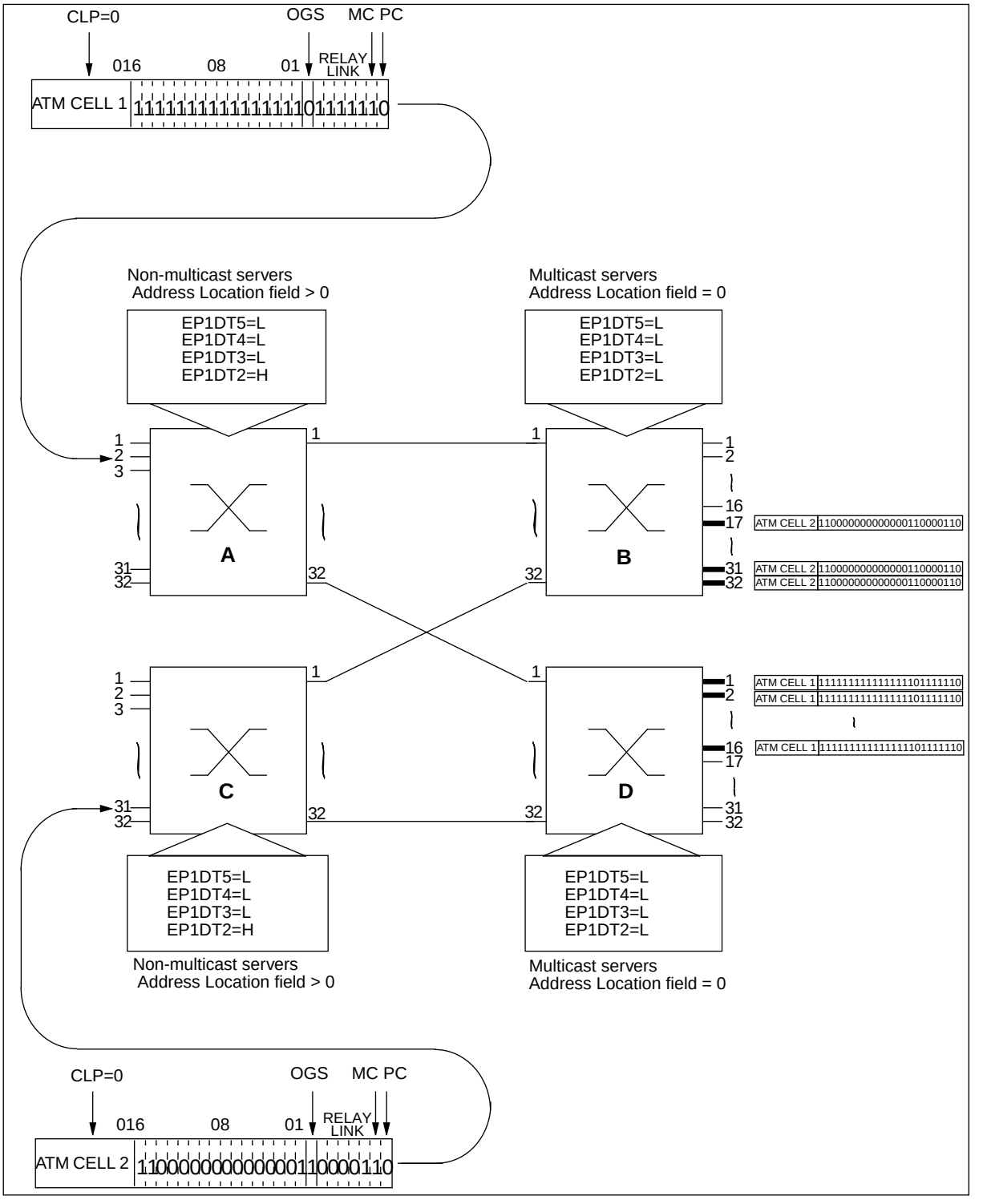



**Figure 13 Multicast Operation with a 64 x 64 Switch**

## 4.3 Explicit Forward Congestion Indication (EFCI) function

The MB86681 switch element's Explicit Forward Congestion Indication (EFCI) function is enabled when the element's internal EFCI Enable/Disable Configuration register is set to a logical "1", as described in Section 3.6.4.

When enabled, the EFCI function permits Low Priority (LP) cells exiting an output data queue to experience EFCI marking when the criteria indicating congestion are satisfied.

A LP cell will experience EFCI marking if the MSB of the PTI field in it's ATM cell header is set to a logic "0" and the fill level of the output queue from which it is **exiting** is greater than or equal to the programmed EFCI threshold configuration register value, as illustrated in Table 2.

When the above criteria for EFCI marking is met, bit 2 of the 3 bit PTI field is set to a logic "1".

**Note:**
**The MB86681 switch element does not regenerate the ATM Cell header's HEC field when it alters the PTI field.**

**No EFCI marking will be carried out on Cells that have their EFCI Threshold field set to "00" irrespective of whether the EFCI function has been enabled or not.**

**Multicast cells satisfying the criteria for EFCI marking are marked when the threshold fill level of the output data queue from which they exit exceeds or equals the 80% threshold fill level. If however the Per VC EFCI function, as explained in section 4.4 is enabled, then Multicast cells may experience EFCI marking at thresholds less than the 80% fill level.**

## 4.4 Per VC EFCI function

When configured to do so, see Section 3.6.7, the MB86681 switch elements permit Per Virtual Circuit (VC) EFCI marking to be carried out on transmitted cells, when certain programmed/user definable thresholds, are equalled or exceeded by the output queue fill levels from which the cell emerges.

Enabling the Per VC EFCI function permits the MB86681 switch elements to interpret the 3 byte routing tag in a manner different from that already mentioned in sections 4.1.1 and 4.1.2.

The interpretation of the 3 byte routing tag is dependant on the type of cell received i.e a normal cell or a Multicast cell and is detailed in the following paragraphs.

### 4.4.1 Per VC EFCI implemented on a Normal cell.

A non-Multicast cell, received by an MB86681 switch element with it's Per VC EFCI Enable / Disable register set, will be subject to EFCI marking depending on the status of the 2 least significant bits of the routing field, PA18 and PA19, and the threshold fill level of the queue from which it exits.

The EFCI marking function is only implemented when the criteria highlighted in section 4.3 are satisfied. Figure 14 illustrates the format for the routing tag of a normal ATM Cell permitting Per VC EFCI marking.

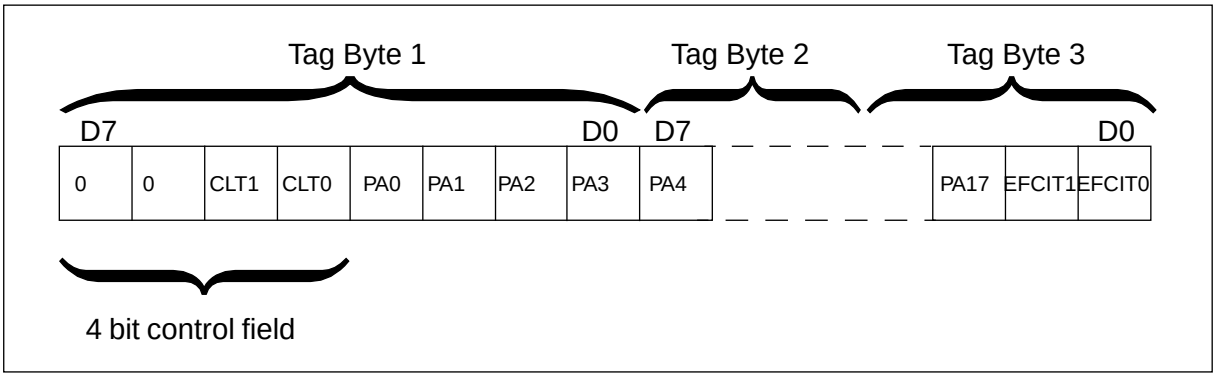



**Figure 14 Normal Routing Tag permitting Per VC EFCI Marking (EFCIT1 EFCIT0)>0**

The user definable EFCI marking Thresholds (EFCIT) should be coded in accordance with the threshold fill levels indicated in Table 7.

| EFCIT 1 | EFCIT 0 | EFCI Marking Threshold |
|---|---|---|
| 0 | 0 | No Per VC Marking |
| 0 | 1 | Output Q 20% full |
| 1 | 0 | Output Q 50% full |
| 1 | 1 | Output Q 80% full |

**Table 7 Per VC EFCI Marking Threshold Coding**

**Note:**
**The MB86681 switch elements will only interpret the routing tag in the manner described when the Per VC EFCI marking function is enabled.**

**As with the normal EFCI marking mechanism described in section 4.3, the MB86681 switch elements do not regenerate the ATM Cell header's HEC field when it alters the PTI field.**

**No Per VC EFCI marking will be carried out on Cells that have their EFCI Threshold field set to "00" irrespective of whether the Per VC EFCI function has been enabled or not.**

**However, it should be noticed that EFCI marking may be carried out on the aforementioned cell if the normal EFCI function is enabled and the conditions for EFCI marking are satisfied.**

**The other fields of the 3 byte routing tag are interpreted in their normal manner as previously described in section 4.1.1.**

## 4.4.2 Per VC EFCI implemented on a Multicast cell.

The MB86681 switch element provides two Per VC EFCI mechanisms for the marking of Multicast cells. Both mechanisms are enabled by setting the Per VC EFCI Enable / Disable control register during initialization. The choice of method used to carry out Per VC EFCI marking on a Multicast cell is dependant on whether the device is configured as a **Multicast server** or as a **Non Multicast server**.

### Non-Multicast Server mode.

When an MB86681 switch element is configured as a Non Multicast server it's Address Field Location register is set to a value greater than zero. The switch element will only carry out Per VC EFCI marking when the most significant bit of the Multicast Cell's Relay Link Address is set to "1", as shown in Figure 15, and the fill level of the Output data queue from which the cell emerges is greater than or equal to the value programmed into the switch element's Per VC EFCI Fixed Threshold register.

No Per VC EFCI marking will be carried out on Multicast cells when the Per VC EFCI Fixed Threshold register is set to "00" irrespective of whether the Per VC EFCI function has been enabled or not.
However, it should be noticed that EFCI marking may be carried out on the aforementioned cell if the normal EFCI function is enabled and the conditions for EFCI marking are satisfied.

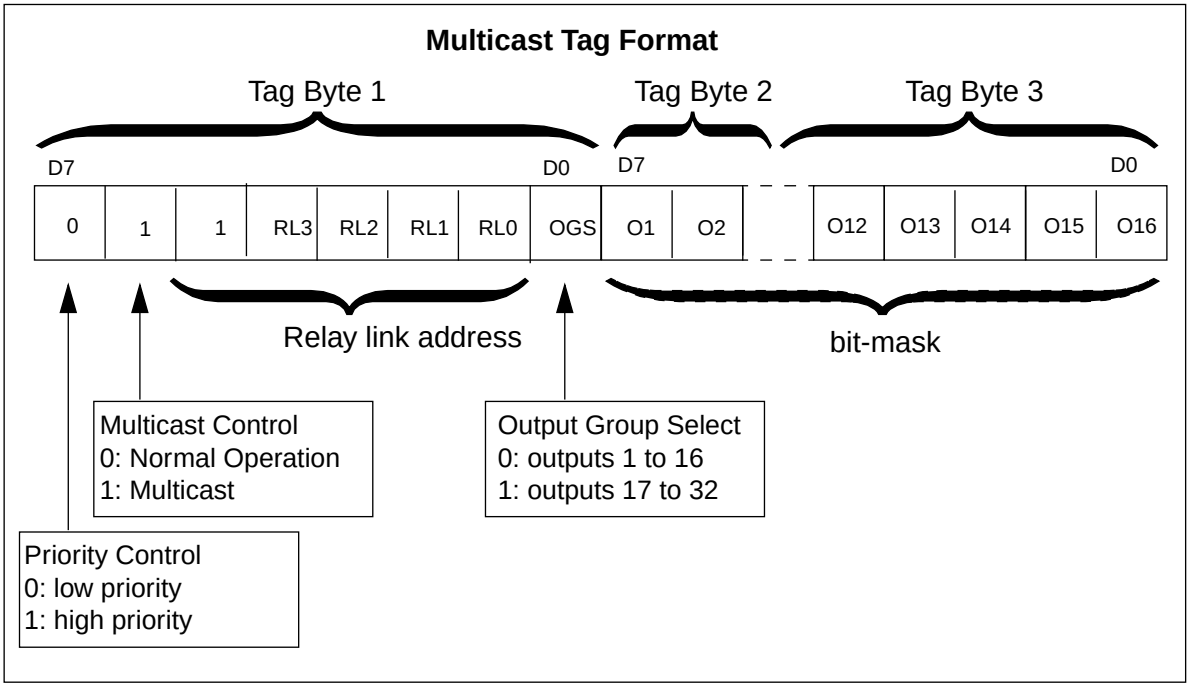



**Figure 15 Non-Multicast Server Routing Tag permitting Per VC EFCI Marking**

**Note:**
**As with the normal EFCI marking mechanism described in section 4.3, the MB86681 switch elements do not regenerate the ATM Cell header's HEC field when it alters the PTI field.**

**When MB86681 switch elements are configured as Non-Multicast servers with Per VC EFCI marking enabled, the maximum permissible switch matrix size is 16 X 16.**

### Multicast Server mode.

When MB86681 switch elements are configured as Multicast servers the Per VC EFCI marking function is only implemented on Multicast cells when the user definable EFCI Threshold field, as specified by the 2 most significant bits of the normal Relay Link Address field, as shown in Figure 16, is greater than or equal to the threshold fill level of the Output queue from which the cell emerges.

No Per VC EFCI marking will be carried out on Multicast cells when the Per VC EFCI Threshold field is set to "00" irrespective of whether the Per VC EFCI function has been enabled or not.
However, it should be noticed that EFCI marking may be carried out on the aforementioned cell if the normal EFCI function is enabled and the conditions for EFCI marking are satisfied.

The EFCI Threshold field is encoded in accordance with the contents of Table 7.

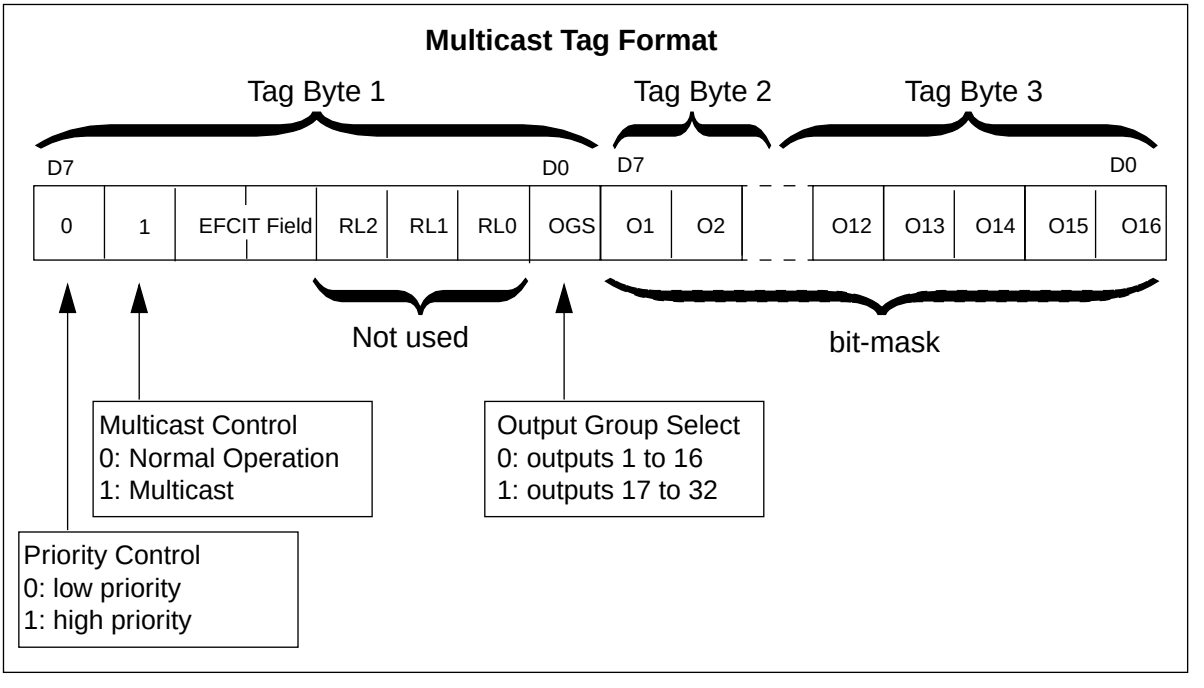



**Figure 16 Multicast Server Routing Tag permitting Per VC EFCI Marking**

## 4.5 Vertical Flow Control

Unlike it's predecessor, the MB86680B, the MB86681 provides flow control information for each output queue. The flow control mechanism permits the implementation of a relatively simple input and output buffering technique at the edge of the switch matrix whilst at the same time guaranteeing no undesired cell loss once a cell has been routed.

As outlined earlier in section 2.2, the flow control information is transferred serially to the next vertically opposite switch element using the VFCI and VFCO pins. Flow control information transmitted on this local serial highway shall be delimited by SYN characters as defined in CCITT international alphabet No. 5. Figure 17 shows the per queue flow control format and Figure 18 shows the MB86681 switch element flow control interconnection for a Master / Slave switch fabric. Identical connections are also used in all Slave fabrics.

Once enabled, the Output buffer flow control mechanism permits flow control on a cell by cell basis. The flow control mechanism is activated once the predefined Output queue's fill level threshold has been reached, see section 3.6.10 and Table 4. The Output queue's flow control signal remains in it's active state until the Output queue's fill level falls below the programmed flow control fill level threshold.

On activating the Output queue flow control signal an MB86681 switch element's vertically opposite neighbour will cease cell transmission from the corresponding Output data queue until the received Output queues flow control signal is de-activated.

If an MB86681 switch element receives an active Output queue flow control from it's vertically opposite neighbour whilst it is in the process of transmitting a cell to this neighbour, the transmitting switch element will complete the transmission of the cell before responding to the flow control request.

When configured with a single Output buffer per port, the MB86681 switch element uses the Low priority queue flow control bits to flow control it's vertically opposite neighbour.

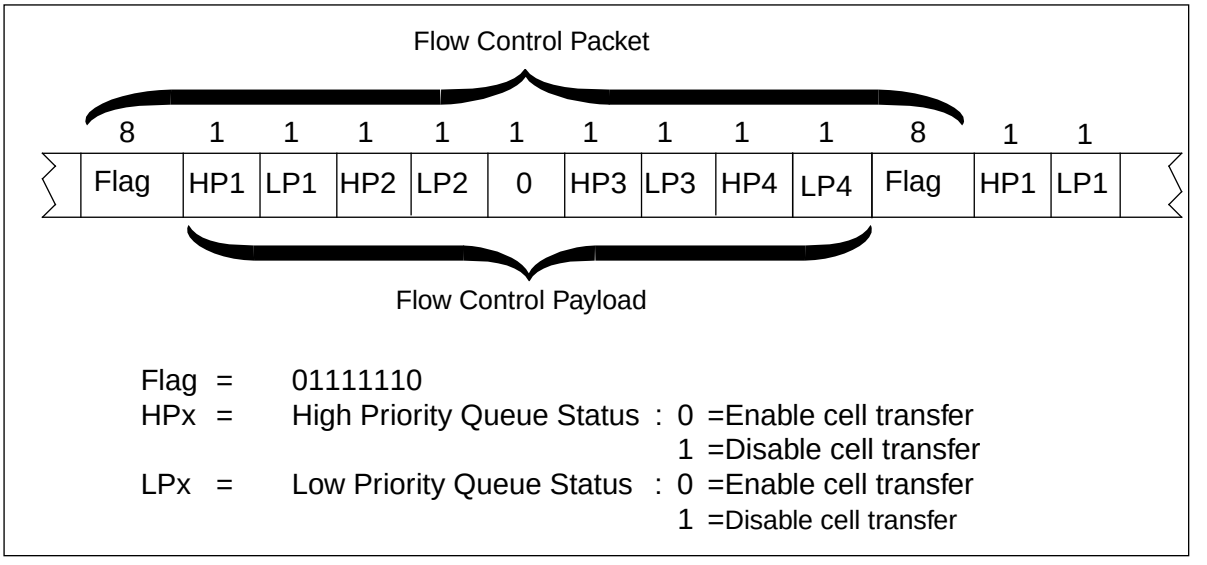



**Figure 17 Flow Control Packet**

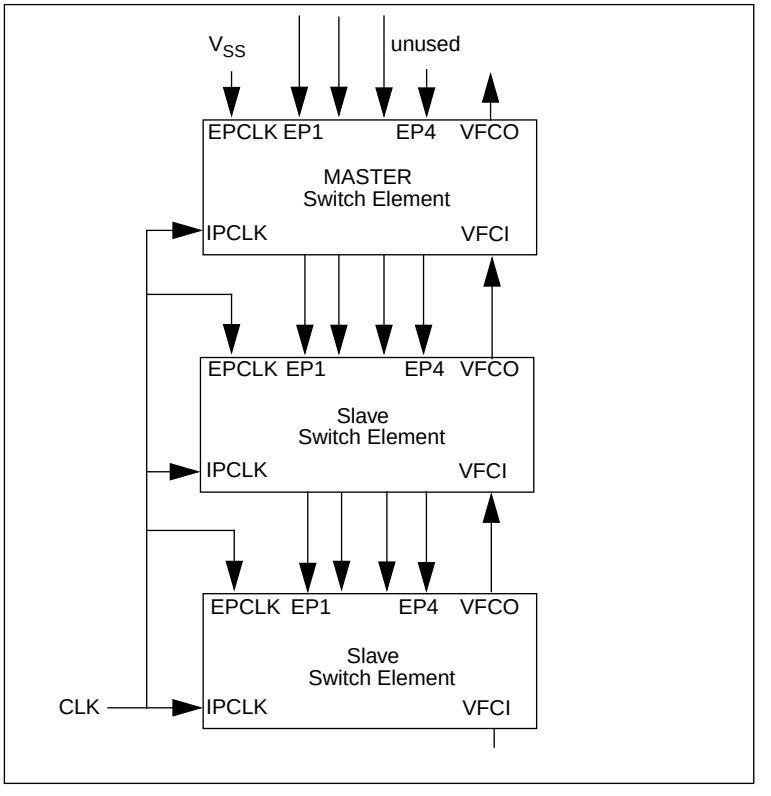



**Figure 18 Serial Flow Control connectivity example**

## 4.6 Early Packet Discard Notification.

The MB86681 switch element provides Early Packet Discard (EPD) notification ports. The 4 EPD ports permit direct communication with EPD mechanisms operating at the ingress side of the switch fabric.
The EPD notification takes the form of an active low transition on the respective EPD port. An active low transition on an EPD port will result when either a selective cell discard or buffer overflow condition results on a cell currently being received at one of the MB86681's I-input ports.

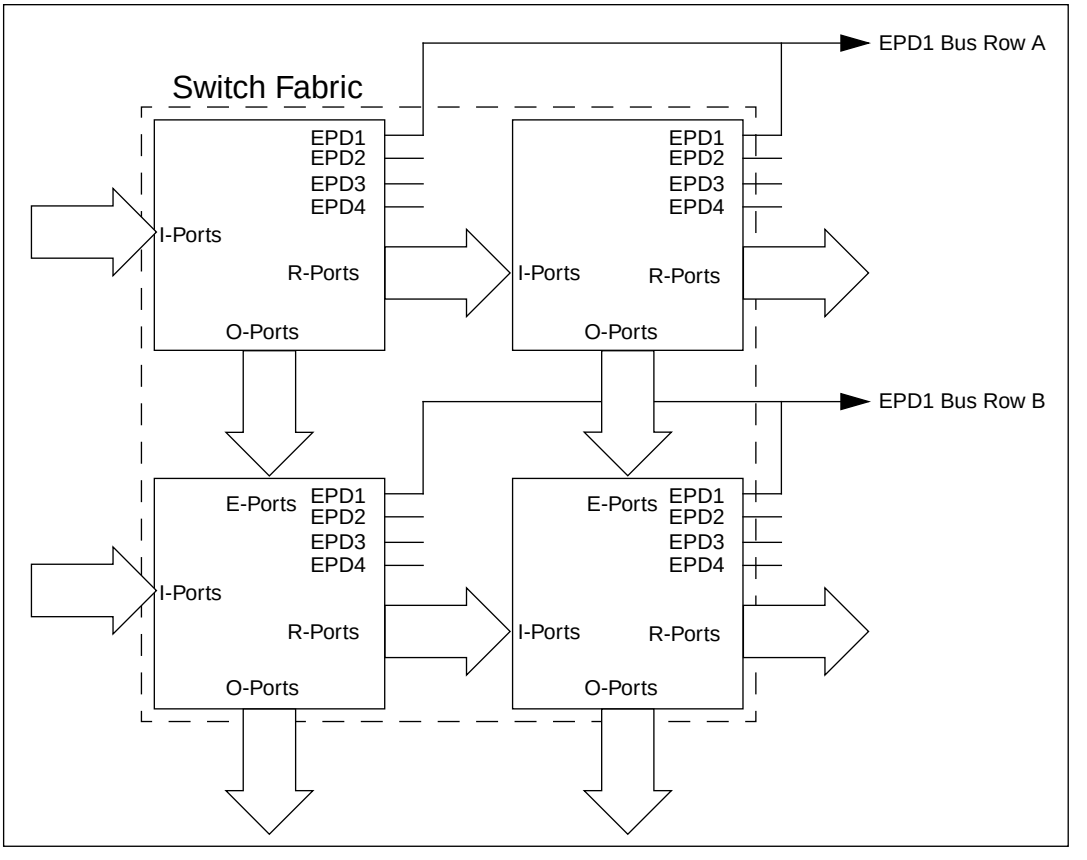



**Figure 19 EPD1 Bus connectivity**

When a cell currently being received on a switch element's I1 input port is discarded, the respective EPD port, namely, EPD1, is driven to it's active low position for the duration of one IPCLK clock period.
The 4 tristate EPD ports permit bus connectivity across the row of a switch fabric as shown in Figure 19.

EPD notification will take place within 20 IPCLK clock cycles from the cell data first being presented to an MB86681's I-input port. As a consequence the discarding of a cell can be notified before the full cell has been received by the MB86681 switch element.

Transitions on the EPD ports take place with respect to the rising edge of the IPCLK clock signal.

# 4.7 JTAG

## 4.7.1 Introduction

This device contains Boundary Scan Test Circuitry compliant with IEEE 1149.1 (JTAG). This requires the addition of the 5 pins identified below. See Appendix C for a full BSDL description.

The JTAG circuitry allows easier board level testing by allowing the signal pins on the device to form a serial scan chain around the device. The test modes are controlled by accessing an internal Test Access Port Controller (TAP), which is in turn controlled from the TAP.

## 4.7.2 Test Access Port (TAP)

Five pins are dedicated to JTAG:TDO; TDI; TMS; TRST & TCK.
The functions of these signals are described in Section 2.2 of this datasheet.

# 4.8 Test Instructions

The following JTAG instructions are implemented:-

BYPASS
SAMPLE/PRELOAD
EXTEST
INTEST.

**BYPASS**
The BYPASS instruction is used to bypass a component that is connected in series with other components. This allows more rapid movement of test data through the components of the board, bypassing the ones that do not need to be tested. The BYPASS operation enables the bypass register, which is a single stage shift register, between TDI and TDO

1. The binary code for the BYPASS instruction is “11”.

2. The BYPASS instruction is forced into the instruction register output latches during the Test_Logic_Reset state. Note the distinction between the “01” content of the instruction shift register and the “11” of the instruction register output latch. Therefore, at the start of the instruction-shift cycle, a “01” pattern will be seen instead of “11”.

3. The BYPASS operation does not interfere with the component operation at all. If the TDI input trace to the component is somehow disconnected, the test logic will see a “11” at TDI input during the instruction-shift state. Therefore, no unwarranted interference with the on-chip system logic occurs.

**SAMPLE/PRELOAD**
The SAMPLE/PRELOAD instruction is used to sample the state of the component pins. The sampled values can be examined by shifting out the data through TDO. This instruction selects the boundary scan-cell output latches with specific values. The preloaded values are then enabled to the output pins by the EXTEST.

1. The binary code for the instruction is “01”.

2. The SAMPLE/PRELOAD instruction selects the boundary-scan cells to be connected between TDI and TDO in the Shift_DR TAP controller state.

3. The values of the component pins are sampled on the rising edge of TCK in the Capture_DR TAP controller state.

4. The preload values shifted in the boundary scan cells are latched into the boundary-scan output latch at the falling edge of TCK in the Update_DR TAP controller state.

**EXTEST**

The EXTEST instruction allows testing of off-chip circuitry and board level interconnections. The PRELOAD /SAMPLE instruction is used to preload the data into the latched parallel outputs of the boundary-scan shift register stages. Then, the EXTEST instruction enables the preloaded values to the components output pins.

1. The binary code for the instruction is “00”.

2. The device outputs the preloaded data to the pins at the falling edge of TCK in the Update_IR TAP controller state at which point the JTAG instruction register is updated with the EXTEST.

3. The EXTEST instruction selects the boundary-scan cells to be connected between TDI and TDO in the SHIFT-DR test logic controller state.

4. Once the EXTEST instruction is effective, the output pins can change at the falling edge of TCK in the Update_DR TAP controller state.

**INTEST**

This instruction allows testing of the on-chip system logic. Test stimuli are shifted in, one at a time, and applied to the on-chip logic. The test results are captured into the boundary scan register (BSR) and are examined by subsequent shifting. The PRELOAD/SAMPLE instruction is used to preload the data into the latched parallel outputs of the boundary-scan shift register stages prior to INTEST being selected.
The binary code for the instruction is “10”.

# 5 Developers Notes

## 5.1 External Interfaces

External interfaces of the switch element are illustrated in Figure 3 and are described in the following paragraphs.

### 5.1.1 ATM Cell Structure

The structure of an ATM cell is illustrated in Figure 20. The only bit in the cell that is processed by the MB86681 switch element is the CLP bit. This bit is used to determine whether a cell should be discarded when the output queue fill level exceeds a programmable threshold.

Note: When EFCI functions are disabled, none of the bits in an ATM cell will be modified by the MB86681 switch elements. The switch elements will not discard idle cells; it is assumed that idle cells will be discarded before data is applied to the switch (e.g. by the FUJITSU Network Termination Controller).

### 5.1.2 External Data Structure

All input/output data for the MB86681 switch elements is comprised of 8 data bits together with a Start of Cell (SOC) bit and a clock signal. The data for one cell period comprises a 3 byte tag field followed by a 53 byte ATM cell. The cell stream may be continuous or discontinuous.

In both cases the SOC bit marks the first tag byte associated with a cell period. The clock rate should be selected to be as close as possible to 56/53 X ATM cell data rate. For SDH STM-1 applications a value of 155.52MHz / 8 provides a good match.

A diagram of the external data interface format for both Fujitsu Cell Steam (FCS) and the Inverse FCS (IFCS) modes of operation is illustrated in Figure 21.

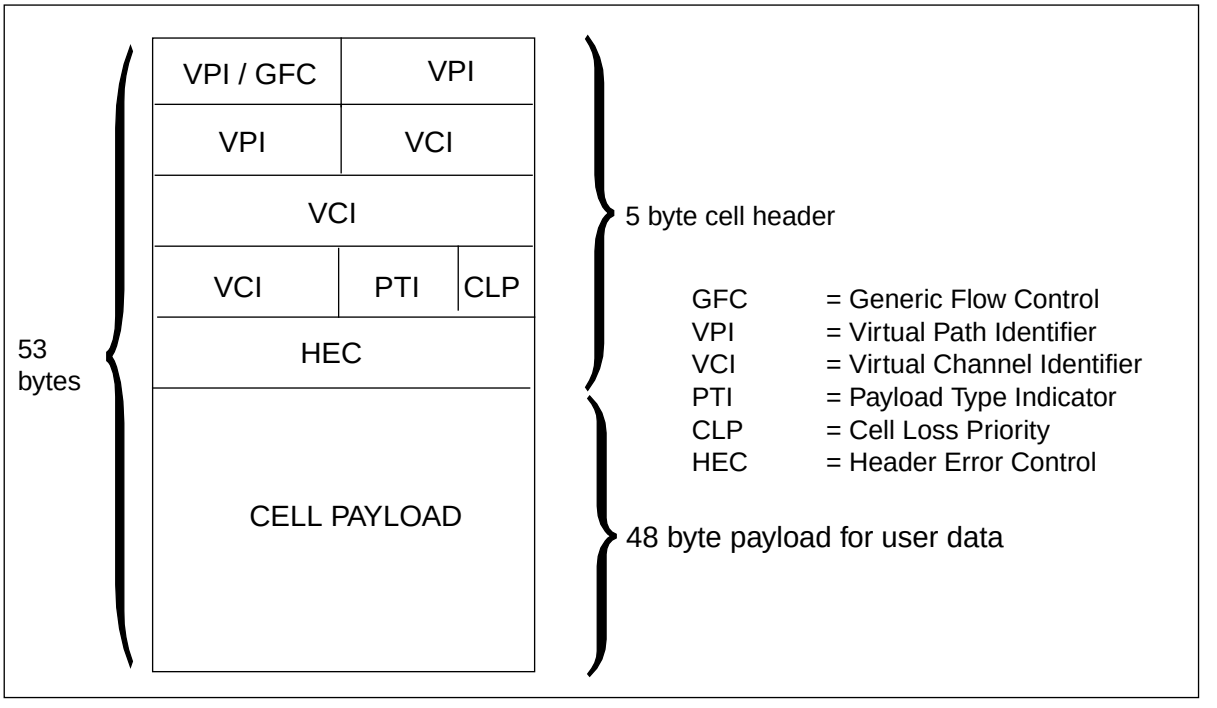



**Figure 20 ATM Cell Header Structure**

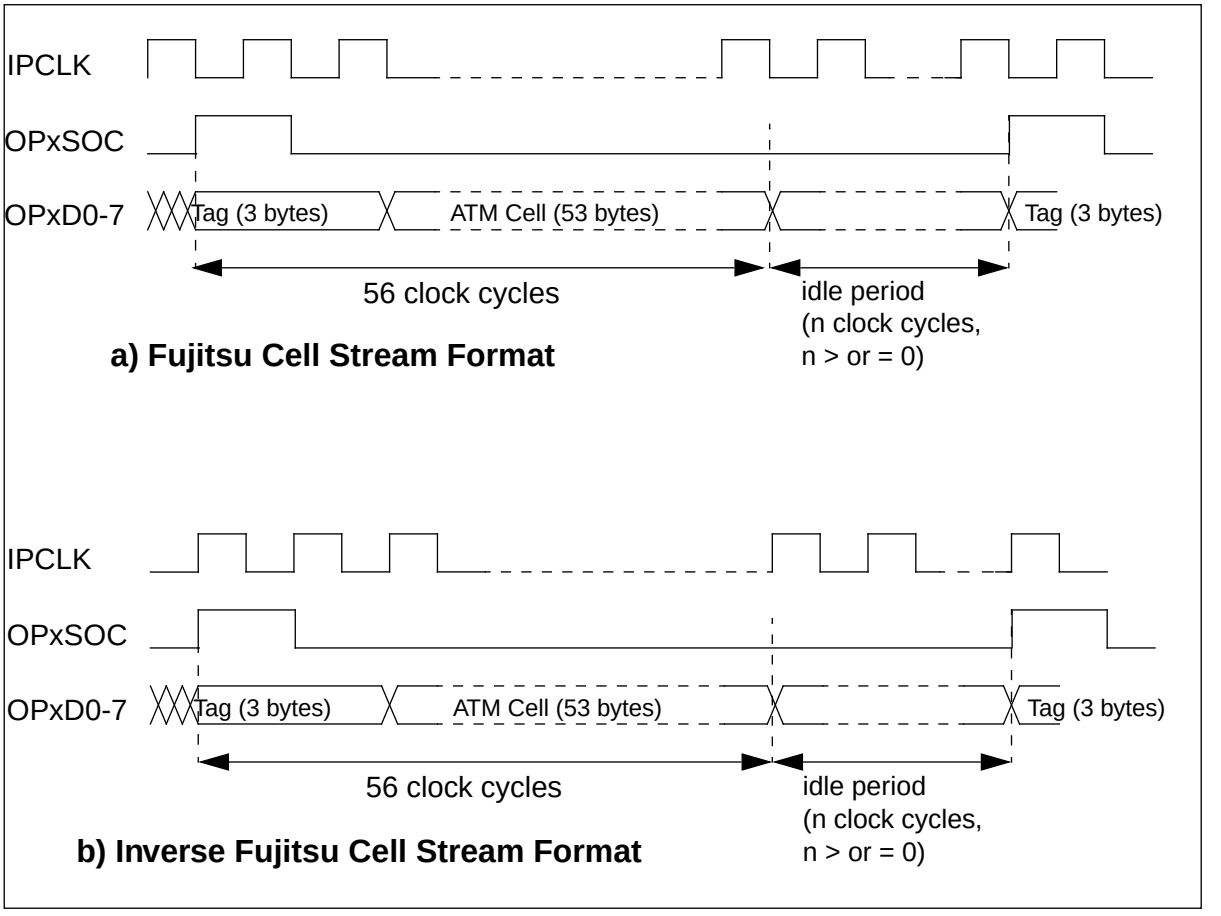



**Figure 21 Cell Stream Transmission Timing**

# A Electrical Specification

## A.1 Absolute Maximum Ratings

| Parameter | Symbol | Values | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| Positive Supply Voltage | $+V_{D5}$ | $V_{SS}$-0.5 | 6.0 | V |
| Positive Supply Voltage | $+V_{D3}$ | $V_{SS}$-0.5 | 4.0 | V |
| Input Voltage | $V_{DIN}$ | $V_{SS}$-0.5 | $V_{D5}$+0.5 | V |
| Output Voltage | $V_{O1}$ | $V_{SS}$-0.5 | $V_{D5}$+0.5 | V |
| Storage Temperature | $T_{STG}$ | -55 | +125 | $^oC$ |
| Operating Temperature | $T_A$ | 0 | +70 | $^oC$ |

## A.2 Recommended Operating Conditions

| Parameter | Symbol | Ratings | | | Units |
|---|---|---|---|---|---|
| | | Min | Typ. | Max | |
| Positive Supply Voltage (for 5V interface) | $+V_{D5}$ | 4.5 | 5.0 | 5.5 | V |
| Positive Supply Voltage (for 3V interface) | $+V_{D3}$ | 3.0 | 3.3 | 3.6 | V |

# A.3 DC Characteristics

| Parameter | Symbol | Test Condition | Ratings | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ. | Max | |
| Positive Supply Current | $I_{DDS}$ | Static no load | -2.0 | - | 2.0 | mA |
| Input High Voltage (TTL) | $V_{IH}$ | - | $V_{D3}$x0.65 | - | $V_{D5}$ | V |
| Input Low Voltage (TTL) | $V_{IL}$ | - | $V_{SS}$ | - | $V_{D3}$x0.2 | V |
| Low Level Output Voltage | $V_{OL}$ | $I_{OL}$=+4.0mA | $V_{SS}$ | - | 0.4 | V |
| High Level Output Voltage | $V_{OH}$ | $I_{OH}$=-4.0mA | $V_{D3}$-0.5 | - | $V_{D5}$ | V |
| Input Leakage Current | $I_{LI}$ | 0<=Vi<=$V_{D5}$ | -5 | - | 5 | µA |
| Input/Output Pin Capacitance | $C_{IN/OUT}$ | - | - | - | 18 | pF |
| Operating Current (normal) | $I_{DD3}$ | - | - | - | 310 | mA |
| | $I_{DD5}$ | | | | 60 | mA |
| Power Dissipation (operating) | $P_{O3}$ | - | - | - | 1.03 | W |
| | $P_{O5}$ | | | | 0.33 | W |

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.
Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.
No warranty is made with respect to uses , operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

# B AC Characteristics

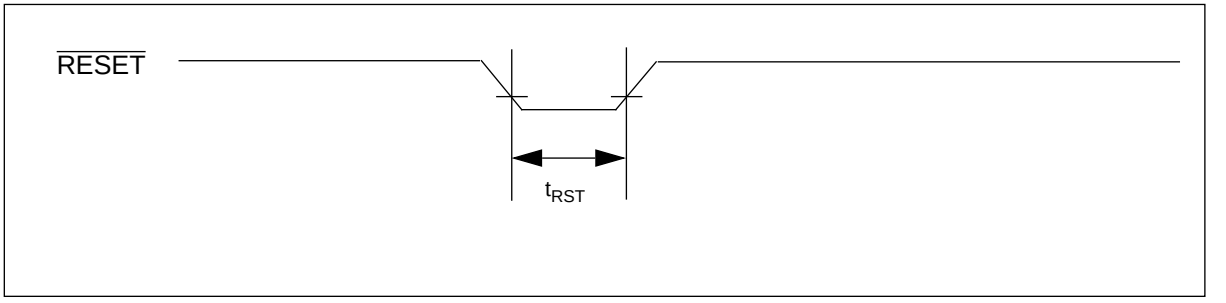



**Figure 22 Reset Timing**

| Parameter | Ref. Signal | Abbrev. | Values | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typical | Max | |
| Reset Pulse Width | $\overline{RESET}$ | $t_{RST}$ | 7 | - | - | ns |

**Table 8 Reset AC Timing Parametrics**

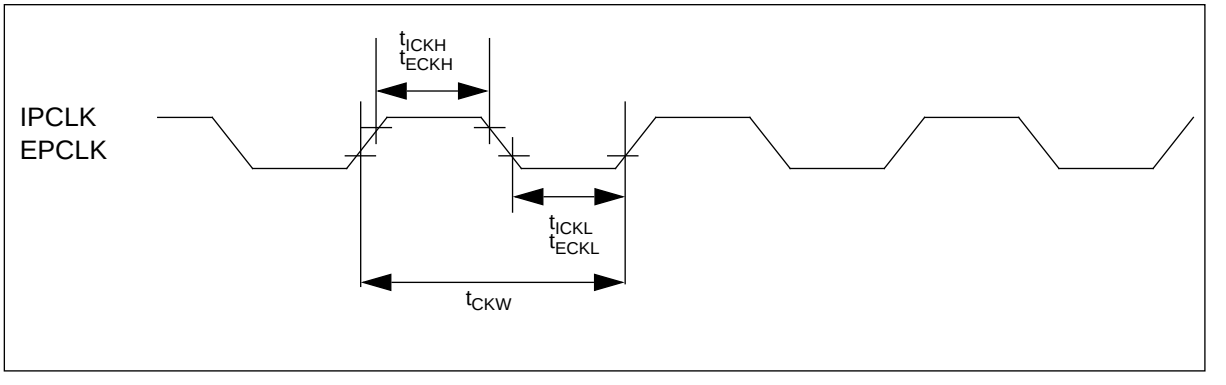



**Figure 23 Input Clock Timing**

| Parameter | Ref. Signal | Abbrev. | Values | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typical | Max | |
| IPCLK High time | IPCLK | $t_{ICKH}$ | 8 | - | - | ns |
| EPCLK High time | EPCLK | $t_{ECKH}$ | 8 | - | - | ns |
| IPCLK Low time | IPCLK | $t_{ICKL}$ | 8 | - | - | ns |
| EPCLK Low time | EPCLK | $t_{ECKL}$ | 8 | - | - | ns |
| IP/EPCLK Frequency | | $t_{CKW}$ | - | - | 40 | MHz |

**Table 9 IPCLK/EPCLK AC Timing Parameters**

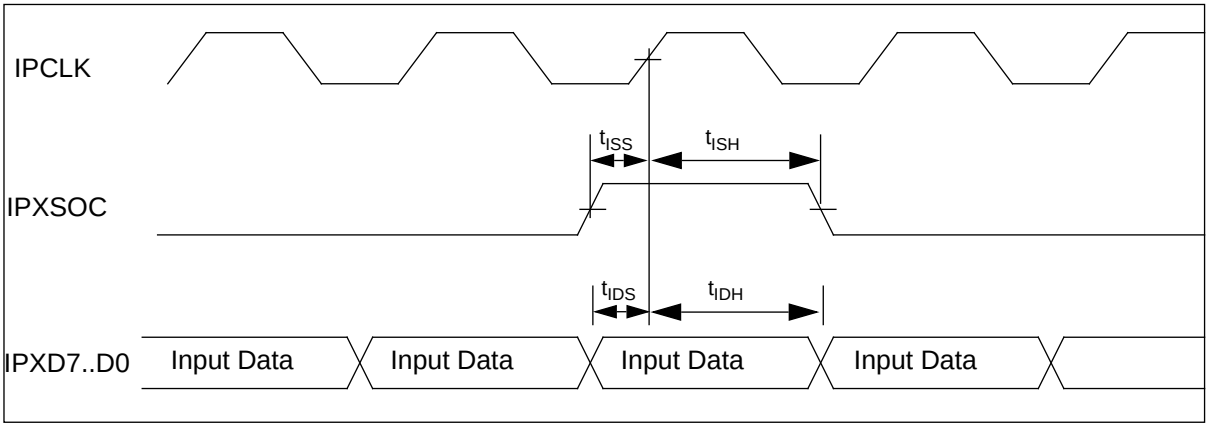



**Figure 24 I-Input Port Timing**

| Parameter | Ref. Signal | Abbrev. | Values | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typical | Max | |
| IPXSOC Data Setup Time | IPCLK | $t_{ISS}$ | 2 | - | - | ns |
| IPXSOC Data Hold Time | IPCLK | $t_{ISH}$ | 3 | - | - | ns |
| IPXD7..D0 Data Setup Time | IPCLK | $t_{IDS}$ | 2 | - | - | ns |
| IPXD7..D0 Data Hold Time | IPCLK | $t_{IDH}$ | 3 | - | - | ns |

**Table 10 I-Input Port AC Timing Parameters**

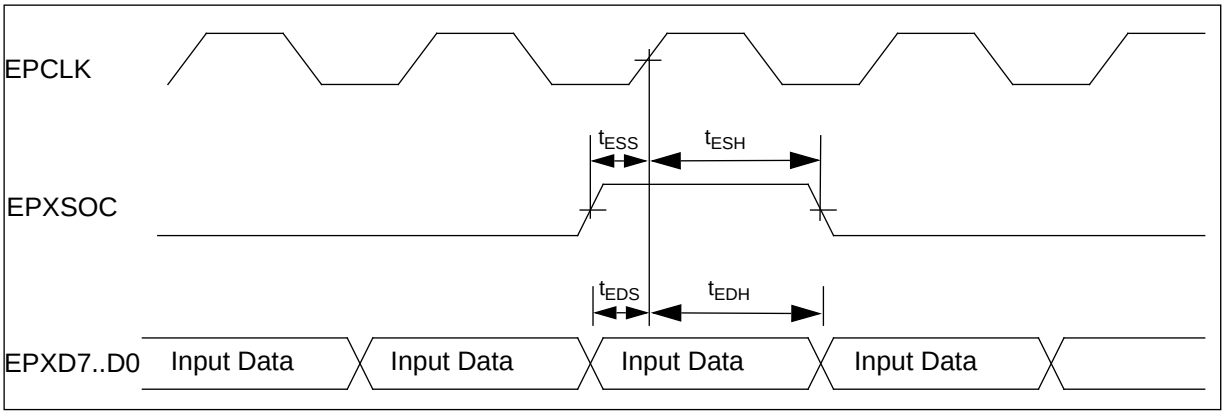



**Figure 25 E-Input Port Timing**

| Parameter | Ref. Signal | Abbrev. | Values | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typical | Max | |
| EPXSOC Data Setup Time | EPCLK | $t_{ESS}$ | 3 | - | - | ns |
| EPXSOC Data Hold Time | EPCLK | $t_{ESH}$ | 2 | - | - | ns |
| EPXD7..D0 Data Setup Time | EPCLK | $t_{EDS}$ | 3 | - | - | ns |
| EPXD7..D0 Data Hold Time | EPCLK | $t_{EDH}$ | 2 | - | - | ns |

**Table 11 E-Input Port AC Timing Parameters**

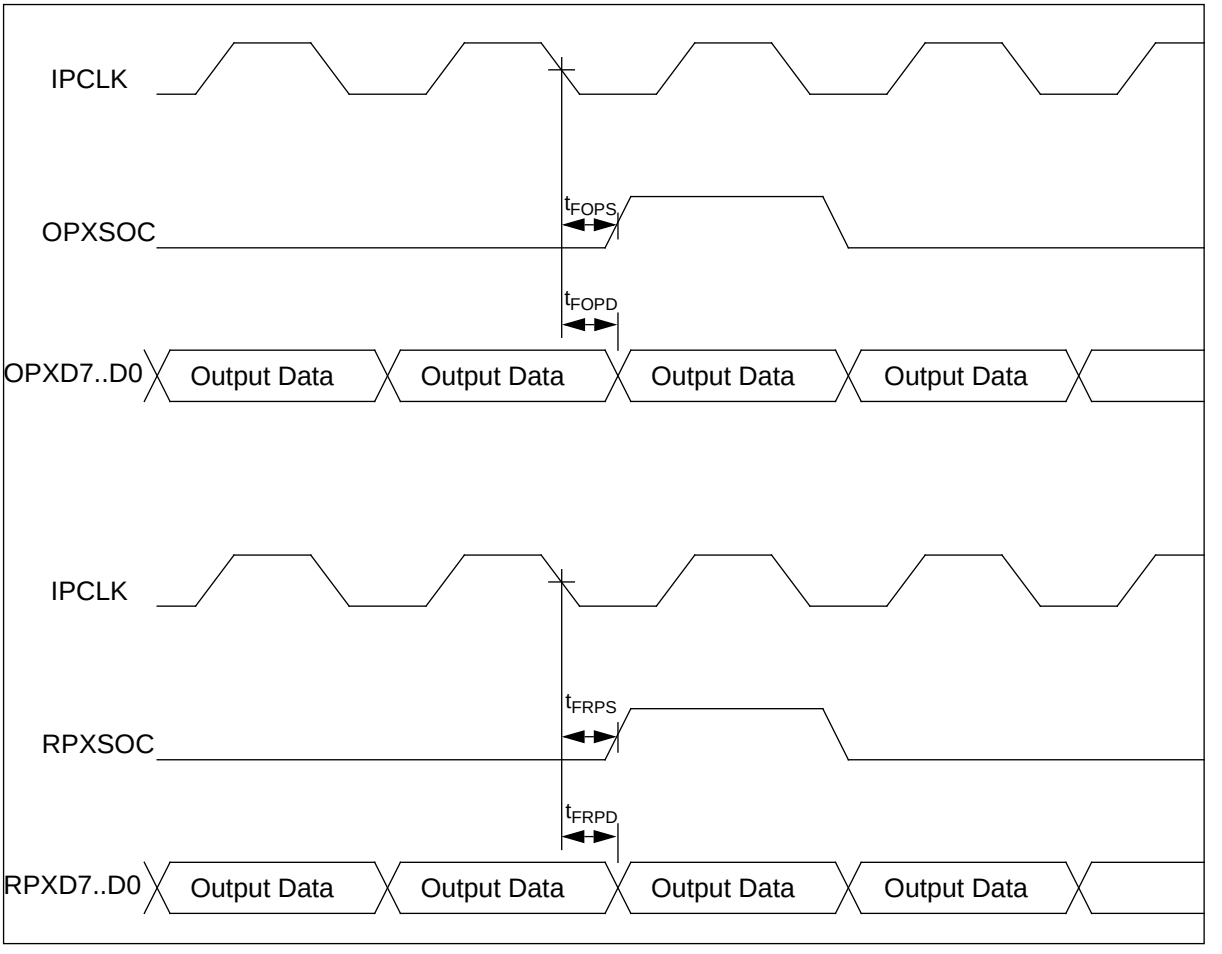



**Figure 26 Output Port Timing-FCS**

| Parameter | Ref. Signal | Abbrev. | Values | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typical | Max | |
| OPXSOC output delay | IPCLK | $t_{FOPS}$ | 3 | - | 20 | ns |
| OPXD7..D0 output delay | IPCLK | $t_{FOPD}$ | 5 | - | 20 | ns |
| RPXSOC output delay | IPCLK | $t_{FRPS}$ | 3 | - | 20 | ns |
| RPXD7..D0 output delay | IPCLK | $t_{FRPD}$ | 3 | - | 20 | ns |

**Table 12 Output Port FCS Mode AC Timing Parameters**

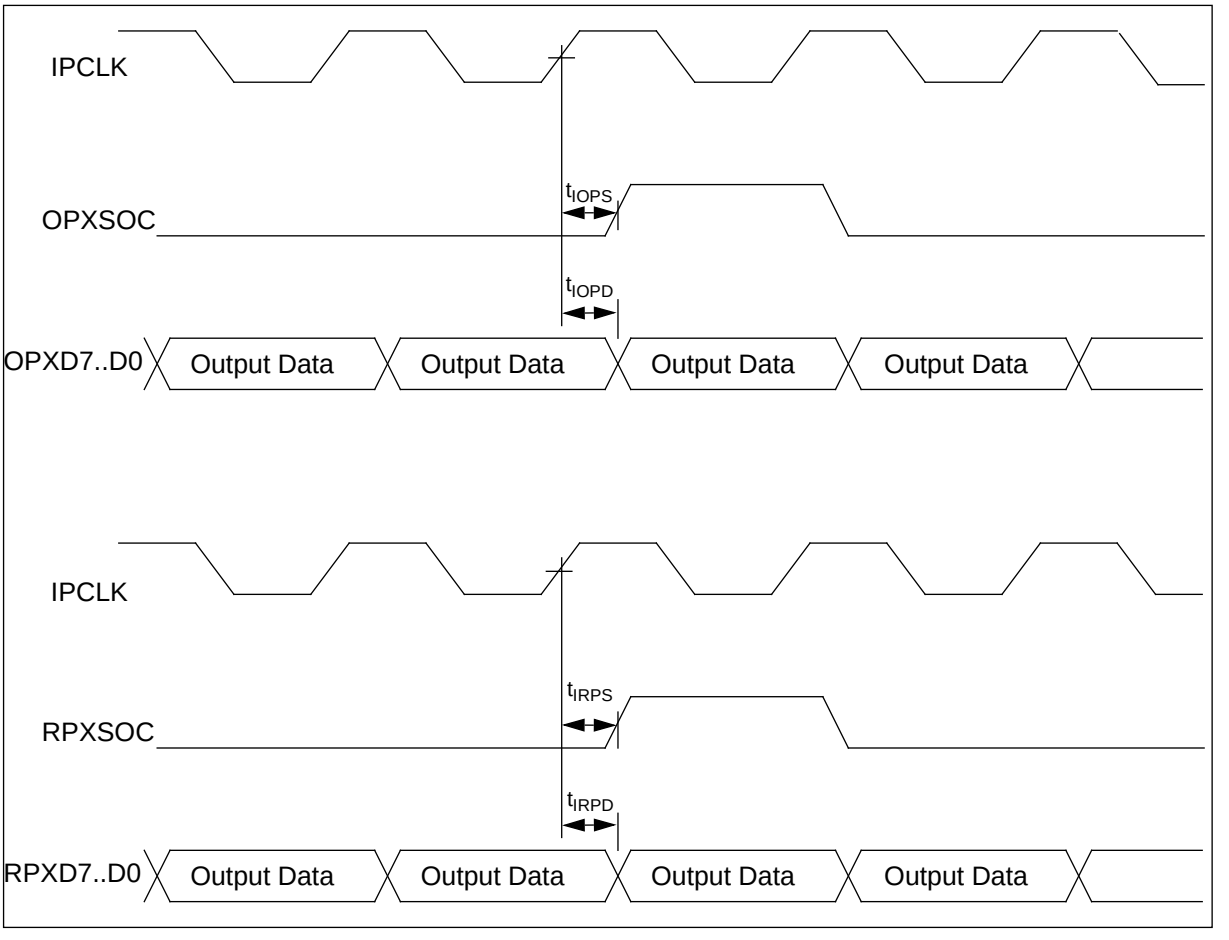



**Figure 27 Output Port Timing-IFCS Mode**

| Parameter | Ref. Signal | Abbrev. | Values | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typical | Max | |
| OPXSOC output delay | IPCLK | $t_{IOPS}$ | 4 | - | 20 | ns |
| OPXD7..D0 output delay | IPCLK | $t_{IOPD}$ | 4 | - | 20 | ns |
| RPXSOC output delay | IPCLK | $t_{IRPS}$ | 3 | - | 20 | ns |
| RPXD7..D0 output delay | IPCLK | $t_{IRPD}$ | 3 | - | 20 | ns |

**Table 13 Output Port IFCS Mode AC Timing Parameters**

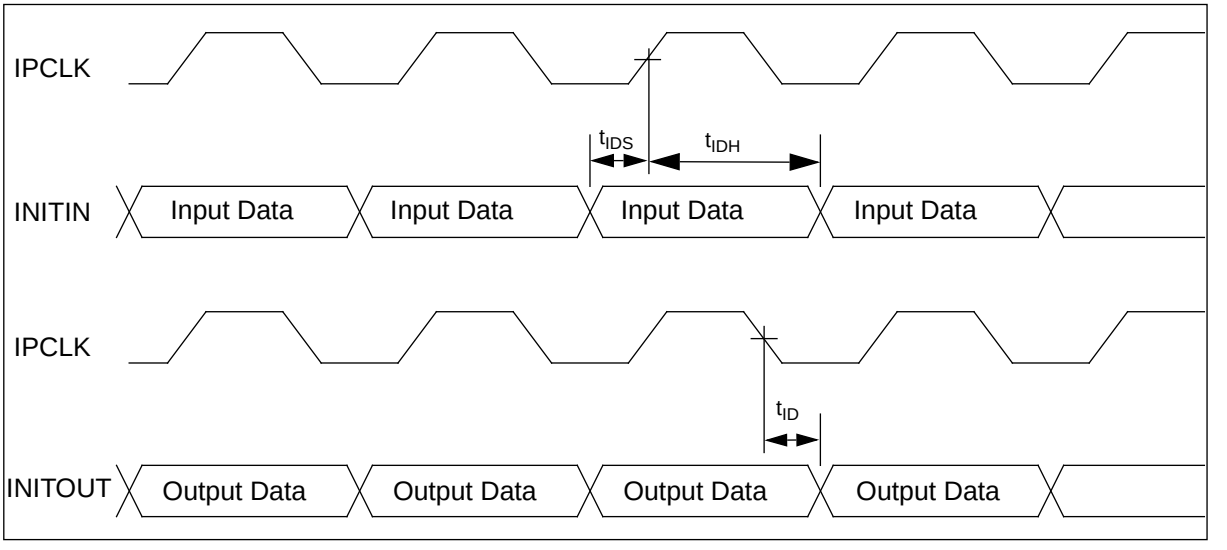



**Figure 28 INIT Port Timing**

| Parameter | Ref. Signal | Abbrev. | Values | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typical | Max | |
| INITIN Data Setup Time | IPCLK | $t_{IDS}$ | 1 | - | - | ns |
| INITIN Data Hold Time | IPCLK | $t_{IDH}$ | 2 | - | - | ns |
| INITOUT Output Delay | IPCLK | $t_{ID}$ | 3 | - | 20 | ns |

**Table 14 INIT Port AC Timing Parameters**

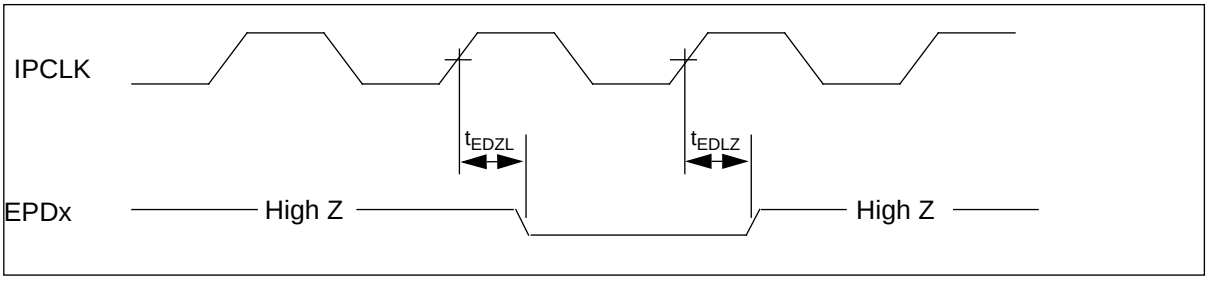



**Figure 29 EPD Port Timing**

| Parameter | Ref. Signal | Abbrev. | Values | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typical | Max | |
| EPD Port Delay (Z-L) | IPCLK | $t_{EDZL}$ | 3 | - | 18 | ns |
| EPD Port Delay (L-Z) | IPCLK | $t_{EDLZ}$ | 8 | - | 20 | ns |

**Table 15 EPD Port AC Timing Parameters**

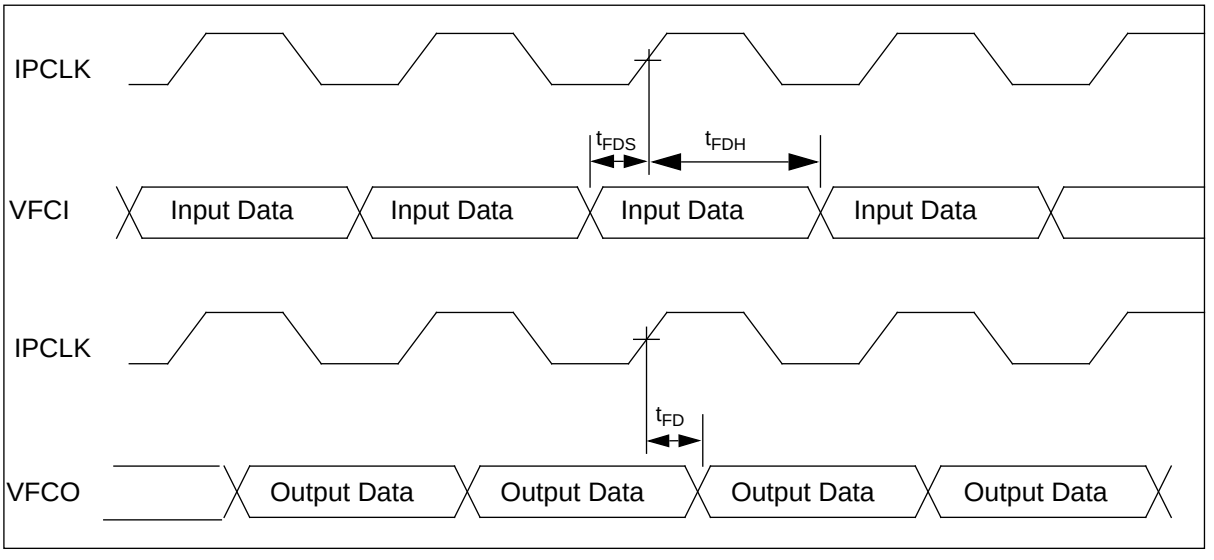



**Figure 30 Vertical Flow Control Port Timing**

| Parameter | Ref. Signal | Abbrev. | Values | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typical | Max | |
| VFCI Data Setup Time | IPCLK | $t_{FDS}$ | 4 | - | - | ns |
| VFCI Data Hold Time | IPCLK | $t_{FDH}$ | 1 | - | - | ns |
| VFCO Out Delay | IPCLK | $t_{FD}$ | 4 | - | 18 | ns |

**Table 16 Vertical Flow Control Port AC Timing Parameters**

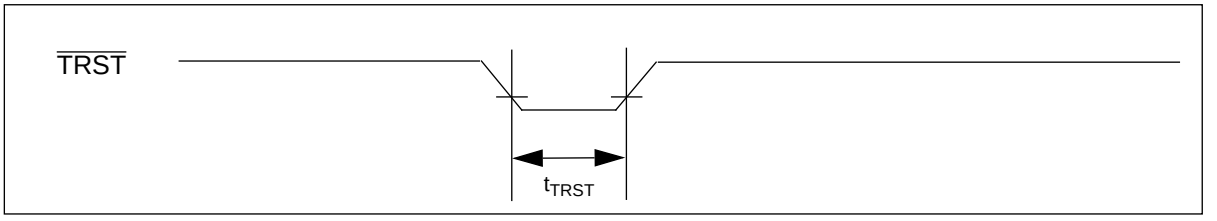



**Figure 31 JTAG Port TRST Timing**

| Parameter | Ref. Signal | Abbrev. | Values | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typical | Max | |
| JTAG TRST Pulse Width | $\overline{TRST}$ | $t_{TRST}$ | 10 | - | - | ns |

**Table 17 JTAG TRST AC Parameters**

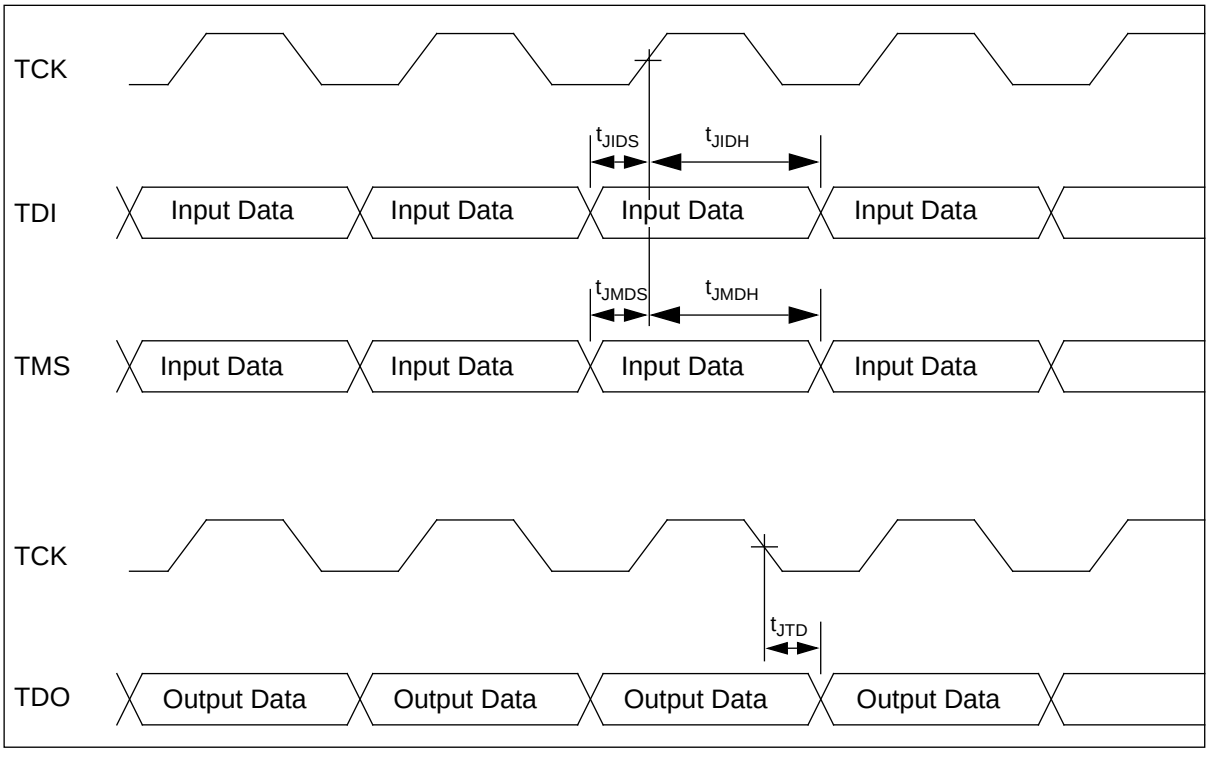



**Figure 32 JTAG Port Timing**

| Parameter | Ref. Signal | Abbrev. | Values | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typical | Max | |
| JTAG TMS Data Setup Time | TCK | $t_{JMDS}$ | 0 | - | - | ns |
| JTAG TMS Data Hold Time | TCK | $t_{JMDH}$ | 1 | - | - | ns |
| JTAG TDI Data Setup Time | TCK | $t_{JIDS}$ | 0 | - | - | ns |
| JTAG TDI Data Hold Time | TCK | $t_{JIDH}$ | 3 | - | - | ns |
| JTAG TDO Out Delay | TCK | $t_{JTD}$ | 3 | - | 20 | ns |

**Table 18 JTAG Port AC Timing Parameters**

**NOTE:**
All timings are characterized over the temperature range $0^0$ to $70^0$ Centigrade for device operation up to and including 40MHz.

# C JTAG Boundary Scan Description

A BSDL description for the MB86681 may be downloaded from the following web site :

http://www.fml.co.uk/

# D Pin Assignments

## D.1 Pin Diagram

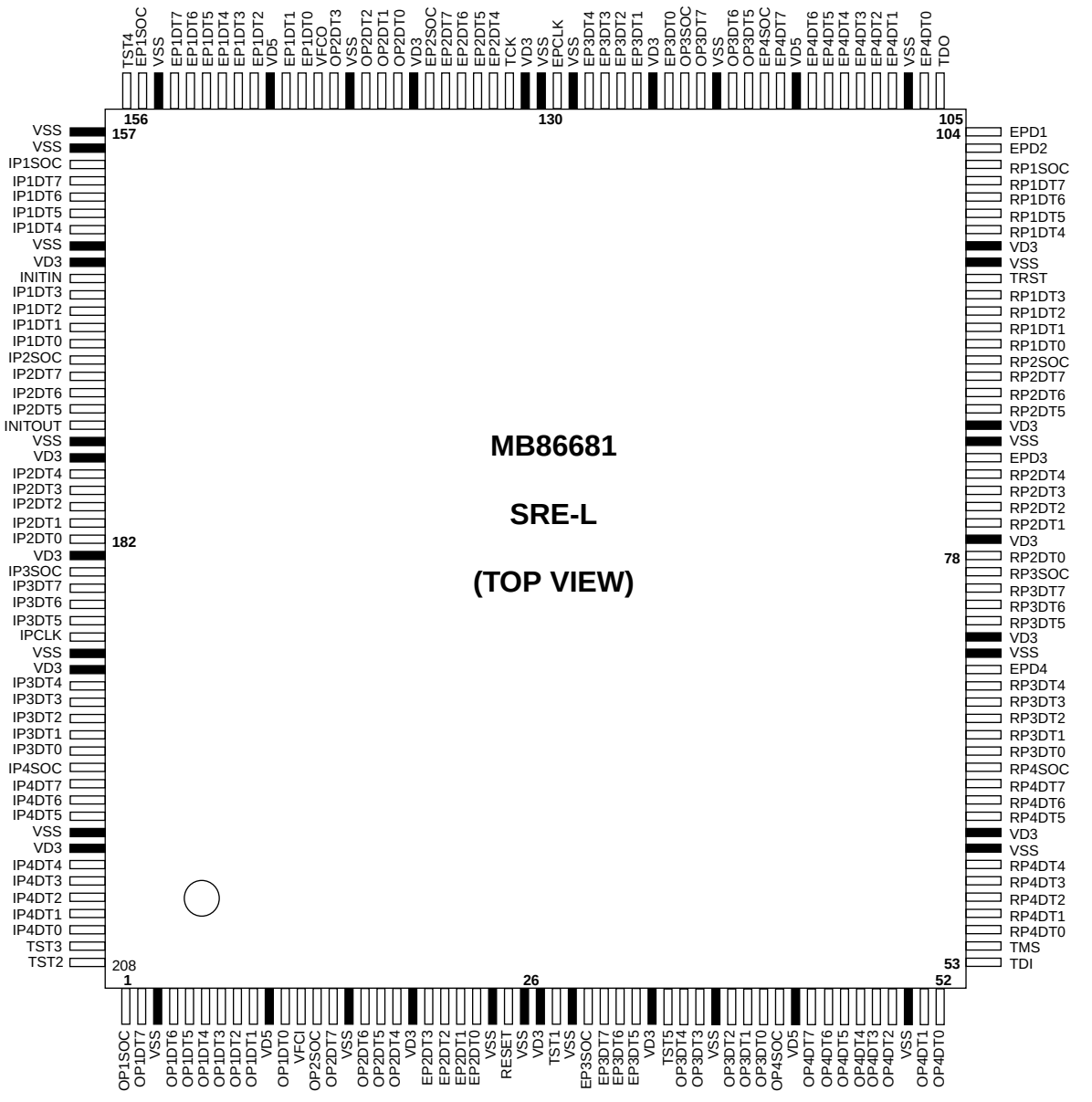



**Figure 33 MB86681 Pin Assignment**

## D.2 Pin Assignment

| Pin No. | Pin Name | Type | Function |
|---|---|---|---|
| 1 | OP1SOC | O(5.0V) | Output Port1, Start Of Cell |
| 2 | OP1DT7 | O(5.0V) | Output Port1, bit D7 (MSB) |
| 3 | $V_{SS}$ | - | |
| 4 | OP1DT6 | O(5.0V) | Output Port1, bit D6 |
| 5 | OP1DT5 | O(5.0V) | Output Port1, bit D5 |
| 6 | OP1DT4 | O(5.0V) | Output Port1, bit D4 |
| 7 | OP1DT3 | O(5.0V) | Output Port1, bit D3 |
| 8 | OP1DT2 | O(5.0V) | Output Port1, bit D2 |
| 9 | OP1DT1 | O(5.0V) | Output Port1, bit D1 |
| 10 | $V_{D5}$ | - | |
| 11 | OP1DT0 | O(5.0V) | Output Port1, bit D0 |
| 12 | VFCI | I | Vertical Flow Control Input Port |
| 13 | OP2SOC | O(5.0V) | Output Port2, Start Of Cell |
| 14 | OP2DT7 | O(5.0V) | Output Port2, bit D7 (MSB) |
| 15 | $V_{SS}$ | - | |
| 16 | OP2DT6 | O(5.0V) | Output Port2, bit D6 |
| 17 | OP2DT5 | O(5.0V) | Output Port2, bit D5 |
| 18 | OP2DT4 | O(5.0V) | Output Port2, bit D4 |
| 19 | $V_{D3}$ | - | |
| 20 | EP2DT3 | I | Expansion Port2, bit D3 |
| 21 | EP2DT2 | I | Expansion Port2, bit D2 |
| 22 | EP2DT1 | I | Expansion Port2, bit D1 |
| 23 | EP2DT0 | I | Expansion Port2, bit D0 |
| 24 | $V_{SS}$ | - | |
| 25 | $\overline{\text{RESET}}$ | I | Reset |
| 26 | $V_{SS}$ | - | |
| 27 | $V_{D3}$ | - | |
| 28 | TST1 | I | Reserved Test Input pin-Connect to $V_{SS}$ |
| 29 | VSS | - | |
| 30 | EP3SOC | I | Expansion Port3, Start Of Cell |
| 31 | EP3DT7 | I | Expansion Port3, bit D7 (MSB) |
| 32 | EP3DT6 | I | Expansion Port3, bit D6 |
| 33 | EP3DT5 | I | Expansion Port3, bit D5 |
| 34 | $V_{D3}$ | - | |
| 35 | TST5 | O(5.0V) | Reserved Test Output pin |

| Pin No. | Pin Name | Type | Function |
|---|---|---|---|
| 36 | OP3DT4 | O(5.0V) | Output Port3, bit D4 |
| 37 | OP3DT3 | O(5.0V) | Output Port3, bit D3 |
| 38 | $V_{SS}$ | - | |
| 39 | OP3DT2 | O(5.0V) | Output Port3, bit D2 |
| 40 | OP3DT1 | O(5.0V) | Output Port3, bit D1 |
| 41 | OP3DT0 | O(5.0V) | Output Port3, bit D0 |
| 42 | OP4SOC | O(5.0V) | Output Port4, Start Of Cell |
| 43 | $V_{D5}$ | - | |
| 44 | OP4DT7 | O(5.0V) | Output Port4, bit D7 (MSB) |
| 45 | OP4DT6 | O(5.0V) | Output Port4, bit D6 |
| 46 | OP4DT5 | O(5.0V) | Output Port4, bit D5 |
| 47 | OP4DT4 | O(5.0V) | Output Port4, bit D4 |
| 48 | OP4DT3 | O(5.0V) | Output Port4, bit D3 |
| 49 | OP4DT2 | O(5.0V) | Output Port4, bit D2 |
| 50 | $V_{SS}$ | - | |
| 51 | OP4DT1 | O(5.0V) | Output Port4, bit D1 |
| 52 | OP4DT0 | O(5.0V) | Output Port4, bit D0 |
| 53 | TDI | I | JTAG Test Data Input |
| 54 | TMS | I | JTAG Test Mode Select |
| 55 | RP4DT0 | O(3.0V) | Regeneration Port4, bit D0 |
| 56 | RP4DT1 | O(3.0V) | Regeneration Port4, bit D1 |
| 57 | RP4DT2 | O(3.0V) | Regeneration Port4, bit D2 |
| 58 | RP4DT3 | O(3.0V) | Regeneration Port4, bit D3 |
| 59 | RP4DT4 | O(3.0V) | Regeneration Port4, bit D4 |
| 60 | $V_{SS}$ | - | |
| 61 | $V_{D3}$ | - | |
| 62 | RP4DT5 | O(3.0V) | Regeneration Port4, bit D5 |
| 63 | RP4DT6 | O(3.0V) | Regeneration Port4, bit D6 |
| 64 | RP4DT7 | O(3.0V) | Regeneration Port4, bit D7 (MSB) |
| 65 | RP4SOC | O(3.0V) | Regeneration Port4, Start Of Cell |
| 66 | RP3DT0 | O(3.0V) | Regeneration Port3, bit D0 |
| 67 | RP3DT1 | O(3.0V) | Regeneration Port3, bit D1 |
| 68 | RP3DT2 | O(3.0V) | Regeneration Port3, bit D2 |
| 69 | RP3DT3 | O(3.0V) | Regeneration Port3, bit D3 |
| 70 | RP3DT4 | O(3.0V) | Regeneration Port3, bit D4 |
| 71 | EPD4 | OT(3.0V) | Tristate I4 Input Port EPD signal |
| 72 | $V_{SS}$ | - | |
| 73 | $V_{D3}$ | - | |

| Pin No. | Pin Name | Type | Function |
|---|---|---|---|
| 74 | RP3DT5 | O(3.0V) | Regeneration Port3, bit D5 |
| 75 | RP3DT6 | O(3.0V) | Regeneration Port3, bit D6 |
| 76 | RP3DT7 | O(3.0V) | Regeneration Port3, bit D7 (MSB) |
| 77 | RP3SOC | O(3.0V) | Regeneration Port3, Start Of Cell |
| 78 | RP2DT0 | O(3.0V) | Regeneration Port2, bit D0 |
| 79 | $V_{D3}$ | - | |
| 80 | RP2DT1 | O(3.0V) | Regeneration Port2, bit D1 |
| 81 | RP2DT2 | O(3.0V) | Regeneration Port2, bit D2 |
| 82 | RP2DT3 | O(3.0V) | Regeneration Port2, bit D3 |
| 83 | RP2DT4 | O(3.0V) | Regeneration Port2, bit D4 |
| 84 | EPD3 | OT(3.0V) | Tristate I3 Input Port EPD signal |
| 85 | $V_{SS}$ | - | |
| 86 | $V_{D3}$ | - | |
| 87 | RP2DT5 | O(3.0V) | Regeneration Port2, bit D5 |
| 88 | RP2DT6 | O(3.0V) | Regeneration Port2, bit D6 |
| 89 | RP2DT7 | O(3.0V) | Regeneration Port2, bit D7 (MSB) |
| 90 | RP2SOC | O(3.0V) | Regeneration Port2, Start Of Cell |
| 91 | RP1DT0 | O(3.0V) | Regeneration Port1, bit D0 |
| 92 | RP1DT1 | O(3.0V) | Regeneration Port1, bit D1 |
| 93 | RP1DT2 | O(3.0V) | Regeneration Port1, bit D2 |
| 94 | RP1DT3 | O(3.0V) | Regeneration Port1, bit D3 |
| 95 | $\overline{TRST}$ | I | JTAG Test Reset |
| 96 | $V_{SS}$ | - | |
| 97 | $V_{D3}$ | - | |
| 98 | RP1DT4 | O(3.0V) | Regeneration Port1, bit D4 |
| 99 | RP1DT5 | O(3.0V) | Regeneration Port1, bit D5 |
| 100 | RP1DT6 | O(3.0V) | Regeneration Port1, bit D6 |
| 101 | RP1DT7 | O(3.0V) | Regeneration Port1, bit D7 (MSB) |
| 102 | RP1SOC | O(3.0V) | Regeneration Port1, Start Of Cell |
| 103 | EPD2 | OT(3.0V) | Tristate I2 Input Port EPD signal |
| 104 | EPD1 | OT(3.0V) | Tristate I1 Input Port EPD signal |
| 105 | TDO | OT(5.0V) | Tristate JTAG Test Data Output |
| 106 | EP4DT0 | I | Expansion Port4, bit D0 |
| 107 | $V_{SS}$ | - | |
| 108 | EP4DT1 | I | Expansion Port4, bit D1 |
| 109 | EP4DT2 | I | Expansion Port4, bit D2 |
| 110 | EP4DT3 | I | Expansion Port4, bit D3 |
| 111 | EP4DT4 | I | Expansion Port4, bit D4 |

| Pin No. | Pin Name | Type | Function |
|---|---|---|---|
| 112 | EP4DT5 | I | Expansion Port4, bit D5 |
| 113 | EP4DT6 | I | Expansion Port4, bit D6 |
| 114 | $V_{D5}$ | - | |
| 115 | EP4DT7 | I | Expansion Port4, bit D6 (MSB) |
| 116 | EP4SOC | I | Expansion Port4, Start Of Cell |
| 117 | OP3DT5 | O(5.0V) | Output Port3, bit D5 |
| 118 | OP3DT6 | O(5.0V) | Output Port3, bit D6 |
| 119 | $V_{SS}$ | - | |
| 120 | OP3DT7 | O(5.0V) | Output Port3, bit D7 (MSB) |
| 121 | OP3SOC | O(5.0V) | Output Port3, Start Of Cell |
| 122 | EP3DT0 | I(5.0V) | Expansion Port3, bit D0 |
| 123 | $V_{D3}$ | - | |
| 124 | EP3DT1 | I | Expansion Port3, bit D1 |
| 125 | EP3DT2 | I | Expansion Port3, bit D2 |
| 126 | EP3DT3 | I | Expansion Port3, bit D3 |
| 127 | EP3DT4 | I | Expansion Port3, bit D4 |
| 128 | $V_{SS}$ | - | |
| 129 | EPCLK | I | Expansion Port Clock |
| 130 | $V_{SS}$ | - | |
| 131 | $V_{D3}$ | - | |
| 132 | TCK | I | JTAG Test Clock |
| 133 | EP2DT4 | I | Expansion Port2, bit D4 |
| 134 | EP2DT5 | I | Expansion Port2, bit D5 |
| 135 | EP2DT6 | I | Expansion Port2, bit D6 |
| 136 | EP2DT7 | I | Expansion Port2, bit D7 (MSB) |
| 137 | EP2SOC | I | Expansion Port2, Start Of Cell |
| 138 | $V_{D3}$ | - | |
| 139 | OP2DT0 | O(5.0V) | Output Port2, bit D0 |
| 140 | OP2DT1 | O(5.0V) | Output Port2, bit D1 |
| 141 | OP2DT2 | O(5.0V) | Output Port2, bit D2 |
| 142 | $V_{SS}$ | - | |
| 143 | OP2DT3 | O(5.0V) | Output Port2, bit D3 |
| 144 | VFCO | O(5.0V) | Vertical Flow Control Output Port |
| 145 | EP1DT0 | I | Expansion Port1, bit D0 |
| 146 | EP1DT1 | I | Expansion Port1, bit D1 |
| 147 | $V_{D5}$ | - | |
| 148 | EP1DT2 | I | Expansion Port1, bit D2 |

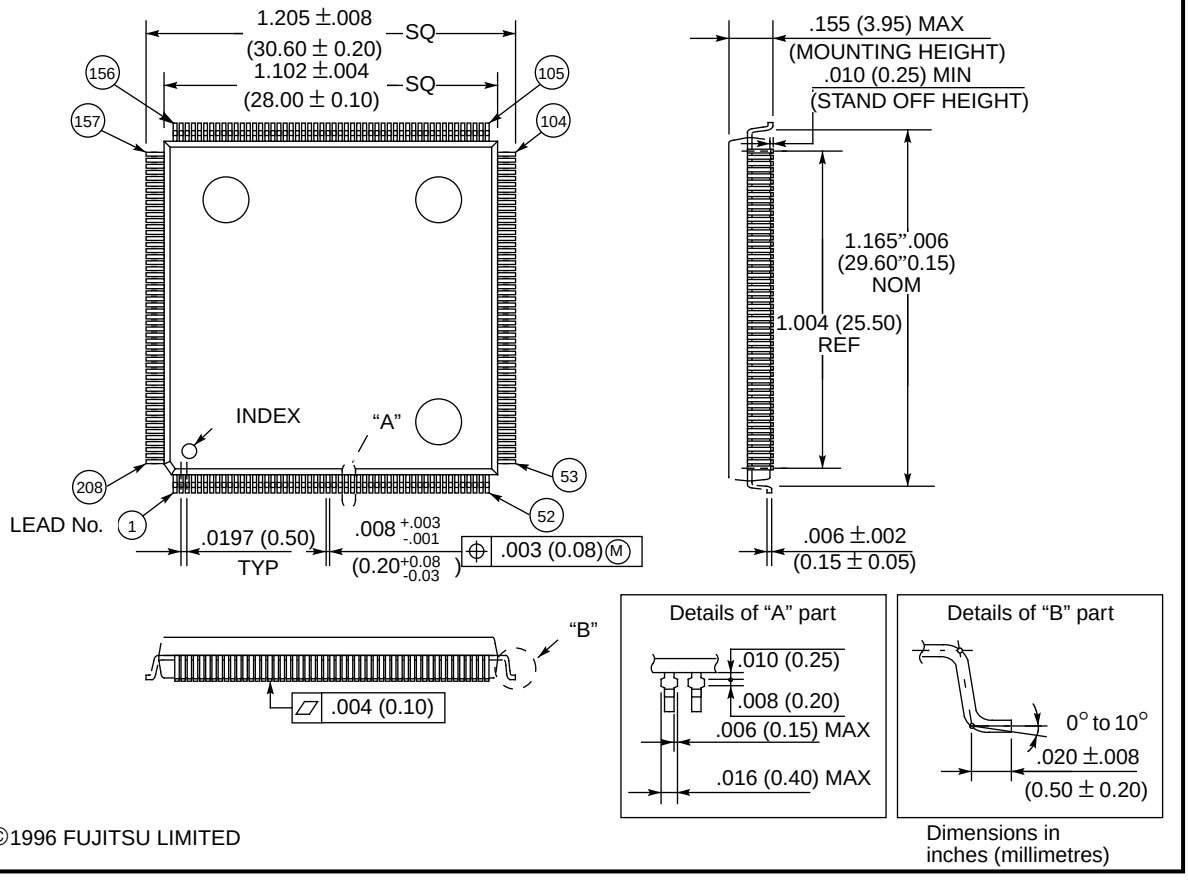
| Pin No. | Pin Name | Type | Function |
|---|---|---|---|
| 149 | EP1DT3 | I | Expansion Port1, bit D3 |
| 150 | EP1DT4 | I | Expansion Port1, bit D4 |
| 151 | EP1DT5 | I | Expansion Port1, bit D5 |
| 152 | EP1DT6 | I | Expansion Port1, bit D6 |
| 153 | EP1DT7 | I | Expansion Port1, bit D7 (MSB) |
| 154 | $V_{SS}$ | - | |
| 155 | EP1SOC | I | Expansion Port1, Start Of Cell |
| 156 | TST4 | O(5.0V) | Reserved Test Output pin |
| 157 | $V_{SS}$ | - | |
| 158 | $V_{SS}$ | - | |
| 159 | IP1SOC | I | Input Port1, Start Of Cell |
| 160 | IP1DT7 | I | Input Port1, bit D7 (MSB) |
| 161 | IP1DT6 | I | Input Port1, bit D6 |
| 162 | IP1DT5 | I | Input Port1, bit D5 |
| 163 | IP1DT4 | I | Input Port1, bit D4 |
| 164 | $V_{SS}$ | - | |
| 165 | $V_{D3}$ | - | |
| 166 | INITIN | I | Initialization Input Port |
| 167 | IP1DT3 | I | Input Port1, bit D3 |
| 168 | IP1DT2 | I | Input Port1, bit D2 |
| 169 | IP1DT1 | I | Input Port1, bit D1 |
| 170 | IP1DT0 | I | Input Port1, bit D0 |
| 171 | IP2SOC | I | Input Port2, Start Of Cell |
| 172 | IP2DT7 | I | Input Port2, bit D7 |
| 173 | IP2DT6 | I | Input Port2, bit D6 |
| 174 | IP2DT5 | I | Input Port2, bit D5 |
| 175 | INITOUT | O(3.0V) | Initialization Output Port |
| 176 | $V_{SS}$ | - | |
| 177 | $V_{D3}$ | - | |
| 178 | IP2DT4 | I | Input Port2, bit D4 |
| 179 | IP2DT3 | I | Input Port2, bit D3 |
| 180 | IP2DT2 | I | Input Port2, bit D2 |
| 181 | IP2DT1 | I | Input Port2, bit D1 |
| 182 | IP2DT0 | I | Input Port2, bit D0 |
| 183 | $V_{D3}$ | - | |
| 184 | IP3SOC | I | Input Port3, Start Of Cell |
| 185 | IP3DT7 | I | Input Port3, bit D7 |
| 186 | IP3DT6 | I | Input Port3, bit D6 |

| Pin No. | Pin Name | Type | Function |
|---|---|---|---|
| 187 | IP3DT5 | I | Input Port3, bit D5 |
| 188 | IPCLK | I | Input Port Clock |
| 189 | $V_{SS}$ | - | |
| 190 | $V_{D3}$ | - | |
| 191 | IP3DT4 | I | Input Port3, bit D4 |
| 192 | IP3DT3 | I | Input Port3, bit D3 |
| 193 | IP3DT2 | I | Input Port3, bit D2 |
| 194 | IP3DT1 | I | Input Port3, bit D1 |
| 195 | IP3DT0 | I | Input Port3, bit D0 |
| 196 | IP4SOC | I | Input Port4, Start Of Cell |
| 197 | IP4DT7 | I | Input Port4, bit D7 |
| 198 | IP4DT6 | I | Input Port4, bit D6 |
| 199 | IP4DT5 | I | Input Port4, bit D5 |
| 200 | $V_{SS}$ | - | |
| 201 | $V_{D3}$ | - | |
| 202 | IP4DT4 | I | Input Port4, bit D4 |
| 203 | IP4DT3 | I | Input Port4, bit D3 |
| 204 | IP4DT2 | I | Input Port4, bit D2 |
| 205 | IP4DT1 | I | Input Port4, bit D1 |
| 206 | IP4DT0 | I | Input Port4, bit D0 |
| 207 | TST3 | I | Reserved Test Input pin-Connect to $V_{SS}$ |
| 208 | TST2 | I | Reserved Test Input pin-Connect to $V_{SS}$ |

# E Package Dimensions

## FPT-208P-M04

**208-LEAD PLASTIC FLAT PACKAGE**
**(CASE No.: FPT-208P-M04)**






Dimensions in
inches (millimetres)

# Revision Control

| Revision Number | Date DD/MM/YY | Description of the Changes |
|---|---|---|
| 0.8 | 11/09/96 | Minor syntax corrections made to JTAG BSDL description in Appendix C.<br>Correction to the Back page Revision Control Number. |
| 0.9 | 21/02/97 | Non Characterized AC Parametrics and updated diagrams added |
| 1.0 | 11/03/97 | Characterized AC Parametrics and updated diagrams added |
| 1.1 | 19/11/97 | AC & DC Parametrics sections altered. |
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