

## Signefics

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FAST Products	

# FAST 74F74 FLIP-FLOP

## Dual D-Type Flip-Flop

TYPE	TYPICAL $f_{MAX}$	TYPICAL SUPPLY CURRENT (TOTAL)
74F74	125 MHz	11.5mA

### DESCRIPTION

The 74F74 is a dual positive edge-triggered D-type flip-flop featuring individual Data, Clock, Set and Reset inputs; also true and complementary outputs.

Set ( $\bar{S}_D$ ) and Reset ( $\bar{R}_D$ ) are asynchronous active-Low inputs and operate independently of the Clock (CP) input.

Set ( $\bar{S}_D$ ) and Reset ( $\bar{R}_D$ ) are synchronously

active Low inputs and operate independently of the clock (CP). When Set and Reset are inactive (High), Data at the D input is transferred to the Q and  $\bar{Q}$  outputs on the Low-to-High transition of the Clock. Data must be stable just one setup time prior to the Low-to-High transition of the clock for predictable operation.

Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the D input may be changed without affecting the levels of the output.

### ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ ; $T_A = 0^\circ C$ to $+70^\circ C$
14-Pin Plastic DIP	N74F74N
14-Pin Plastic SO	N74F74D

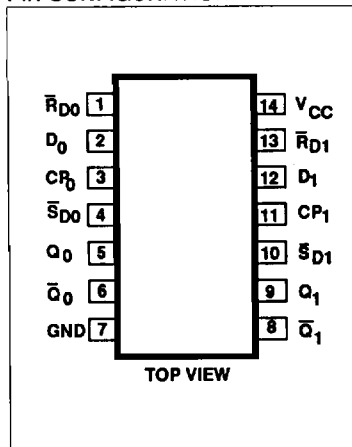
### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0, D_1$	Data inputs	1.0/1.0	20 $\mu$ A/0.6mA
$CP_0, CP_1$	Clock inputs (active rising edge)	1.0/1.0	20 $\mu$ A/0.6mA
$\bar{S}_{D0}, \bar{S}_{D1}$	Set inputs (active Low)	1.0/3.0	20 $\mu$ A/1.8mA
$\bar{R}_{D0}, \bar{R}_{D1}$	Reset inputs (active Low)	1.0/3.0	20 $\mu$ A/1.8mA
$Q_0, \bar{Q}_0, Q_1, \bar{Q}_1$	Data outputs	50/33	1.0mA/20mA

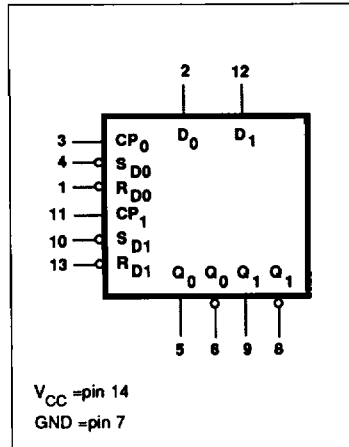
#### NOTE:

One (1.0) FAST Unit Load is defined as: 20 $\mu$ A in the High state and 0.6mA in the Low state.

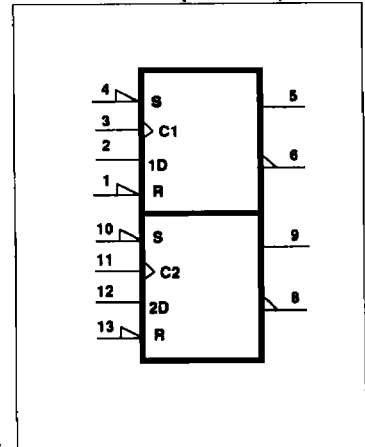
### PIN CONFIGURATION



### LOGIC SYMBOL



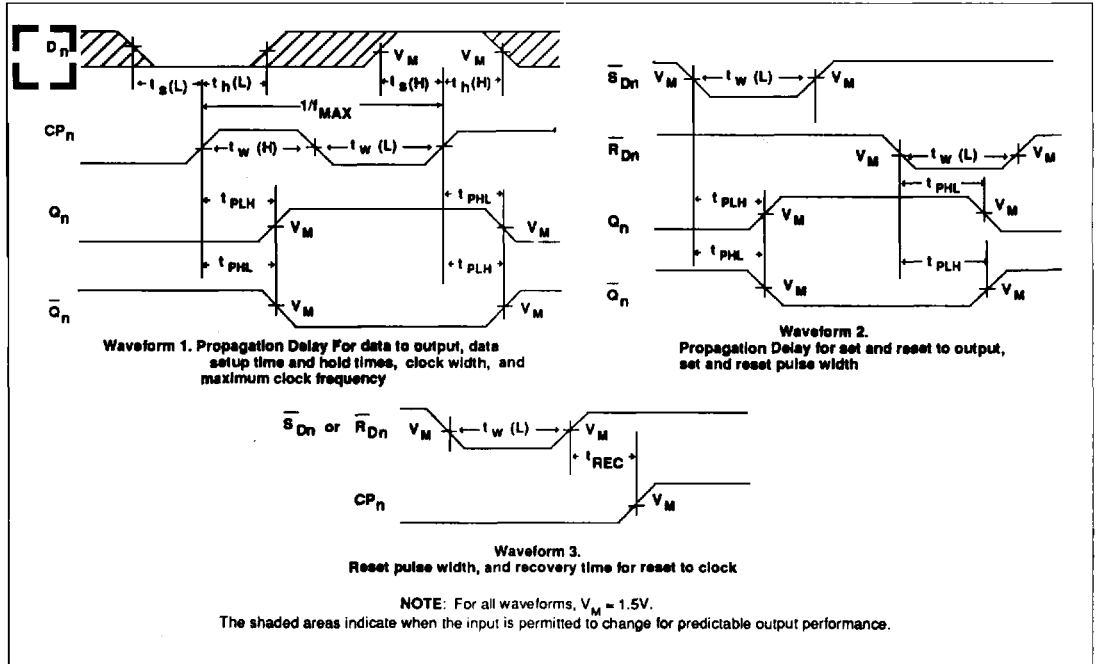
### LOGIC SYMBOL (IEEE/IEC)



FLIP-FLOP

74F74

AC WAVEFORMS



TEST CIRCUIT AND WAVEFORMS

