TYPES 3N201, 3N202, 3N203
N-CHANNEL DUAL-GATE DEPLETION-TYPE INSULATED-GATE FIELD-EFFECT TRANSISTORS

BULLETIN NO. DL-S 7111487, APRIL 1971

DEPLETION-TYPE MOS SILICON TRANSISTORS

- Monolithic Gate-Protection Diodes
- Low C_{rss} . . . 0.03 pF Max
- High $|y_{fs}|$ . . . 12, 000 μmhos Typ

description

The 3N201, 3N202, and 3N203 are N-channel, depletion-type, dual-gate, metal-oxide-semiconductor transistors. They are protected from excessive input voltages by integrated back-to-back diodes between gates and source, thus eliminating precautionary handling procedures required by unprotected MOS transistors. These transistors are ideally suited for many applications which previously only vacuum tubes could fulfill.

The 3N201 is intended for use in VHF pre-amplifiers where linear, low-noise amplification is required. Its extremely low feedback capacitance permits high stable gain without the use of neutralization.

The 3N202 is intended for use as a VHF mixer and is well suited for TV tuners. Its use as a mixer minimizes cross-modulation distortion and provides low-noise operation.

The 3N203 is designed for application in tuned high-frequency amplifiers such as TV IF strips. Its extremely low feedback capacitance permits high stage gain and stability without the necessity for neutralization.

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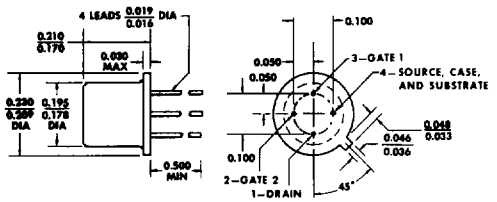
*mechanical data

THE SUBSTRATE AND SOURCE ARE IN ELECTRICAL CONTACT WITH THE CASE



ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED

ALL JEDEC TO-72 DIMENSIONS AND NOTES ARE APPLICABLE

*absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Drain—Gate-One Voltage	30 V
Drain—Gate-Two Voltage	30 V
Drain-Source Voltage	25 V
Forward Gate-One-Terminal Current (See Note 1)	10 mA
Forward Gate-Two-Terminal Current (See Note 1)	10 mA
Reverse Gate-One-Terminal Current	−10 mA
Reverse Gate-Two-Terminal Current	−10 mA
Continuous Drain Current	50 mA
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 2)	360 mW
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	1.2 W
Storage Temperature Range	−65°C to 200°C
Lead Temperature 1/16 Inch from Case for 10 Seconds	300°C

NOTES: 1. Forward gate-terminal current is the current into a gate terminal with a forward gate-source voltage applied. This voltage is of such polarity that an increase in its magnitude causes the channel resistance to decrease.
2. Derate linearly to 175°C free-air temperature at the rate of 2.4 mW/°C.
3. Derate linearly to 175°C case temperature at the rate of 8 mW/°C.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

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TYPES 3N201, 3N202, 3N203
N-CHANNEL DUAL-GATE DEPLETION-TYPE INSULATED-GATE FIELD-EFFECT TRANSISTORS

*electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
$V_{(BR)DS}$	Drain-Source Breakdown Voltage	I_D = 10 μA,	$V_{G1S} = V_{G2S}$ = −5 V		25		V
$V_{(BR)G1SSF}$	Gate-One–Source Forward Breakdown Voltage	I_{G1} = 10 mA,	$V_{G2S} = V_{DS}$ = 0,	See Note 4	6	30	V
$V_{(BR)G1SSR}$	Gate-One–Source Reverse Breakdown Voltage	I_{G1} = −10 mA,	$V_{G2S} = V_{DS}$ = 0,	See Note 4	−6	−30	V
$V_{(BR)G2SSF}$	Gate-Two–Source Forward Breakdown Voltage	I_{G2} = 10 mA,	$V_{G1S} = V_{DS}$ = 0,	See Note 4	6	30	V
$V_{(BR)G2SSR}$	Gate-Two–Source Reverse Breakdown Voltage	I_{G2} = −10 mA,	$V_{G1S} = V_{DS}$ = 0,	See Note 4	−6	−30	V
I_{G1SSF}	Gate-One-Terminal Forward Current	V_{G1S} = 5 V,	$V_{G2S} = V_{DS}$ = 0			10	nA
I_{G1SSR}	Gate-One-Terminal Reverse Current	V_{G1S} = −5 V,	$V_{G2S} = V_{DS}$ = 0			−10	nA
		V_{G1S} = −5 V,	$V_{G2S} = V_{DS}$ = 0,	T_A = 150°C		−10	μA
I_{G2SSF}	Gate-Two-Terminal Forward Current	V_{G2S} = 5 V,	$V_{G1S} = V_{DS}$ = 0			10	nA
I_{G2SSR}	Gate-Two-Terminal Reverse Current	V_{G2S} = −5 V,	$V_{G1S} = V_{DS}$ = 0			−10	nA
		V_{G2S} = −5 V,	$V_{G1S} = V_{DS}$ = 0,	T_A = 150°C		−10	μA
I_{DS}	Zero-Gate-One-Voltage Drain Current	V_{DS} = 15 V, V_{G2S} = 4 V,	V_{G1S} = 0, See Note 5	3N201, 3N202	6	30	mA
				3N203	3	15	
$V_{G1S(off)}$	Gate-One–Source Cutoff Voltage	V_{DS} = 15 V,	V_{G2S} = 4 V,	I_D = 20 μA	−0.5	−5	V
$V_{G2S(off)}$	Gate-Two–Source Cutoff Voltage	V_{DS} = 15 V,	V_{G1S} = 0,	I_D = 20 μA	−0.2	−5	V
$\lvert y_{fs} \rvert$	Small-Signal Common-Source Forward Transfer Admittance	V_{DS} = 15 V, V_{G2S} = 4 V, See Note 6	V_{G1S} = 0, f = 1 kHz,	3N201, 3N202	8	20	mmho
				3N203	7	15	
C_{rss}	Common-Source Short-Circuit Reverse Transfer Capacitance	V_{DS} = 15 V, f = 1 MHz	V_{G2S} = 4 V,	I_D = 10 mA,	0.005	0.03	pF

NOTES: 4. All gate breakdown voltages are measured while the device is conducting rated gate current. This ensures that the gate-voltage-limiting network is functioning properly.

5. This parameter must be measured using pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

6. This parameter must be measured with bias voltages applied for less than 5 seconds to avoid overheating.

*3N201 operating characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS		3N201 MIN	3N201 MAX	UNIT
NF	Common-Source Spot Noise Figure	V_{DD} = 18 V, f = 200 MHz,	V_{GG} = 7 V, See Figure 1		4.5	dB
G_{ps}	Small-Signal Common-Source Insertion Power Gain			15	25	dB
BW	Bandwidth			5	9	MHz
$V_{GG(GC)}$	Gain-Control Gate-Supply Voltage	V_{DD} = 18 V, f = 200 MHz,	ΔG_{ps} = −30 dB†, See Figure 1	0	−3	V

† ΔG_{ps} is defined as the change in G_{ps} from the value at V_{GG} = 7 volts.

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*3N202 operating characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS		3N202 MIN	3N202 MAX	UNIT
$G_{ps(conv)}$	Small-Signal Conversion Power Gain	V_{DD} = 18 V, f_{RF} = 200 MHz,	f_{LO} = 245 MHz‡, See Figure 2	15	25	dB
BW	Bandwidth			4.5	7.5	MHz

‡Amplitude at input from local oscillator is 3 volts rms.

*3N203 operating characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS		3N203 MIN	3N203 MAX	UNIT
NF	Common-Source Spot Noise Figure	V_{DD} = 18 V, f = 45 MHz,	V_{GG} = 6 V, See Figure 3		6	dB
G_{ps}	Small-Signal Common-Source Insertion Power Gain			20	30	dB
BW	Bandwidth			3	6	MHz
$V_{GG(GC)}$	Gain-Control Gate-Supply Voltage	V_{DD} = 18 V, f = 45 MHz,	ΔG_{ps} = −30 dB §, See Figure 3	0	−3	V

§ΔG_{ps} is defined as the change in G_{ps} from the value at V_{GG} = 6 volts.

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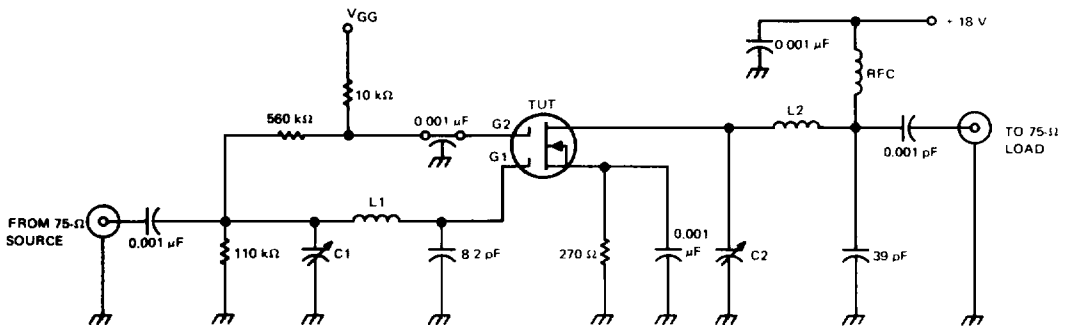
*PARAMETER MEASUREMENT INFORMATION



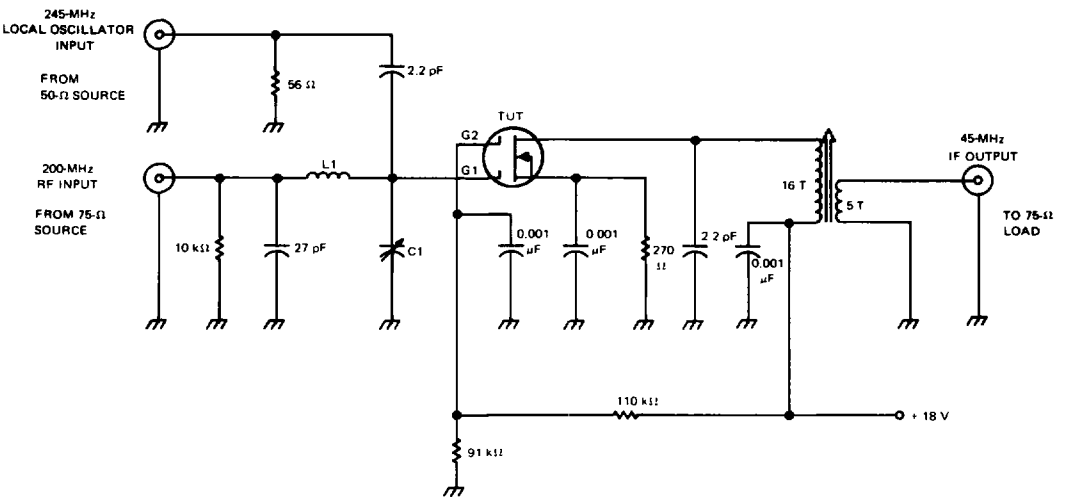
CIRCUIT COMPONENT INFORMATION

C1: Erie variable ceramic, 4–30 pF, set for ≈ 22 pF
C2: Erie variable ceramic, 4–30 pF, set for ≈ 10 pF
L1: 4T, #14 copper, 1/4" ID, 1/6" pitch
L2: 3T, #14 copper, 1/4" ID, 1/8" pitch
RFC: Delevan No. 153712, 1 µH

FIGURE 1–200-MHz POWER GAIN, GAIN-CONTROL VOLTAGE, AND NOISE FIGURE TEST CIRCUIT FOR 3N201

*JEDEC registered data

*PARAMETER MEASUREMENT INFORMATION



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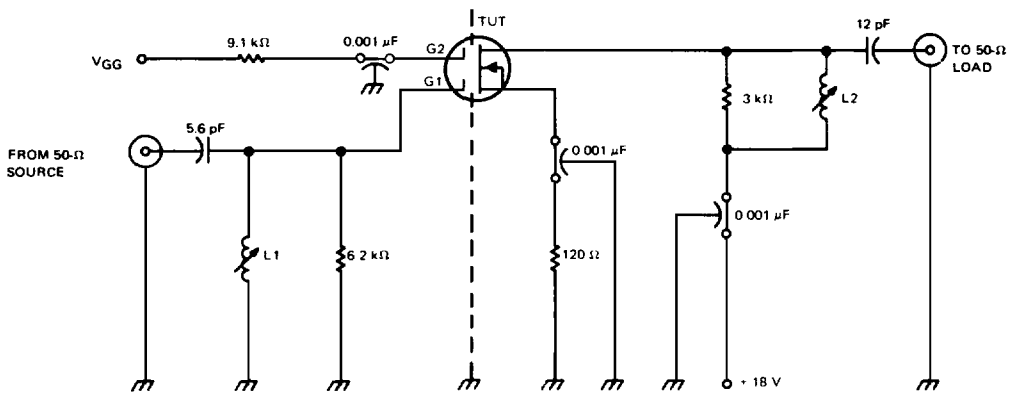
CIRCUIT COMPONENT INFORMATION

C1: Erie variable ceramic, 1.5–7 pF, set for ≈ 4.7 pF
L1: 4T, #14 copper, 1/4" ID, 1/6" pitch

FIGURE 2–200-MHz-to-45-MHz CIRCUIT FOR CONVERSION POWER GAIN FOR 3N202



CIRCUIT COMPONENT INFORMATION

L1: 14T, #30 copper, close-wound on 7/32" OD form with Arnold Engineering type "J" tuning core
L2: 10T, #30 copper, close-wound on 7/32" OD form with Arnold Engineering type "J" tuning core

FIGURE 3–45-MHz POWER GAIN, GAIN-CONTROL VOLTAGE, AND NOISE FIGURE TEST CIRCUIT FOR 3N203

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TYPICAL CHARACTERISTICS AT T_A = 25°C

3N201
RELATIVE SMALL-SIGNAL POWER-GAIN vs GAIN-CONTROL GATE-SUPPLY VOLTAGE

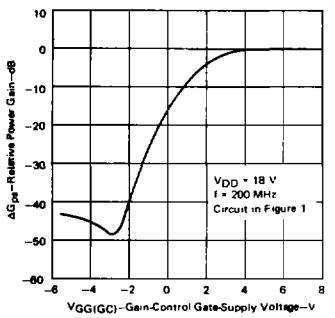

FIGURE 4

3N201
SMALL-SIGNAL COMMON-SOURCE INSERTION POWER GAIN vs DRAIN CURRENT

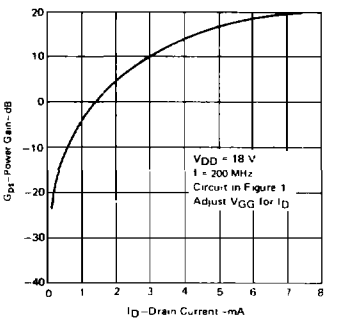

FIGURE 5

3N201
COMMON-SOURCE SPOT NOISE FIGURE vs GAIN-CONTROL GATE-SUPPLY VOLTAGE

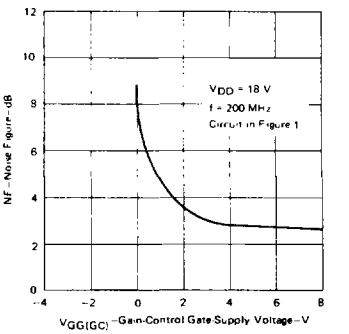

FIGURE 6

3N202
SMALL-SIGNAL CONVERSION POWER GAIN vs INPUT FROM LOCAL OSCILLATOR

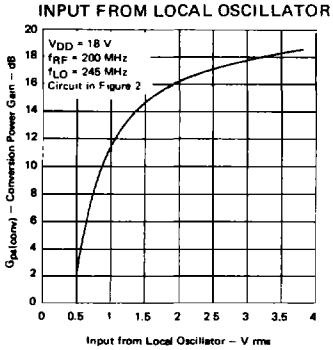

FIGURE 7

3N203
SMALL-SIGNAL COMMON-SOURCE INSERTION POWER GAIN vs GAIN-CONTROL SUPPLY VOLTAGE

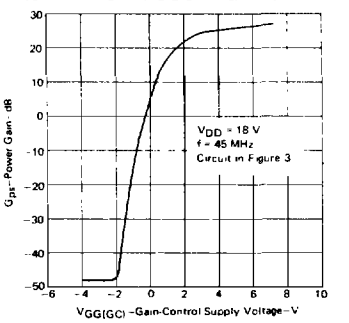

FIGURE 8

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