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The S-4630A is a CMOS thermal print head driver containing a 64-bit shift register and a latch. It can be easily used for general purpose because "H" or "L" can be selected for the driver enable and the latch is fixed to "L". It is ideal for the thermal print head of 200 dpi or 8 dots/mm because of its driver output pad pitch of 110 μm .

■ Features

- Low current consumption : 0.4 mA typ.
($f_{\text{CLK}}=5$ MHz, SI : fixed)
- High speed operation : 7 MHz (chip)
5 MHz (cascade connection)
- Driver output voltage : 36 V max.
- Driver output current : 9 mA max.
- 64-bit shift register and latch are built in
- Driver enable
- Driver-off function when supply voltage falls

■ Block Diagram

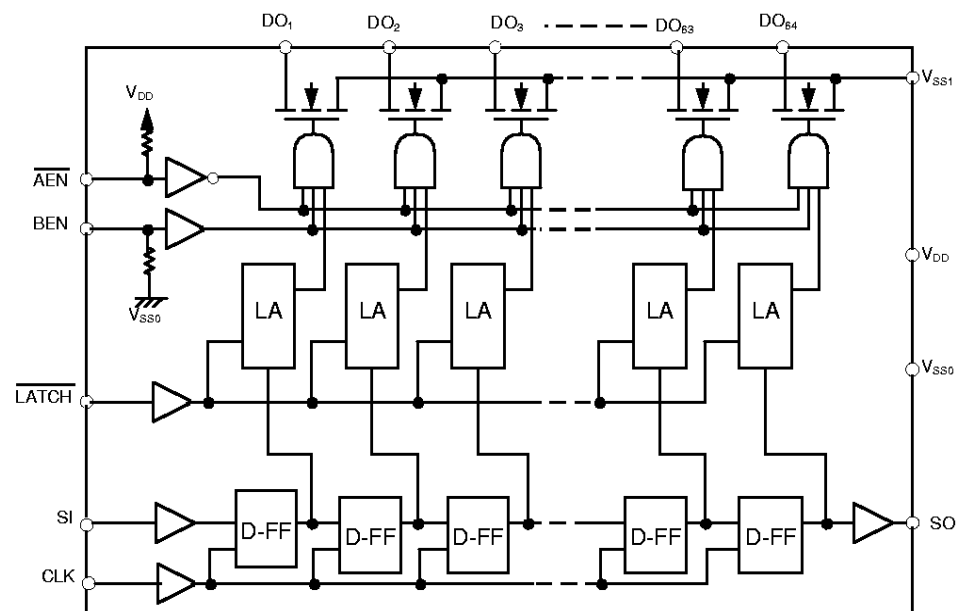


Figure 1

64-bit THERMAL HEAD DRIVER
S-4630A

■ **Operation**

The 64-bit shift register reads the data input to SI on the rising edge of the CLOCK input.

The latch circuit reads the data of the shift register when it is "L" level, and it holds the preceding data when it is "H" level.

The latch data are output to the respective drivers when $\overline{\text{AEN}}$ is low and $\overline{\text{BEN}}$ is high. The driver output transistor turns on when the latch data are high and turns off when low. Turning $\overline{\text{AEN}}$ high or $\overline{\text{BEN}}$ low makes all driver output transistors go off.

All driver output transistors go off when power supply voltage becomes lower than V_{DET} regardless of all input signals.

■ **Terminal Functions** (Refer to the dimensions for the pad arrangement)

Table 1

No.	Name	Functions
1 to 64	DO ₁ to DO ₆₄ (DO _n)	Driver output terminals (Nch open-drain)
65, 66, 71, 72, 79, 80	V _{SS1}	GND for driver (0 V)
68, 75	V _{DD}	Positive power supply for logic (+5 V)
70, 73	V _{SS0}	GND for logic (0 V)
76	CLK	Clock input terminal for 64-bit shift register
78	SI	Serial data input terminal for 64-bit shift register
67	SO	Serial data output terminal for 64-bit shift register
77	$\overline{\text{LATCH}}$	Data latch signal input terminal $\overline{\text{LATCH}} = \text{"L"} : \text{reads the data of the shift register}$ $\overline{\text{LATCH}} = \text{"H"} : \text{holds the preceding data}$
74	$\overline{\text{AEN}}$	Driver enable terminal : outputs the latch data to the driver when low (pull-up resistor is built in)
69	BEN	Driver enable terminal : outputs the latch data to the driver when high (pull-down resistor is built in)

■ **Absolute Maximum Ratings**

Table 2

Parameter	Symbol	Ratings	Unit
Supply voltage	V _{SS0,1} - V _{DD}	-0.4 to +7.0	V
Driver output voltage	V _{DOH}	36	V
Driver output current	I _{DOL}	15	mA
Input voltage	V _{IN}	V _{SS0} -0.5 to V _{DD} +0.5	V
Output voltage	V _{OUT}	V _{SS0} -0.5 to V _{DD} +0.5	V
Max. junction temperature	T _{JMAX}	125	°C
Operating temperature	T _{opr}	-10 to +80	°C
Storage temperature	T _{stg}	-40 to +125	°C

■ DC Electrical Characteristics

Table 3
(Unless otherwise specified : $V_{DD}=5.0\text{ V}\pm 10\%$, $T_a=-10^\circ\text{C}$ to 80°C)

Parameter	Sybl	Conditions	Min.	Typ.	Max.	Unit	
Supply voltage	V_{DD}		4.5	5.0	5.5	V	
High level input voltage	V_{IH}		$0.7\times V_{DD}$	—	V_{DD}	V	
Low level input voltage	V_{IL}		V_{SS}	—	$0.3\times V_{DD}$	V	
High level input current	I_{IH}	$V_{DD}=5.0\text{ V}$ $V_{IH}=5.0\text{ V}$ $T_a=25^\circ\text{C}$	BEN	—	—	35	μA
				—	—	0.5	μA
Low level input current	I_{IL}	$V_{DD}=5.0\text{ V}$ $V_{IL}=0\text{ V}$ $T_a=25^\circ\text{C}$	$\overline{\text{AEN}}$	-35	—	—	μA
				-0.5	—	—	μA
High level output voltage	V_{OH}	SO terminal, no load	4.45	—	—	V	
Low level output voltage	V_{OL}	SO terminal, no load	—	—	0.05	V	
High level output current	I_{OH}	SO terminal, $V_{OH}=V_{DD}-0.4\text{ V}$	—	—	-0.5	mA	
Low level output current	I_{OL}	SO terminal, $V_{OL}=0.4\text{ V}$	0.5	—	—	mA	
High level driver output voltage	V_{DOH}		—	24	26	V	
Low level driver output voltage	V_{DOL}	$I_{DOL}=9\text{ mA}$, $V_{DD}=5.0\text{ V}$	—	0.7	1.5	V	
Driver leakage current	I_{LEAK}	$V_{DOH}=26\text{ V}$ Per 1-bit of driver output	—	—	1.0	μA	
Current consumption	I_{DD}	$T_a=25\text{ C}$	$f_{CLK}=2\text{ MHz}$, SI : fixed	—	0.2	0.6	mA
			$f_{CLK}=5\text{ MHz}$, SI : fixed	—	0.4	1.2	mA
			$f_{CLK}=5\text{ MHz}$, SI=1/2 f_{CLK}	—	1.6	5.0	mA
Lower V_{DD} detection voltage	V_{DET}		2.0	—	4.0	V	

■ AC Electrical Characteristics

Table 4
($V_{DD}=5.0\text{ V}\pm 10\%$, $T_a=-10^\circ\text{C}$ to 80°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
CLK pulse width	t_{WCLK}		70	—	—	ns
Data setup time	t_{SUD}	$V_{IH}=V_{DD}$, $V_{IL}=V_{SS0}$	40	—	—	ns
Data hold time	t_{HD}	$V_{IH}=V_{DD}$, $V_{IL}=V_{SS0}$	40	—	—	ns
Latch pulse width	t_{WLA}		100	—	—	ns
Latch setup time	t_{SULA}		100	—	—	ns
CLK-SO propagation delay time	t_{dSO}	$C_L=3\text{ pF}$	—	—	120	ns
EN-DOn propagation delay time	t_{dDO}	$R_L=3.0\text{ k}\Omega$, $V_{DOH}=24\text{ V}$	—	—	3.0	μs
DOn rise time	t_{rDO}	$R_L=3.0\text{ k}\Omega$, $V_{DOH}=24\text{ V}$	—	1.0	3.0	μs
DOn fall time	t_{fDO}	$R_L=3.0\text{ k}\Omega$, $V_{DOH}=24\text{ V}$	—	1.0	3.0	μs
Clock frequency	f_{CLK}	When cascade connection	—	—	5.0	MHz

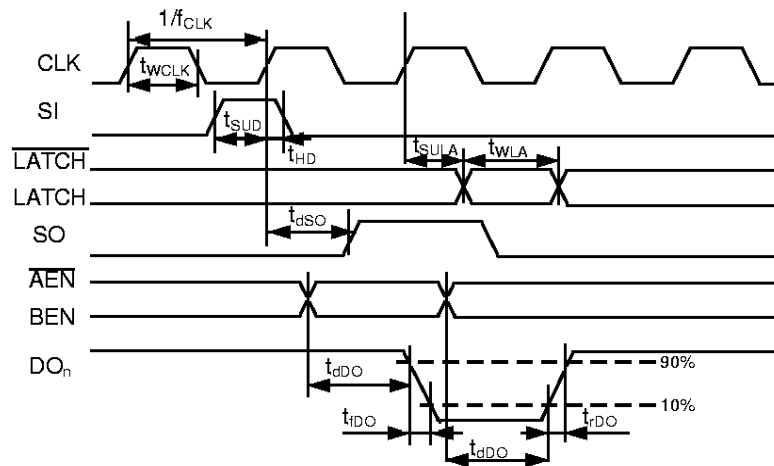


Figure 2

64-bit THERMAL HEAD DRIVER S-4630A

■ Dimensions

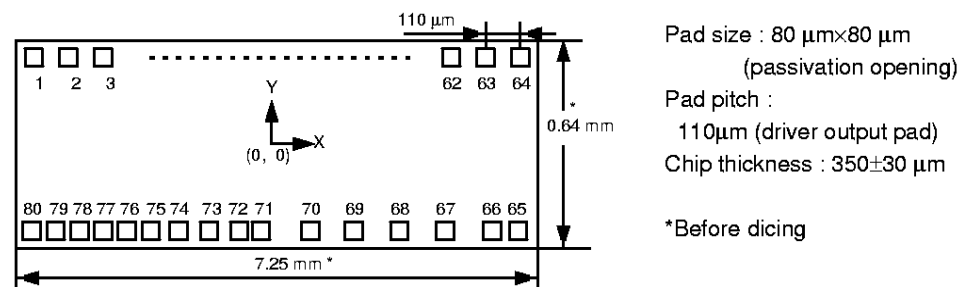


Figure 3

■ Pad Coordinates (The origin of the coordinates axes is the center of the chip)

Table 5

Unit : μm

Pad No.	Name	X	Y	Pad No.	Name	X	Y	Pad No.	Name	X	Y
1	DO ₁	-3465	210	28	DO ₂₈	-495	210	55	DO ₅₅	2475	210
2	DO ₂	-3355	210	29	DO ₂₉	-385	210	56	DO ₅₆	2585	210
3	DO ₃	-3245	210	30	DO ₃₀	-275	210	57	DO ₅₇	2695	210
4	DO ₄	-3135	210	31	DO ₃₁	-165	210	58	DO ₅₈	2805	210
5	DO ₅	-3025	210	32	DO ₃₂	-55	210	59	DO ₅₉	2915	210
6	DO ₆	-2915	210	33	DO ₃₃	55	210	60	DO ₆₀	3025	210
7	DO ₇	-2805	210	34	DO ₃₄	165	210	61	DO ₆₁	3135	210
8	DO ₈	-2695	210	35	DO ₃₅	275	210	62	DO ₆₂	3245	210
9	DO ₉	-2585	210	36	DO ₃₆	385	210	63	DO ₆₃	3355	210
10	DO ₁₀	-2475	210	37	DO ₃₇	495	210	64	DO ₆₄	3465	210
11	DO ₁₁	-2365	210	38	DO ₃₈	605	210	65	V _{SS1}	3466	-210
12	DO ₁₂	-2255	210	39	DO ₃₉	715	210	66	V _{SS1}	3286	-210
13	DO ₁₃	-2145	210	40	DO ₄₀	825	210	67	SO	2870	-210
14	DO ₁₄	-2035	210	41	DO ₄₁	935	210	68	V _{DD}	1696	-210
15	DO ₁₅	-1925	210	42	DO ₄₂	1045	210	69	BEN	1160	-210
16	DO ₁₆	-1815	210	43	DO ₄₃	1155	210	70	V _{SS0}	580	-210
17	DO ₁₇	-1705	210	44	DO ₄₄	1265	210	71	V _{SS1}	130	-210
18	DO ₁₈	-1595	210	45	DO ₄₅	1375	210	72	V _{SS1}	-50	-210
19	DO ₁₉	-1485	210	46	DO ₄₆	1485	210	73	V _{SS0}	-500	-210
20	DO ₂₀	-1375	210	47	DO ₄₇	1595	210	74	AEN	-1000	-210
21	DO ₂₁	-1265	210	48	DO ₄₈	1705	210	75	V _{DD}	-1500	-210
22	DO ₂₂	-1155	210	49	DO ₄₉	1815	210	76	CLK	-2000	-210
23	DO ₂₃	-1045	210	50	DO ₅₀	1925	210	77	LATCH	-2500	-210
24	DO ₂₄	-935	210	51	DO ₅₁	2035	210	78	SI	-3016	-210
25	DO ₂₅	-825	210	52	DO ₅₂	2145	210	79	V _{SS1}	-3286	-210
26	DO ₂₆	-715	210	53	DO ₅₃	2255	210	80	V _{SS1}	-3466	-210
27	DO ₂₇	-605	210	54	DO ₅₄	2365	210				