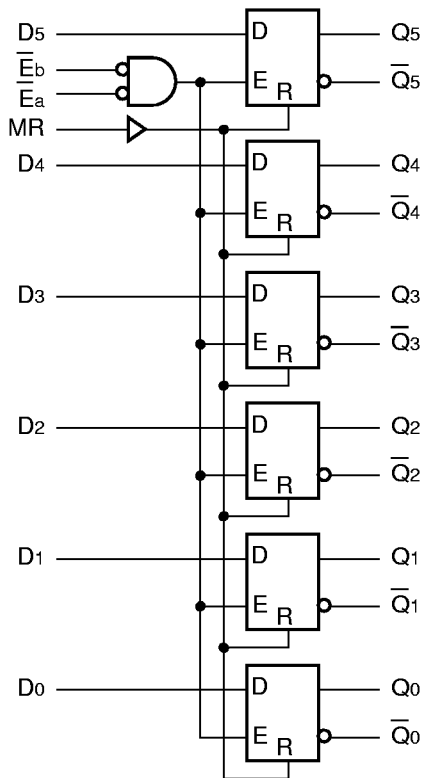


FEATURES

- Max. transparent propagation delay of 900ps
- Min. Master Reset and Enable pulse widths of 100ps
- IEE min. of -98mA
- Industry standard 100K ECL levels
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75KΩ input pull-down resistors
- More than 40% faster than National or Signetics
- Approximately 30% lower power than National or Signetics
- Function and pinout compatible with National and Signetics F100K
- ESD protection of 2000V
- Available in 24-pin CERDIP, 24-pin CERPACK and 28-pin PLCC packages

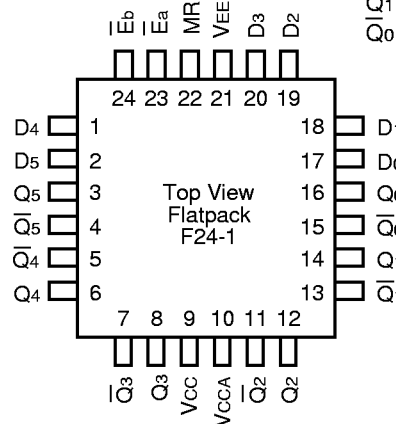
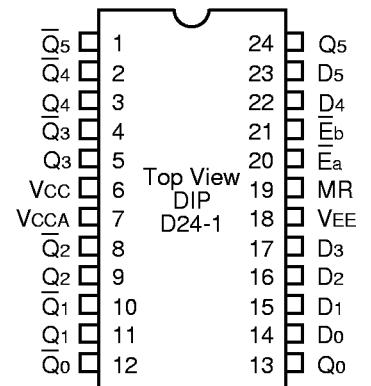
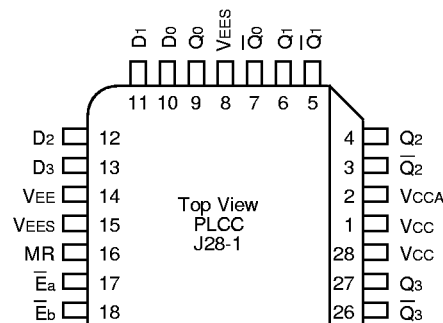
BLOCK DIAGRAM



DESCRIPTION

The SY100S350 offers six high-speed D-Latches with both true and complement outputs, and is performance compatible for use with high-performance ECL systems. When both enable signals (\bar{E}_a and \bar{E}_b) are at a logic LOW, the latches are transparent and the input signals (D_0 – D_5) appear at the outputs (Q_0 – Q_5) after a propagation delay. If either or both of the enable signals are at a logic HIGH, then the latches store the last valid data present on its inputs before \bar{E}_a or \bar{E}_b went to a logic HIGH. The Master Reset (MR) overrides all other input signals and takes the outputs to a logic LOW state. All inputs have 75KΩ pull-down resistors.

PIN CONFIGURATIONS



PIN NAMES

Pin	Function
D ₀ — D ₅	Data Inputs
\bar{E}_a, \bar{E}_b	Common Enable Inputs (Active LOW)
MR	Asynchronous Master Reset Input
Q ₀ — Q ₅	Data Outputs
\bar{Q}_0 — \bar{Q}_5	Complementary Data Outputs
VEES	VEE Substrate
VCCA	Vcco for ECL Outputs

TRUTH TABLE⁽¹⁾

Each Latch

Inputs				Outputs		Operating Mode
D _n	\bar{E}_a	\bar{E}_b	MR	Q _n	\bar{Q}_n	
H	L	L	L	H	L	Latch
L	L	L	L	L	H	
X	X	H	L	Latched ⁽²⁾	Latched ⁽²⁾	
X	H	X	L	Latched ⁽²⁾	Latched ⁽²⁾	
X	X	X	H	L	H	Asynchronous

NOTES:

- H = HIGH State
L = LOW State
X = Don't Care

- Retains data that is present before \bar{E} positive transition.

DC ELECTRICAL CHARACTERISTICS

VEE = -4.2V to -5.5V unless otherwise specified; VCC = VCCA = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I _{IH}	Input HIGH Current MR D _n \bar{E}_a, \bar{E}_b	—	—	250	μA	V _{IN} = V _{IH} (Max.)
I _{EE}	Power Supply Current	-98	-78	-49	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERDIP

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = 0^\circ C$		$T_A = +25^\circ C$		$T_A = +85^\circ C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
tPLH tPHL	Propagation Delay D_n to Output	450	1050	450	1050	450	1050	ps	
tPLH tPHL	Propagation Delay \bar{E}_a, \bar{E}_b to Output	450	1150	450	1150	450	1150	ps	
tPLH tPHL	Propagation Delay MR to Output	450	1250	450	1250	450	1250	ps	
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
t _s	Set-up Time, D_n to \bar{E}_n	600	—	600	—	600	—	ps	
t _h	Hold Time, D_n to \bar{E}_n	600	—	600	—	600	—	ps	
t _r	Release Time, MR to \bar{E}_n	1000	—	1000	—	1000	—	ps	
tpw (L)	Pulse Width, \bar{E}_a, \bar{E}_b	1000	—	1000	—	1000	—	ps	
tpw (H)	Pulse Width, MR	1100	—	1100	—	1100	—	ps	

CERPACK

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = 0^\circ C$		$T_A = +25^\circ C$		$T_A = +85^\circ C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
tPLH tPHL	Propagation Delay D_n to Output	300	1000	300	1000	300	1000	ps	
tPLH tPHL	Propagation Delay \bar{E}_a, \bar{E}_b to Output	300	1100	300	1100	300	1100	ps	
tPLH tPHL	Propagation Delay MR to Output	300	1250	300	1250	300	1250	ps	
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
t _s	Set-up Time, D_n to \bar{E}_n	500	—	500	—	500	—	ps	
t _h	Hold Time, D_n to \bar{E}_n	500	—	500	—	500	—	ps	
t _r	Release Time, MR to \bar{E}_n	1000	—	1000	—	1000	—	ps	
tpw (L)	Pulse Width, \bar{E}_a, \bar{E}_b	1000	—	1000	—	1000	—	ps	
tpw (H)	Pulse Width, MR	1000	—	1000	—	1000	—	ps	

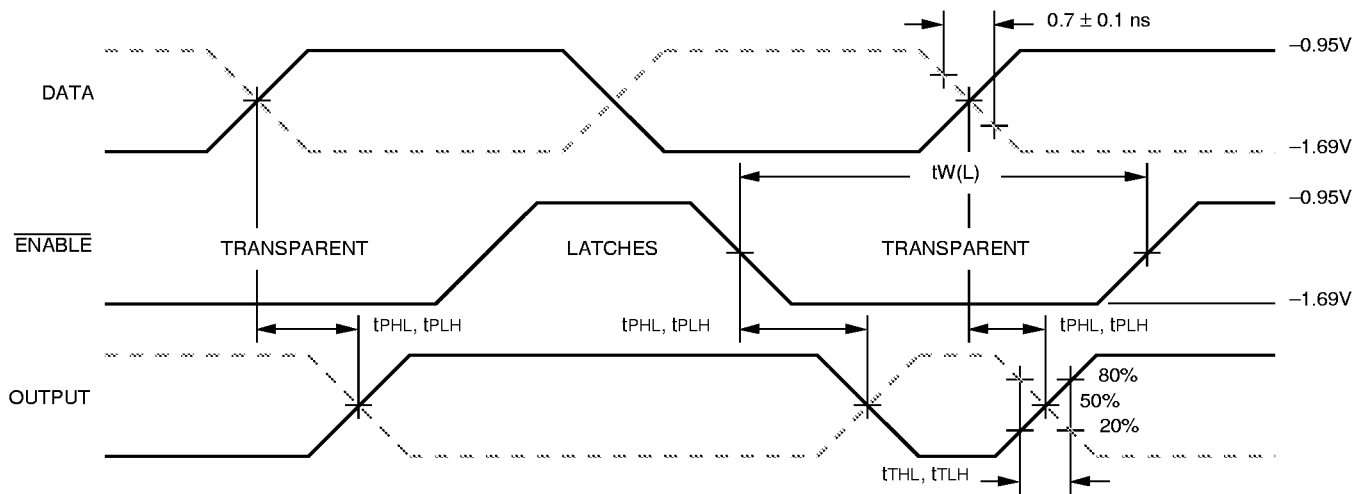
AC ELECTRICAL CHARACTERISTICS (Continued)

PLCC

VEE = -4.2V to -5.5V unless otherwise specified; VCC = VCCA = GND

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
tPLH tPHL	Propagation Delay Dn to Output	300	900	300	900	300	900	ps	
tPLH tPHL	Propagation Delay \bar{E}_a, \bar{E}_b to Output	300	1000	300	1000	300	1000	ps	
tPLH tPHL	Propagation Delay MR to Output	300	1200	300	1200	300	1200	ps	
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
ts	Set-up Time, Dn to \bar{E}_n	500	—	500	—	500	—	ps	
th	Hold Time, Dn to \bar{E}_n	500	—	500	—	500	—	ps	
tr	Release Time, MR to \bar{E}_n	1000	—	1000	—	1000	—	ps	
tPW (L)	Pulse Width, \bar{E}_a, \bar{E}_b	1000	—	1000	—	1000	—	ps	
tPW (H)	Pulse Width, MR	1000	—	1000	—	1000	—	ps	

TIMING DIAGRAMS

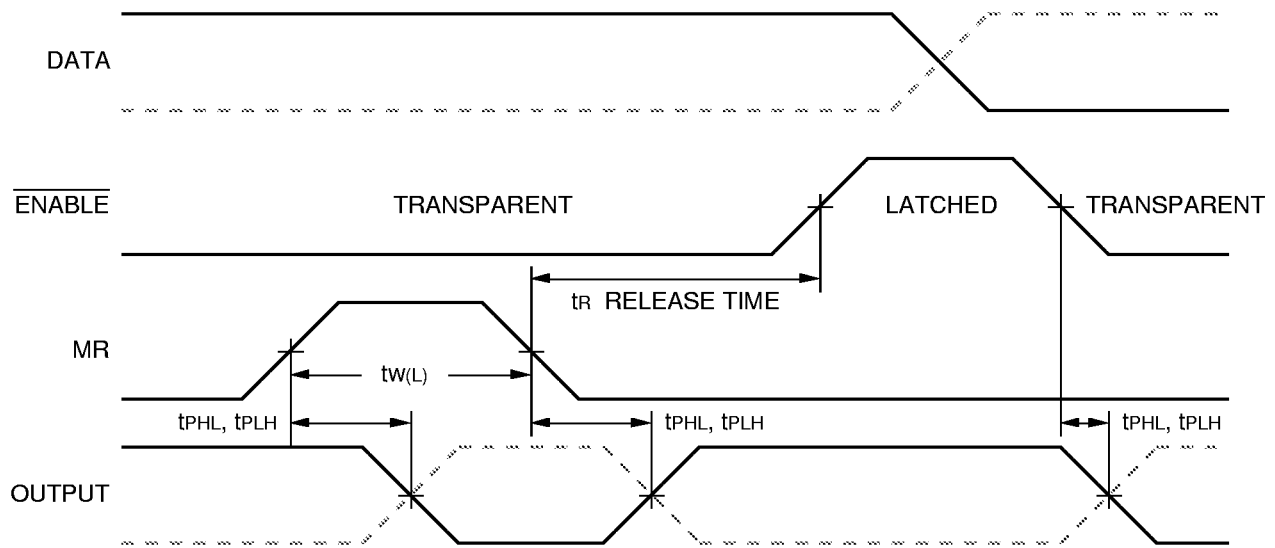


Enable Timing

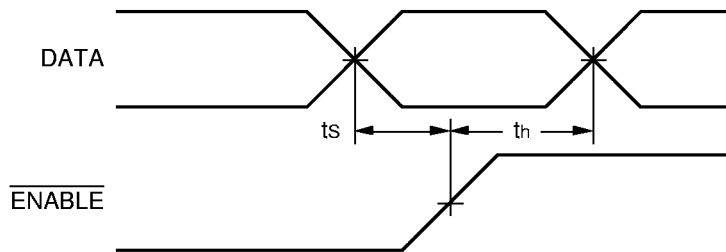
NOTE:

VEE = -4.2V to -5.5V unless otherwise specified; VCC = VCCA = GND

TIMING DIAGRAMS



Reset Timing



Data Set-up and Hold Times

NOTES:

t_s is the minimum time before the transition of the clock that information must be present at the data input.

t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

PRODUCT ORDERING CODE

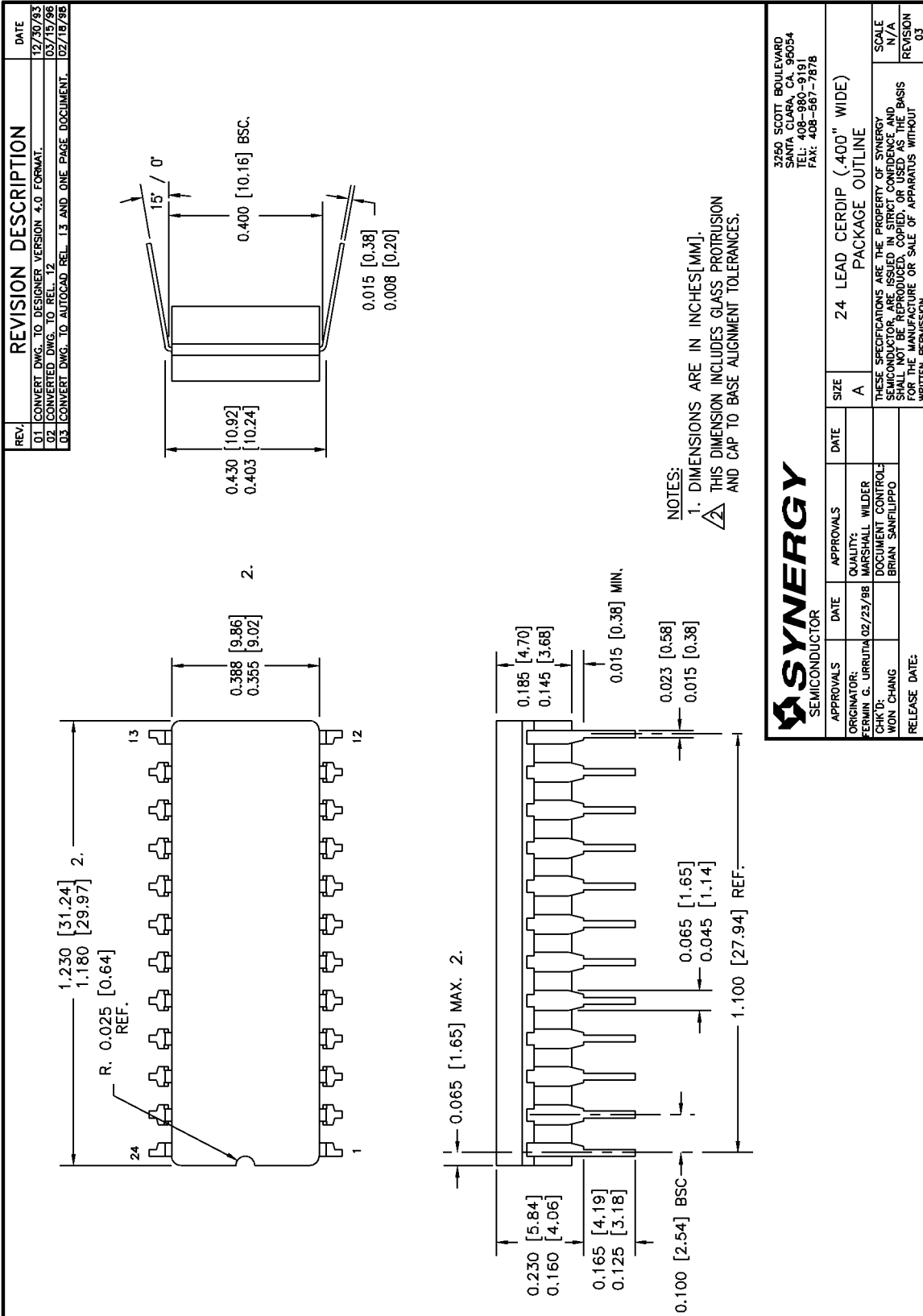
Ordering Code	Package Type	Operating Range
SY100S350DC	D24-1	Commercial
SY100S350FC	F24-1	Commercial
SY100S350JC	J28-1	Commercial
SY100S350JCTR	J28-1	Commercial

24 LEAD CERDIP (D24-1)

FILE/REV #: PD0003A03

PD/0003/ASCORP

PAGE 1 OF 1

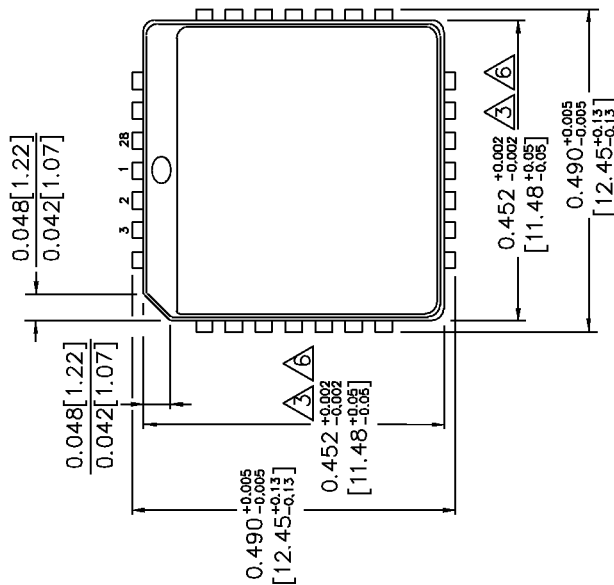


28 LEAD PLASTIC LEADED CHIP CARRIER (J28-1)

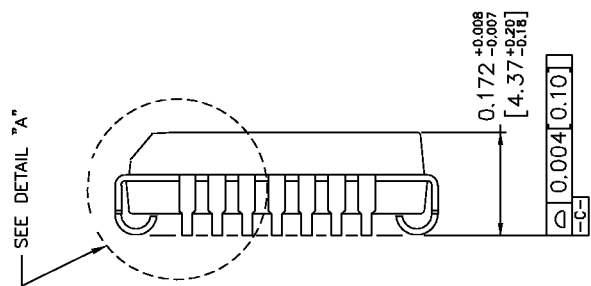
FILE/REV #: PD0008A03
PD/0008/ASCORP
PAGE 1 OF 1

REV	REVISION DESCRIPTION	DATE
01	CONVERT TO DESIGNER VERSION 4.0 FORMAT. ADD COVER PAGE TO SPEC. CHANGE BODY WIDTH DIMENSION FROM 0.450(11.43) TO 0.443(11.25). TYPOGRAPHICAL ERROR.	08/18/94
02	CONVERT DWG FROM DESIGNER TO AUTOCAD REL. 12. REFERENCE AMKOR DWG. NO. 34855 REV. 00.	02/22/96
03	CONVERT DWG TO REL. 13 AND ONE PAGE DOCUMENT.	02/18/98

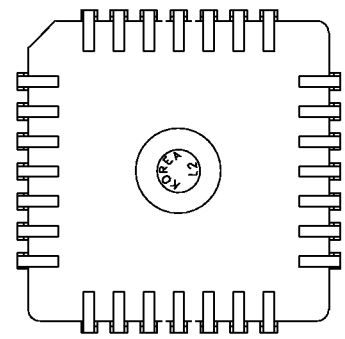
TOP VIEW



SIDE VIEW

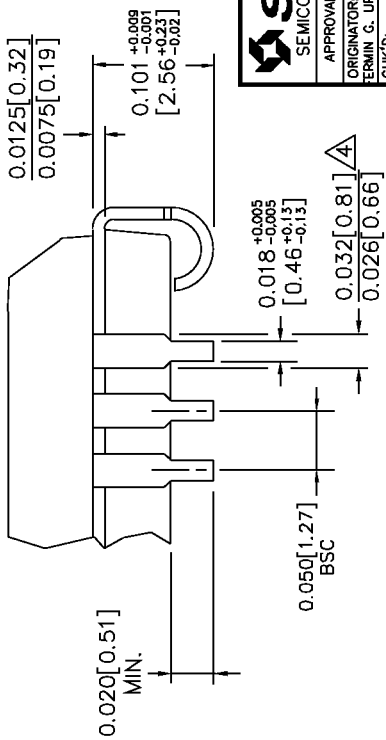


BOTTOM VIEW



NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.



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APPROVALS	DATE	APPROVALS	DATE	SIZE	SCALE
ORIGINATOR: ERWIN G. LIRRUTIA	02/23/98	QUALITY: MARSHALL WILDER		A	N/A
CHK'D: RON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO			REVISION
RELEASE DATE:					03

28 LEAD PLCC
PACKAGE OUTLINE

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DETAIL "A"