Ordering number : ENA0194A

SANYO Semiconductors
DATA SHEET

LV24100LP — Bi-CMOS IC
FM and AM Tuner IC for Small Portable Equipment

Overview

The LV24100LP is an innovative FM/AM tuner IC that is capable of configuring an FM/AM radio with just one external component. Since all the FM/AM radio functions are incorporated into a compact VQLP package with dimensions of only 5mm×5mm×0.8mm, this IC can easily incorporate FM/AM tuner function into mobile phones, PDA, MP3 player and other small mobile sets where space is always at a premium.

Functions

- FM Tuner
- AM Tuner
- MPX stereo decoder
- Tuning

Features

- No external components required except for an AM bar antenna.
- No alignments necessary
- Improved selectivity with low FMIF frequency (110kHz)
- Built-in adjacent channel interference total reduction (no 114kHz, no 190kHz)
- New tuning system
- Very high sensitivity reception with low-noise mixer input circuit
- Built-in low power standby mode eliminates the need for a power switch circuit.
- Composite output for RDS applications
- 3-wire bus interface (data, clock, and NR-W) featured
- Digital AFC function provided
- Soft muting and stereo blend functions (8-step software control)
- Support for manual search, automatic search, and auto preset
- Support for reception of worldwide bands
  (reception of all bands in Japan, Europe, and the US enabled by changes in the program.)

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Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max	Analog block supply voltage	5.0	V
	V_{DD} max	Digital block supply voltage	4.5	V
Digital input voltage	$V_{IN}1$ max	Clock, Data, NR_W	V_{DD}+0.3	V
	$V_{IN}2$ max	External_clk_in	V_{DD}+0.3	V
Allowable power dissipation	Pd max	Ta≤70°C, Mounted on a specified board *	140	mW
Operating temperature	Topr		-20 to +70	°C
Storage temperature	Tstg		-40 to +125	°C

Note: Mounted on a specified board: 40mm×50mm×0.8mm, glass epoxy

Operating Condition at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}	Analog block supply voltage	3.0	V
	V_{DD}	Digital block supply voltage	3.0	V
Operating supply voltage range	V_{CC} op		3.0 to 4.8	V
	V_{DD} op		3.0 to 4.0	V
	V_{IO} op	Interface voltage	1.8 to 4.0	V

Note: The V_{IO} application voltage must be either equivalent to V_{DD} or the V_{DD} value or less. ($V_{IO} \leq V_{DD}$)

Interface Block Allowable Operation Range at Ta = -20 to +70°C, V_{IO} = 3.0V, V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		2.5		4.0	V
Digital block input	V_{IH}	High level input voltage range	0.7V_{DD}		V_{DD}	V
	V_{IL}	Low level input voltage range	0		0.6	V
Digital block output	I_{OL}	Output current at Low level	2.0			mA
	V_{OL}	Output voltage at Low level I_{OL}=2mA			0.6	V
Clock input operating frequency	fclk	(Pin29) clock frequency for 3wire_bus			0.7	MHz
External clock operating frequency	fclk_ext	(Pin31) clock frequency for external input	32k		14M	Hz
External clock operating voltage	Vclk_ext	(Pin31) clock voltage for external input	0.7V_{DD}		V_{DD}	V

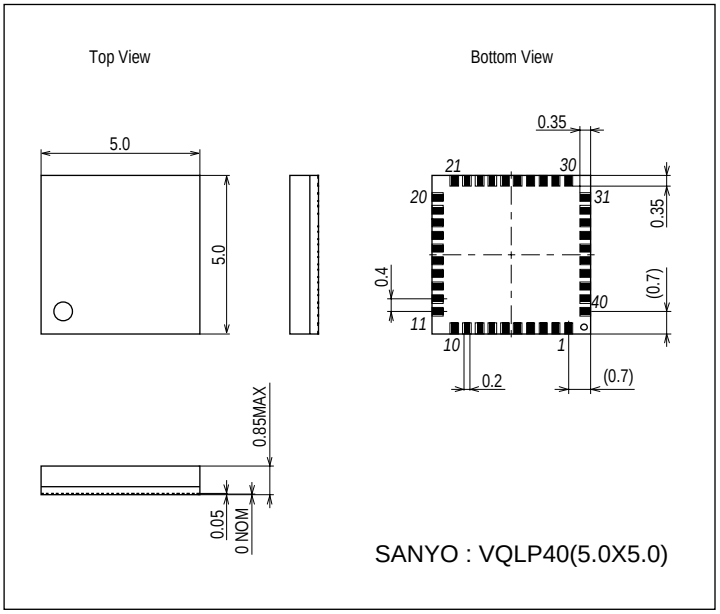
Note: External clock input (pin31) allows also input of the sine wave signal. Frequency deviation is need 250ppm.

Operating Characteristics at Ta=25°C, V_{CC}=3.0V, V_{DD}=3.0V, V_{IO}=3.0V, V_{SS}=0V, Soft Mute/Soft Stereo=off, with the specified test circuit.
Output level setting means control register Block 2, Register 07h Bit 6(VOLSH)=0, Register 09h Bit 0 (nAUBST) =0.

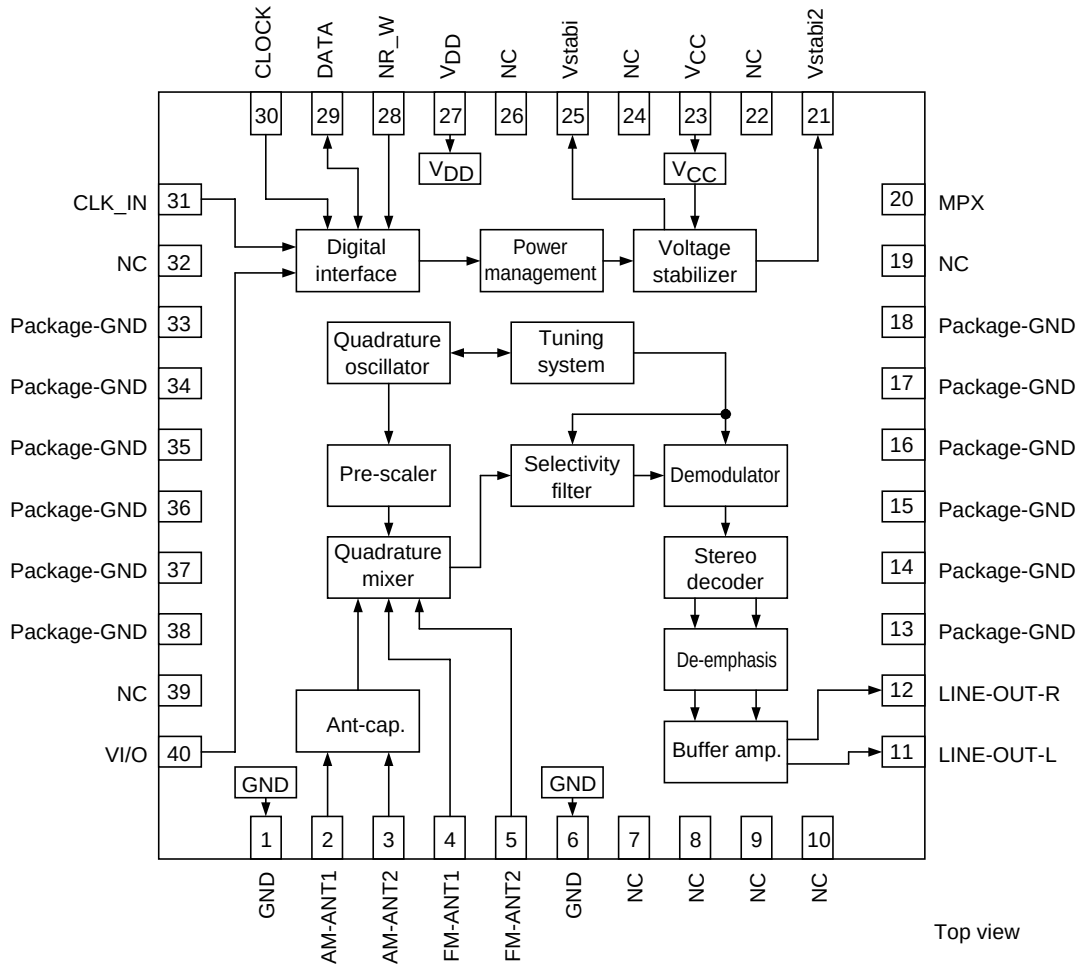
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain (in operation)	ICCA_FM	Measurement at pin 23 with FM 60dBμV monaural input of the analog section.	11	14	17	mA
	ICCA_AM	Measurement at pin 23 with AM 80dBμV input of the analog section.	9	12	15	
	ICCD	Measurement at pins 27 and 40 with FM 60dBμV input in the digital block.	0.1	0.5	0.8	
Current drain (in standby)	ICCA_stb	Measurement at pin 23 in the standby mode of the analog block.		3	30	μA
	ICCD_stb	Measurement at pins 27 and 40 in the standby mode of the digital block.		3	30	
FM receive band	F_range	In the PCB mounting conditions	76		108	MHz
FM receiving characteristics MONO : fc=80MHz, fm=1kHz, 22.5kHz dev. V_{IN}=60dBμV, Audio filter=IHF_BPF						
3dB sensitivity	-3dB LS	22.5kHz dev. output standard, input -3dB.		5	11	dBμV
Practical sensitivity 1	QS1	Input level with S/N=30dB		10	16	dBμV
Practical sensitivity 2 (Reference)	QS2	Input level with S/N=26dB		1.25		μV
Demodulator output	V_O	Pin11 output	50	70	110	mV
Channel balance	CB	Pin11/pin12 output	-2	0	2	dB
Signal-to-noise ratio	S/N	Pin11 output	48	58		dB
Total harmonic distortion 1 (MONO)	THD1	Pin11 output, 22.5kHz dev.		0.4	1.5	%
Total harmonic distortion 2 (MONO)	THD2	Pin11 output, 75kHz dev.		1.3	3.0	%
Field intensity display level	FS	Input level at which FS3 changes to FS4	35		49	dBμV
Mute attenuation	Mute-Att	Pin 11 output	60	70		dB
FM receive characteristic STEREO characteristic : fc=80MHz, fm=1kHz, V_{IN}60dBμV, L+R=90% (67.5kHz dev.), Pilot=10% (7.5kHz dev.), Audio filter = IHF_BPF+15kHz_LPF						
Separation	SEP	L-mod, Pin11/pin12 output	20	35		dB
Total harmonic distortion (Main)	THD-ST	Main-mod (for L+R input), Pin11 output		1.3	3.0	%
AM receive characteristic : fc=1.2MHz, fm=1kHz, 30% mod, Audio filter = IHF_BPF						
Demodulation output 1	V_O1	V_{IN}=30dBμV, Pin11 output	35	55	80	mVrms
Demodulation output 2	V_O2	V_{IN}=80dBμV, Pin11 output	30	50	75	mVrms
Signal-to-noise ratio 1	S/N1	V_{IN}=30dBμV, Pin11 output	14	21		dB
Signal-to-noise ratio 2	S/N2	V_{IN}=80dBμV, Pin11 output	40	45		dB
Total harmonic distortion	THD	V_{IN}=80dBμV, Pin11 output		1.0	3.0	%
Field intensity display level	FS	Input level at which FS3 changes to FS4	35		49	dBμV

Package Dimensions

unit : mm (typ)
3302A



Block Diagram and Pin Assigment



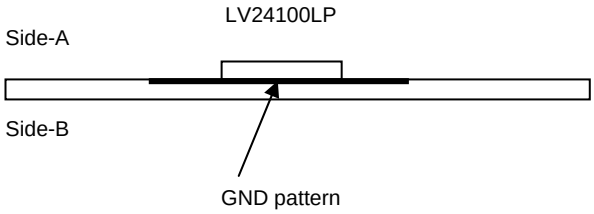
Pin Discription

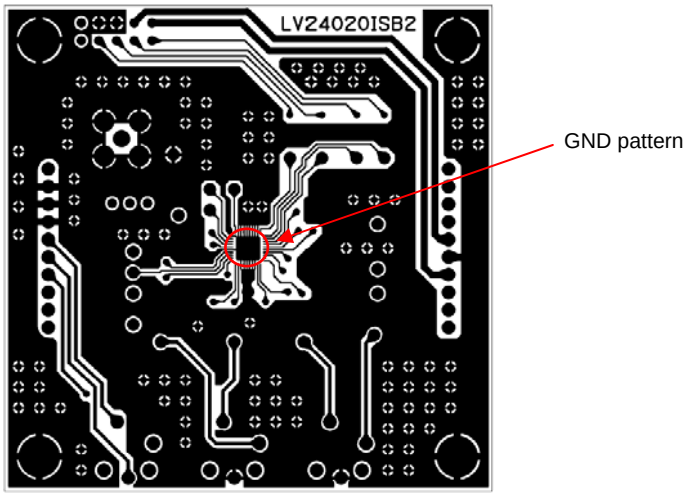
Pin	Name	I/O	Description	Remarks	DC Voltage
1	GND		Analog and Digital GND		
2	AM-ANT1	I	AM Antenna input		
3	AM-ANT2	I	AM Antenna GND		
4	FM-ANT1	I	FM Antenna input		
5	FM-ANT2	I	FM Antenna GND		
6	GND		Analog and Digital GND		
7	NC				
8	NC				
9	NC				
10	NC				
11	LINE-OUT-L	O	Radio Lch Line-output		1.2V
12	LINE-OUT-R	O	Radio Rch Line-output		1.2V
13	Package-shield GND		GND for Package-shield		
14	Package-shield GND		GND for Package-shield		
15	Package-shield GND		GND for Package-shield		
16	Package-shield GND		GND for Package-shield		
17	Package-shield GND		GND for Package-shield		
18	Package-shield GND		GND for Package-shield		
19	NC				
20	MPX		MPX-signal output		V_{CC}-0.3V
21	Vstabi2		2nd Stabilizer voltage		3.0V
22	NC				
23	V_{CC}		Analog supply voltage		
24	NC				
25	Vstabi.		Stabilizer voltage		2.4V
26	NC				
27	V_{DD}		Digital supply voltage		
28	NR_W	I	Digital interface Read/Write		
29	DATA	I/O	Digital interface DATA		
30	CLOCK	I	Digital interface Clock		
31	CLK_IN	I	Reference clock-source input for measurement	Connect to GND if not used	
32	NC				
33	Package-shield GND		GND for Package-shield		
34	Package-shield GND		GND for Package-shield		
35	Package-shield GND		GND for Package-shield		
36	Package-shield GND		GND for Package-shield		
37	Package-shield GND		GND for Package-shield		
38	Package-shield GND		GND for Package-shield		
39	NC				
40	VI/O		Digital interface supply voltage		

The PCB mounting conditions which cover FM receiving frequency range 76MHz to 108MHz

This IC Package is printed inductor backside of the package for local oscillation. It is necessary to place GND pattern right under the IC package for covering received frequency range 76MHz to 108MHz.
This IC is measured under this condition for received frequency range. Then, the GND pattern must be placed at the center of the IC.

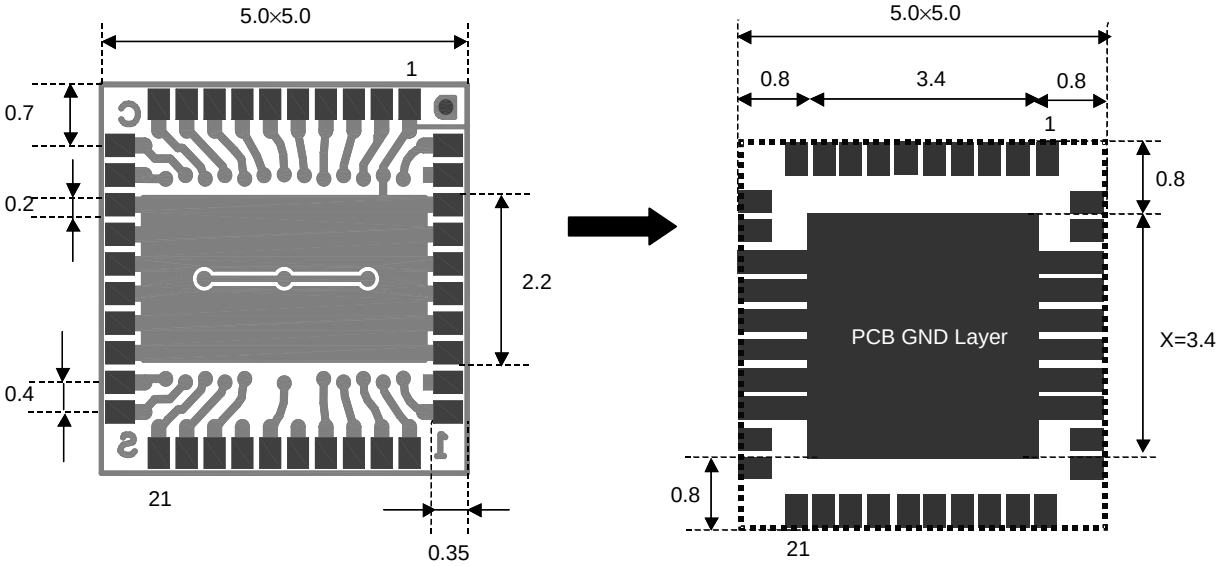
Printed circuit board





LV24100LP Evaluation board side-A

PCB layout recommendations



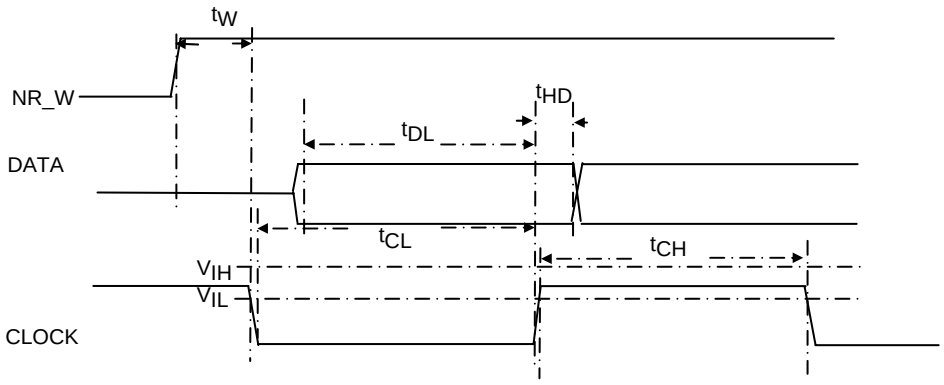
Substrate layout of LV24100LP

PCB pattern light under of LV24100LP

At the GND pattern light under of LV24100LP, X=3.4mm is recommended.
The limit of X is min=2.2mm and max=3.6mm same as GND shield size of LV24100LP.
Please do not arrange other wirings as much as possible within 0.4mm under the GND pattern.

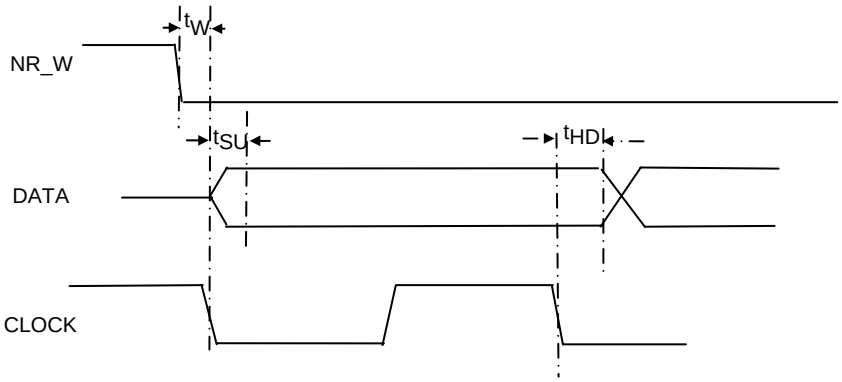
Serial Data Timing

• Write timing



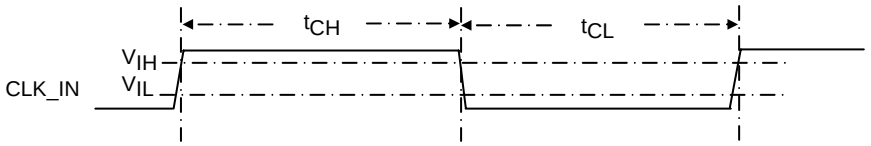
Symbol	Conditions	Ratings			Unit
		min	typ	max	
t_W	Delay from command to data	750			ns
t_{DL}	Delay from data stable to data latch time	750			ns
t_{HD}	Data Hold time	750			ns
t_{CH}	Clock High-level time	750			ns
t_{CL}	Clock Low-level time	750			ns

• Read timing



Symbol	Conditions	Ratings			Unit
		min	typ	max	
t_W	Delay from command to 1st data bit	350			ns
t_{SU}	Data Setup time			350	ns
T_{HD}	Data hold time			350	ns

• External clock timing (Pin 31)



Symbol	Conditions	Ratings			Unit
		min	typ	max	
t_{CH}	Clock High-level time	36	-	15625	ns
t_{CL}	Clock Low-level time	36	-	15625	ns
f_{ext}	External clock frequency	32	-	14000	kHz
V_{IH}	High level input voltage level	$0.7V_{DD}$	-	V_{DD}	V
V_{IL}	Low level input voltage level	0	-	0.6	V

Digital Interface

• 3-wire bus (For communication line)

Access to the LV24100 is done through the 3-wire bus.

CLOCK	Data strobe, input to the LV24100
NR_W	Command (Read or write data), input to the LV24100
DATA	Bi-directional pin: Written data in to the LV24100 when NR_W is high, Read data from the LV24100 when NR_W is low.

The LV24100 can be configured to generate interrupt through the DATA-line. When interrupt mode is selected, care should be taken that the DATA-line connection to the application micro-controller also supports interrupt.

When the required timing window for frequency measurements is not generated by the application micro-controller, an external clock must be connected to CLK_IN pin of the LV24100.

• Register map

The LV24100 registers are divided in 3 blocks:

Block 01h	Status and measurement
Block 02h	FM Control
Block 03h	AM control

To access a register in a block, the block must be first selected by writing the block number to the BLK_SEL register. Block selection can be skipped for subsequent accesses to other registers in the same block.

The mapping is as follows:

Block	Address	Register name	Access	Operation
01h	00h	CHIP_ID	R	Chip identification
	01h	BLK_SEL	W	Block Select
	02h	MSRC_SEL	W	Measure source select
	03h	FM_OSC	W	DAC control for FM-RF oscillator
	04h	SD_OSC	W	DAC control for stereo decoder oscillator
	05h	IF_OSC	W	DAC control for IF oscillator
	06h	CNT_CTRL	W	Counter control
	07h	NA	-	
	08h	IRQ_MSK	W	Interrupt mask
	09h	FM_CAP	W	CAP bank control for RF-frequency
	0Ah	CNT_L	R	Counter value low byte
	0Bh	CNT_H	R	Counter value high byte
	0Ch	CTRL_STAT	R	Control status
	0Dh	RADIO_STAT	R	Radio station status
	0Eh	IRQ_ID	R	Interrupt identify
	0Fh	IRQ_OUT	W	Set Interrupt on DATA-line
02h	01h	BLK_SEL	W	Access register 01h of block 1
	02h	RADIO_CTRL1	W	Radio control 1
	03h	IF_CENTER	W	IF Center Frequency
	04h	AM_CAP	W	All to be set to “0”
	05h	IF_BW	W	IF Bandwidth
	06h	RADIO_CTRL2	W	Radio control 2
	07h	RADIO_CTRL3	W	Radio control 3
	08h	STEREO_CTRL	W	Stereo control
	09h	AUDIO_CTRL1	W	Audio control 1
	0Ah	AUDIO_CTRL2	W	Audio control 2
	0Bh	PW_SCTRL	W	Power and soft control
03h	01h	BLK_SEL	W	Access register 01h of block 1
	02h	AM_ACAP	W	AM antenna capacitor
	03h	AM_FE	W	AM front end control
	04h	AM_CTRL	W	AM control

Not mentioned registers are not defined and should not be accessed.

Register Description

Block x, Register 01h-BLK_SEL-Block Select Register(Write only)

7	6	5	4	3	2	1	0
BN[7:0]							

Bit 7-0: **BN[7:0]**: 8-bit block number. For LV24100, the following numbers are valid:
01h.
02h.
03h.

Note: This register can be accessed from any block

Block 1, Register 00h-CHIP_ID-Chip Identify Register(Read only)

7	6	5	4	3	2	1	0
ID[7:0]							

Bit 7-0: **ID[7:0]**: 8-bit chip ID.
For LV24100, value 7 should be read

Block 1, Register 02h-MSRC_SEL-Measurement Source Select Register(Write-only)

7	6	5	4	3	2	1	0
MSR_O	AFC_LVL	AFC_SPD	MSS_RF16	MSS_AM	MSS_SD	MSS_FM	MSS_IF

Bit 7: **MSR_O**: Output measure source to DATA-pin
0 = Measuring source not available at DATA-pin (normal operation).
1 = Measuring source available at DATA-pin (test mode).

Bit 6: **AFC_LVL**: AFC trigger level
0 = AFC is always active (trigger at 0dBµV)
1 = AFC is only active when field strength is above 20dBµV

Bit 5: **AFC_SPD**: AFC speed
0 = AFC adjusts with 3Hz speed
1 = AFC adjusts with 8kHz speed (test mode)

Bit 4: **MSS_RF16**: RF/16 measurement.
0 = Disable RF/16 oscillator measurement
1 = Enable RF/16 oscillator measurement

Bit 3: **MSS_AM**: AM antenna frequency measurement.
0 = Disable AM antenna measurement
1 = Enable AM antenna measurement

Bit 2: **MSS_SD**: Stereo decoder oscillator measurement
0 = Disable stereo decoder oscillator measurement
1 = Enable stereo decoder oscillator measurement

Bit 1: **MSS_FM**: FM RF oscillator measurement
0 Disable FM RF oscillator measurement
1 = Enable FM RF oscillator measurement

Bit 0: **MSS_IF**: IF oscillator measurement
0 = Disable IF oscillator measurement
1 = Enable IF oscillator measurement

Note: Only one of the measurement source MSS_xx bits may be set at a time.
The FM RF frequency is divided by 256 or 16 before it goes to the measuring circuitry.

Block 1, Register 03h-FM_OSC-FM RF Oscillator Register(Write-only)

7	6	5	4	3	2	1	0
FMOSC[7:0]							

Bit 7-0: **FMOSC[7:0]**: DAC value to control the FM RF oscillator (fine step)

Note: Positive DAC control (i.e. the frequency increases with the register's value)
See also FM_CAP register

Block 1, Register 04h-SD_OSC-Stereo Decoder Oscillator Register(Write-only)

7	6	5	4	3	2	1	0
SDOSC[7:0]							

Bit 7-0: **SDOSC[7:0]**: DAC value to control the stereo decoder oscillator

Note: Positive DAC control(i.e. the frequency increases with the register's value)

Block 1, Register 05h-IF–OSC-IF Oscillator Register(Write-only)

7	6	5	4	3	2	1	0
IFOSC[7:0]							

Bit 7-0: **IFOSC[7:0]**: DAC value to control the IF oscillator

Note: Positive DAC control (i.e. the frequency increases with the register's value)

Block 1, Register 06h-CNT–CTRL-Counters Control Register(Write-only)

7	6	5	4	3	2	1	0
CNT1_CLR	CTAB2	CTAB1	CTAB0	SWP_CNT_L	CNT_EN	CNT_SEL	CNT_SET

Bit 7: **CNT1_CLR**: Clear counter 1 bit

0 = Normal mode

1 = Clear and keep counter 1 in reset mode

Bit 6-4: **CTAB[2:0]**: Tab select for counter 2 measuring interval bits

Value	Dec.	Stop value
000b	0	Stop after 2 counts
001b	1	Stop after 8 counts
010b	2	Stop after 32 counts
011b	3	Stop after 128 counts
100b	4	Stop after 512 counts
101b	5	Stop after 2048 counts
110b	6	Stop after 8192 counts
111b	7	Stop after 32768 counts

Bit 3: **SWP_CNT_L**: Swap counter 1 and counter 2 bit(Active low)

0 = Clock source 1 to counter 2, clock source 2 to counter 1(swapping)

1 = Clock source 1 to counter 1, clock source 2 to counter 2(no swap)

Bit 2: **CNT_EN**: Enable the currently selected counter bit

0 = Disable counter(stop counting)

1 = Enable counter(counting mode)

Bit 1: **CNT_SEL**: counter select bit

0 = Select counter 1 for measurement

1 = Select counter 2 for measurement

Bit 0: **CNT_SET**: Set counters bit

0 = Normal mode

1 = Set both counter 1 and counter 2 to FFFFh and keep them set

Block 1, Register 08h-IRQ–MSK-Interrupt Mask Register(Write-only)

7	6	5	4	3	2	1	0
Reserved	IM_MS	Reserved		IRQ_LVL	IM_AFC	IM_FS	IM_CNT2

Bit 7: **Reserved**: Must be programmed with 0.

Bit 6: **IM_MS**: Mono/Stereo interrupt mask bit

0 = Disable mono/stereo change interrupt

1 = Enable mono/stereo change interrupt

Bit 5: **Reserved**: Must be programmed with 0.

Bit 4: **Reserved**: Must be programmed with 0.

Bit 3: **IRQ_LVL**: Interrupt level select bit

0 = Drive DATA-line from low to high when interrupt occurs(active high)

1 = Drive DATA-line from high to low when interrupt occurs(active low)

Bit 2: **IM_AFC**: AFC out of range interrupt mask bit

0 = Disable AFC out of range interrupt

1 = Enable AFC out of range interrupt

Bit 1: **IM_FS**: Field strength change interrupt mask bit

0 = Disable field strength change interrupt

1 = Enable field strength change interrupt

Bit 0: **IM_CNT2**: Counter 2 counting done interrupt mask bit

0 = Disable counter 2 counting done interrupt

1 = Enable counter 2 counting done interrupt

Block 1, Register 09h-FM_CAP-FM RF Capacitor Bank Register(Write-only)

7	6	5	4	3	2	1	0
FMCAP[7:0]							

Bit 7-0: **FMCAP[7:0]**: CAP bank value to control the FM RF frequency (coarse steps)

Note: 7½ bit CAP value (Bit[7:6]: Combination 10b and 01b results in the same CAP-range)

Negative control: de RF frequency decreases when increasing the register's value

See also FM_OSC register

Block 1, Register 0Ah-CNT_L-Counter Value Low Register(Read-only)

7	6	5	4	3	2	1	0
CNT_LSB[7:0]							

Bit 7-0: **CNT_LSB[7:0]**: Lower 8-bit value of the 16 bit counter

Block 1, Register 0Bh-CNT_H-Counter Value High Register(Read-only)

7	6	5	4	3	2	1	0
CNT_MSB[7:0]							

Bit 7-0: **CNT_MSB[7:0]**: Upper 8-bit value of the 16 bit counter

Block 1, Register 0Ch-CTRL_STAT-Control Status Register(Read-only)

7	6	5	4	3	2	1	0
REV3	REV2	REV1	REV0	Reserved		COV_FLG	AFC_FLG

Bit 7-4: **REV[3:0]**: should be read as 0Dh

Bit 3-2: **Reserved[1:0]**: should be read as all 1

Bit 1: **COV_FLG**: counter overflow flag

0 = No overflow of the internal counter

1 = The last counting loop causes overflow of the internal counter

Bit 0: **AFC_FLG**: AFC out of range bit

0 = AFC is within control range

1 = AFC is out of control range

Note: Reading this register will clear AFC, count 2 done interrupt.

COV_FLG is clear when CLR_CNT1 bit of CNT_CTRL register is high

Block 1, Register 0Dh-RADIO_STAT-Radio Station Status Register(Read-only)

7	6	5	4	3	2	1	0
RSS_MS	RSS_FS						

Bit 7: **RSS_MS**: Radio station mono/stereo state bit

0 = Mono

1 = Stereo

Bit 6-0: **RSS_FS[6:0]**: Radio station field strength bits

1111111b = Field strength less then 10dBµV

0111111b = Field strength between 10 to 20dBµV

0011111b = Field strength between 20 to 30dBµV

0001111b = Field strength between 30 to 40dBµV

0000111b = Field strength between 40 to 50dBµV

0000011b = Field strength between 50 to 60dBµV

0000001b = Field strength between 60 to 70dBµV

0000000b = Field strength above 70dBµV

Note: Reading this register will clear field strength and mono/stereo interrupt

Block 1, Register 0Eh-IRQ–ID-Interrupt Identify Register(Read-only)

7	6	5	4	3	2	1	0
Reserved		II_CNT2	Reserved	II_AFC	Reserved		II_FS_MS

Bit 7: **Reserved**: should be read as 1
Bit 6: **Reserved**: should be read as 1
Bit 5: **II_CNT2**: Counter 2 counting done flag
0 = No counting 2 counting done interrupt
1 = Measuring with counter 2 is done
Bit 4: **Reserved**: should be read as 0
Bit 3: **II_AFC**: AFC out of range interrupt bit
0 = No AFC interrupt
1 = AFC fails to hold the RF-frequency in range
Bit 2: **Reserved**: should be read as 0
Bit 1: **Reserved**: should be read as 0
Bit 0: **II_FS_MS**: Field strength and Mono/stereo interrupt bit
0 = No change in either the field strength or the mono/stereo mode
1 = Change in field strength bits detected or mono/stereo mode has changed

Block 1, Register 0Fh-IRQ–OUT-Set Interrupt Out Register(Write Only)

7	6	5	4	3	2	1	0
IRQO_VAL[7:0]							

Bit 7-0: **IRQO_VAL[7:0]**: Write any value to this register will select the interrupt as output on the DATA-line of the LV24100 (the DATA-line can then be used as interrupt pin)

Block 2, Register 02h-RADIO–CTRL1-Radio Control 1 Register(Write-only)

7	6	5	4	3	2	1	0
EN_MEAS	EN_AFC	Reserved	AM_CD2	DIR_AFC	RST_AFC	AM_CD1	AM_CD0

Bit 7: **EN_MEAS**: Enable measurement bit
0 = Normal mode
1 = Measurement mode
Bit 6: **EN_AFC**: Enable AFC bit
0 = Disable AFC
1 = Enable AFC
Bit 5: **EN_RF16**:Enable RF16 Divider bit
0 = Disable RF16
1 = Enable RF16
Bit 4: **AM_CD2**: AM clock divider bit 2. Should be kept at 1 in FM mode
Bit 3: **DIR_AFC**: AFC direction bit
0 = AFC normal direction
1 = AFC reverse direction (for test purpose)
Bit 2: **RST_AFC**: Reset AFC bit
0 = Normal operation
1 = Reset AFC to the middle of the control range
Bit 1: **AM_CD1**: AM clock divider bit 1. Should be kept at 1 in FM mode
Bit 0: **AM_CD0**: AM clock divider bit 0. Should be kept at 1 in FM mode

Note: The AM_CD[2:0] bits are used to scale the FM-RF frequency down to AM-RF frequency. In FM mode, the AM divider should be turned off.

AM_CD[2:0]	Divider factor	Approx. AM-RF (in kHz)	
0	48	1354	2291
1	64	1015	1718
2	80	812	1375
3	96	677	1145
4	128	507	859
5	160	406	687
6	192	338	572
7	Divider OFF		

Block 2, Register 03h-IFCEN–OSC-IF Center Frequency Oscillator Register(Write-only)

7	6	5	4	3	2	1	0
IFCOSC[7:0]							

Bit 7-0: **IFCENT[7:0]**: value for centering the IF frequency

Block 2, Register 04h-AM_CAP(Write-only)

7	6	5	4	3	2	1	0
AM_CAP[7:0]							
Bit 7-0:	**AM_CAP[7:0]**:all bit to be set to 0						

Block 2, Register 05h-IF_BW-IF Bandwidth Register(Write-only)

7	6	5	4	3	2	1	0
IFBW[7:0]							
Bit 7-0:	**IFBW[7:0]**: Value for IF bandwidth						

Block 2, Register 06h-RADIO_CTRL2-Radio Control 2 Register(Write-only)

7	6	5	4	3	2	1	0
VREF2	VREF	STABI_BP	IF_PM_L	DCFB_SPD	DCFB_OFF	AGCSP	Reserved

Bit 7: **VREF2**: V_{REF2} control bit
- 0 = VREF2 is ON
- 1 = $VREF_2$ is OFF

Bit 6: **VREF**: V_{REF} control bit
- 0 = VREF is ON
- 1 = VREF is OFF

Bit 5: **STABI_BP**: Voltage stabilizer bypass bit
- 0 = Internal voltage is V_{stabi} (normal operation)
- 1 = Internal voltage is V_{CC} (stabilizer bypassed)

Bit 4: **IF_PM_L**: IF PLL mute bit
- 0 = IF PLL mute on (presetting IF mode)
- 1 = IF PLL mute off (normal operation mode)

Bit 3: **DCFB_SPD**: DC feedback speed
- 0 = normal speed
- 1 = high speed (test mode)

Bit 2: **DCFB_OFF**: DC feedback control
- 0 = Enable DC feedback (FM mode)
- 1 = Turn off the DC feedback (AM mode)

Bit 1: **AGCSP**: AGC speed control bit
- 0 = Normal speed
- 1 = High speed (test mode)

Bit 0: **Reserved**: should be written with 0

Block 2, Register 07h-RADIO_CTRL3-Radio Control 3 Register(Write-only)

7	6	5	4	3	2	1	0
AGC_SLVL	VOLSH	Reserved	AMUTE_L	SE_FM	SE_AM	Reserved	

Bit 7: **AGC_SLVL**: AGC set level bit
- This bit must be set to 1

Bit 6: **VOLSH**: Volume level shift bit
- 0 = Normal volume level
- 1 = Extra volume of 12dB

Bit 5: **Reserved**: should be written with 0

Bit 4: **AMUTE_L**: Audio mute bit
- 0 = Audio muted
- 1 = Audio not muted

Bit 3: **SE_FM**: FM radio select bit
- 0 = Disable FM radio
- 1 = Enable FM radio

Bit 2: **SE_AM**: AM radio select bit
- 0 = Disable AM radio
- 1 = Enable AM radio

Bit 1: **Reserved**: should be written with 0

Bit 0: **Reserved**: should be written with 0

Note: Do not set bit 3 and 2 on at the same time.

Block 2, Register 08h-STEREO_CTRL-Stereo Control Register(Write-only)

7	6	5	4	3	2	1	0
FRCST	FMCS[2:0]			DLT_TNE	PILOTCANC	SD_PM	ST_M

Bit 7: **FRCST**: Force stereo bit
- 0 = Normal mode
- 1 = Force stereo mode for test

Bit 6-4: **FMCS[2:0]**: FM channel separation bits
- 0…7=FM channel separation level

Bit 3: **DLT_TNE**: Delta tune bit
- 0 = Decrease delta tune
- 1 = Normal delta tune

Bit 2: **PILOTCANC**: Pilot cancellation bit
- 0 = No pilot cancellation
- 1 = Pilot cancellation enabled

Bit 1: **SD_PM**: Stereo decoder PLL mute bit
- 0 = Stereo decoder PLL not muted(normal operation)
- 1 = Stereo decoder PLL is muted(presetting mode)

Bit 0: **ST_M**: FM stereo/mono mode bit
- 0 = Stereo mode
- 1 = Mono mode

Block 2, Register 09h-AUDIO_CTRL1-Audio Control 1 Register(Write-only)

7	6	5	4	3	2	1	0
Reserved							nAUBST

Bit 7-1: **Reserved**: should be written with 0

Bit 0: **nAUBST**: Audio output level boost bit
- 0 = Boost output level with 3dB
- 1 = No output level boosting

Block 2, Register 0Ah-AUDIO_CTRL2-Audio Control 2 Register(Write-only)

7	6	5	4	3	2	1	0
Reserved		DEEMP	Reserved				

Bit 7-6: **Reserved**: should be written with 1

Bit 5: **DEEMP**: De-emphasis bit
- 0 = De-emphasis 50μs.
- 1 = De-emphasis 75μs.

Bit 4-0: **Reserved**: should be written with 0

Block 2, Register 0Bh-PW_SCTRL-Power and Soft Control Register(Write-only)

7	6	5	4	3	2	1	0
SS_CTRL			SM_CTRL			Reserved	PW_RAD

Bit 7-5: **SS_CTRL**: Soft stereo control bits(8 levels)
- 000b = Minimal soft stereo(off)
- 111b = Maximal soft stereo level

Bit 4-2: **SM_CTRL**: Soft audio mute bits(8 levels)
- 000b = Minimal soft audio mute(off)
- 111b = Maximal soft audio mute level

Bit 1: **Reserved**: should be written with 0

Bit 0: **PW_RAD**: Radio circuitry power bit
- 0 = Radio circuitry is switched OFF.
- 1 = Switch radio circuitry ON

Note: PW_RAD is 0 at power up

Block 3, Register 02h-AM_ACAP-AM Antenna Capacitor Bank Register(Write-only)

7	6	5	4	3	2	1	0
AMCAP[7:0]							

Bit 7-0: **AMCAP[7:0]**: CAP bank value to control the AM antenna frequency

Note: AM antenna capacitor bank is controlled by 10 bits. The upper 2 bits are located in AM_FE register.
Negative control: de frequency decreases when increasing the register's value.

Block 3, Register 03h-AM_FE-AM Front End Register(Write-only)

7	6	5	4	3	2	1	0
AGC_LVL			AGC_GAIN			AMCAP9	AMCAP8

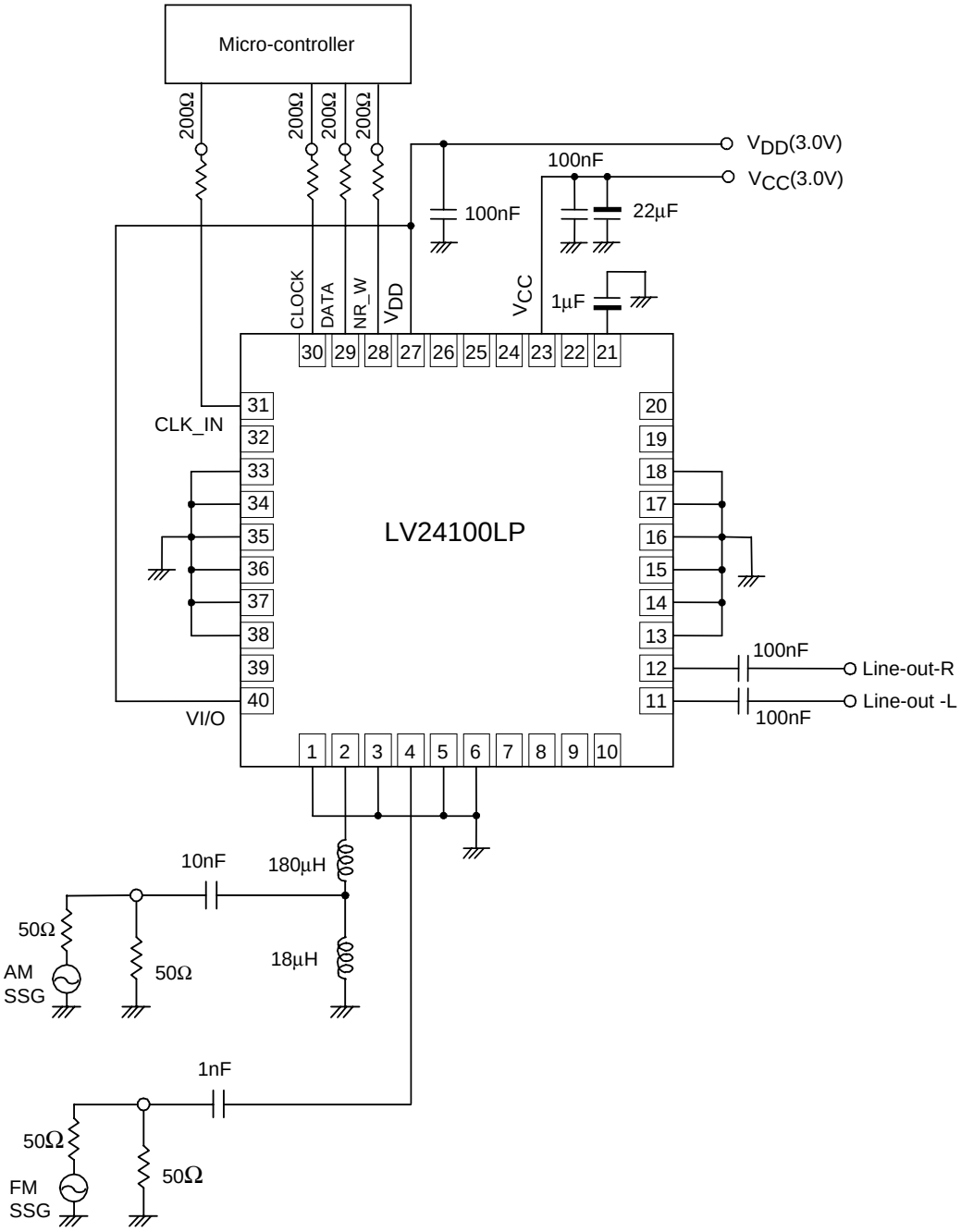
Bit 7-5: **AGC_LVL[2:0]**: AGC level bits
Bit 4: **AAGC_EG**: AM AGC extra gain
Bit 3-2: **AAGC_GAIN[1:0]**: AM AGC gain setting
Bit 1-0: **AMCAP[9:8]**: Upper bits of AM antenna capacitor bank

Block 3, Register 04h-AM_CTRL-AM Control Register(Write-only)

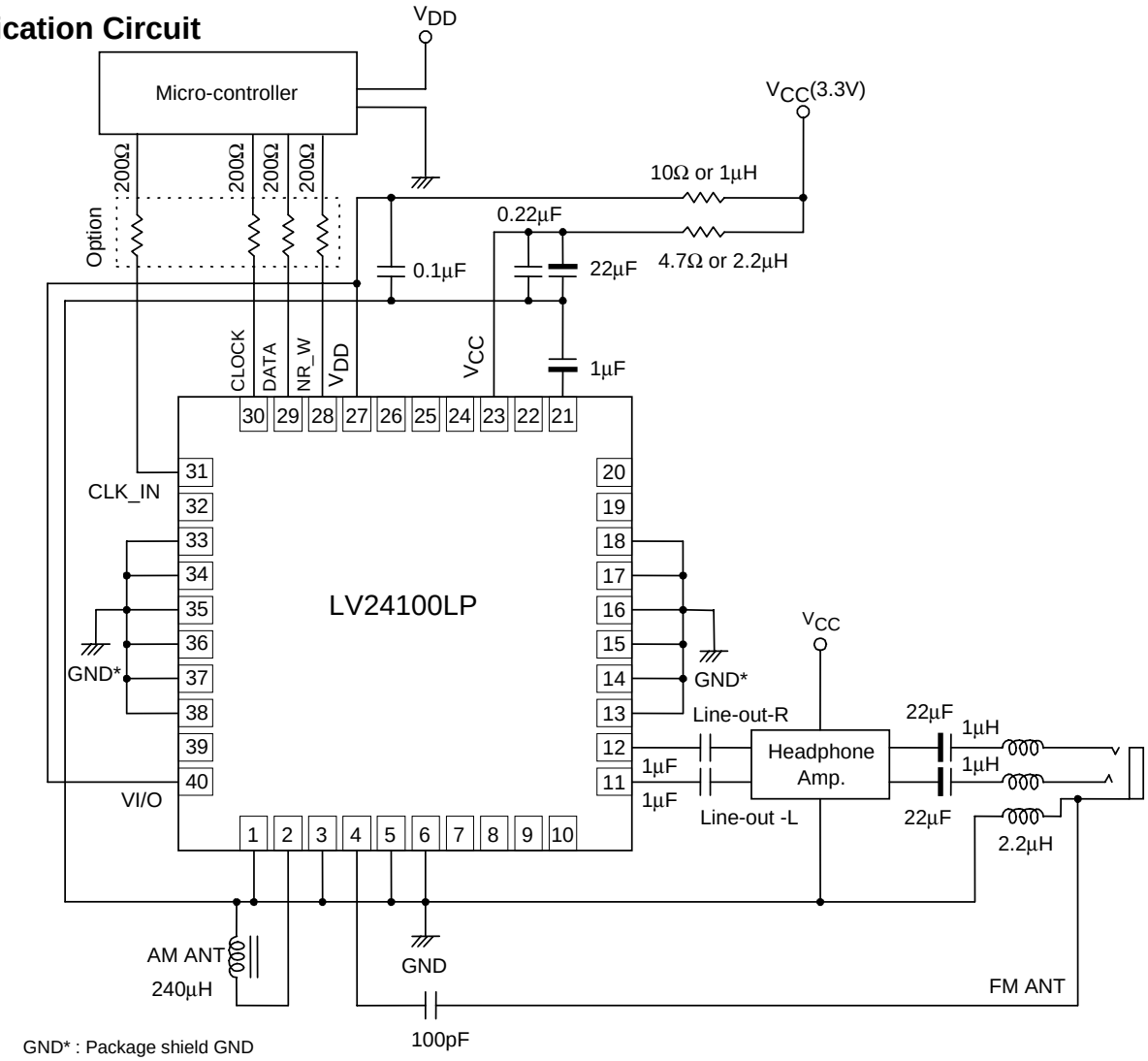
7	6	5	4	3	2	1	0
AMFE_AT	AABSW	nFIFAGC	AMFE_EN	AM_CAL	nAMEMG	FE_SPD[1:0]	

Bit 7: **AMFE_AT**: AM front end attenuator
0 = Disable AM front end attenuator
1 = Enable AM front end attenuator
Note: This bit is don't care for FM and should be 1 for AM
Bit 6: **AABSW**: AM antenna band switch
0 = Switch off AM antenna band
1 = Switch on AM antenna band
Bit 5: **nFIFAGC**: Fast IF AGC(active low)
0 = Fast IF AGC speed
1 = Norma lF AGC speed
Note: This bit must be 0 for FM.
In AM mode, this bit must be 1 and can be changed to 0 during scanning for AM stations to speed up the scan operation.
Bit 4: **AMFE_EN**: Enable AM front end bit
0 = Disable AM front end
1 = Enable AM front end
Bit 3: **AM_CAL**: AM calibration bit
0 = Disable AM calibration(normal operation)
1 = Enable AM calibration(calibrate AM antenna frequency mode)
Note: This bit must be set to 1 before measuring the AM antenna frequency
Bit 2: **nAMEMG**: Extra gain AM mixer bit
0 = Extra mixer gain(normal operation)
1 = No extra mixer gain
Bit 1-0: **FE_SPD[1:0]**: AM front end speed bits

Test Circuit



Application Circuit



GND* : Package shield GND

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