

MOS INTEGRATED CIRCUIT MC-421000A8, 421000A9 SERIES

1 M-WORD BY 8-BIT, 1 M-WORD BY 9-BIT DYNAMIC RAM MODULE FAST PAGE MODE

Description

The MC-421000A8 is a 1 048 576 words by 8 bits dynamic RAM module on which 2 pieces of 4 M DRAM (μ PD424400LA) are assembled.

The MC-421000A9 is a 1 048 576 words by 9 bits dynamic RAM module on which 2 pieces of 4 M DRAM (μ PD424400LA) and 1 piece of 1 M DRAM (μ PD421000LA) are assembled.

These modules provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 1 048 576 words by 8 bits organization (MC-421000A8)
- 1 048 576 words by 9 bits organization (MC-421000A9)
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-421000A8-60	60 ns	120 ns	1 320 mW	11 mW (CMOS level input)
MC-421000A8-70	70 ns	140 ns	1 100 mW	
MC-421000A8-80	80 ns	160 ns	990 mW	
MC-421000A8-10	100 ns	190 ns	880 mW	
MC-421000A9-60	60 ns	120 ns	1 815 mW	16.5 mW (CMOS level input)
MC-421000A9-70	70 ns	140 ns	1 540 mW	
MC-421000A9-80	80 ns	160 ns	1 375 mW	
MC-421000A9-10	100 ns	190 ns	1 210 mW	

- 1 024 refresh cycles/16 ms
- Three refresh modes are available: $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh
- 30-pin single in-line memory module (Pin pitch=2.54 mm)
- All inputs and outputs are TTL compatible
- Single +5.0 V $\pm$ 10 % power supply

The information in this document is subject to change without notice.

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-421000A8BA-60	60 ns	30-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating (HAL)	2 pieces of μ PD424400LA (300 mil SOJ) [Single side]
MC-421000A8BA-70	70 ns		
MC-421000A8BA-80	80 ns		
MC-421000A8BA-10	100 ns		
MC-421000A8FA-60	60 ns	30-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-421000A8FA-70	70 ns		
MC-421000A8FA-80	80 ns		
MC-421000A8FA-10	100 ns		
MC-421000A9BA-60	60 ns	30-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating (HAL)	2 pieces of μ PD424400LA (300 mil SOJ) 1 piece of μ PD421000LA (300 mil SOJ) [Single side]
MC-421000A9BA-70	70 ns		
MC-421000A9BA-80	80 ns		
MC-421000A9BA-10	100 ns		
MC-421000A9FA-60	60 ns	30-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-421000A9FA-70	70 ns		
MC-421000A9FA-80	80 ns		
MC-421000A9FA-10	100 ns		

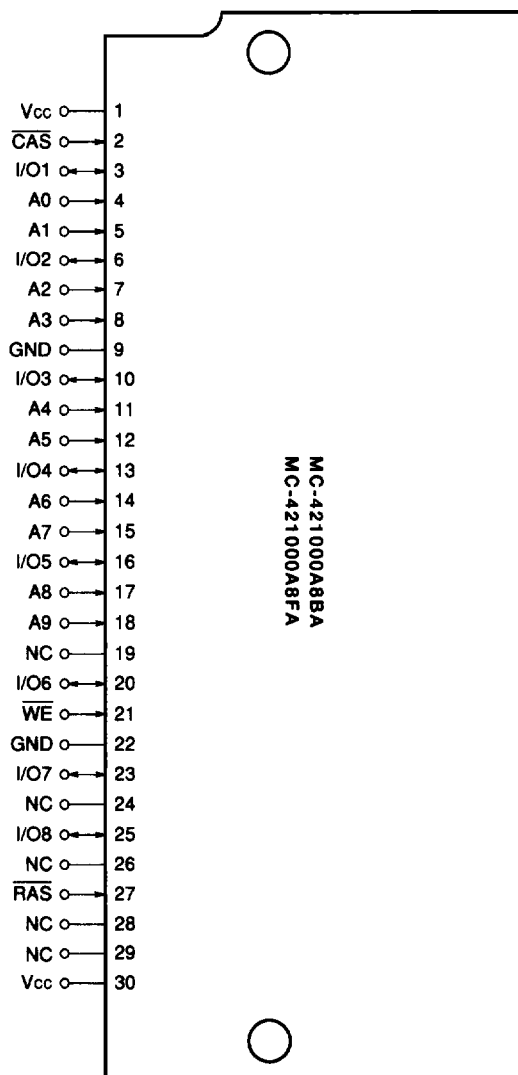
Quality Grade

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

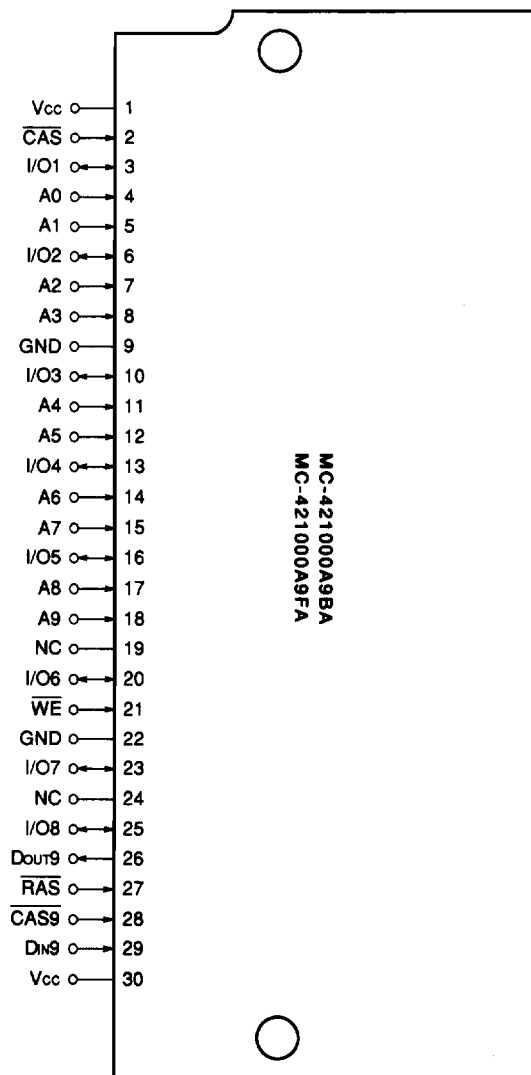
Pin Configurations (Front View)

[MC-421000A8 series]



- A0-A9 : Address Inputs
- I/O1-I/O8 : Data Inputs/Outputs
- $\overline{\text{RAS}}$: Row Address Strobe
- $\overline{\text{CAS}}$: Column Address Strobe
- $\overline{\text{WE}}$: Write Enable
- Vcc : Power Supply
- GND : Ground
- NC : No Connection

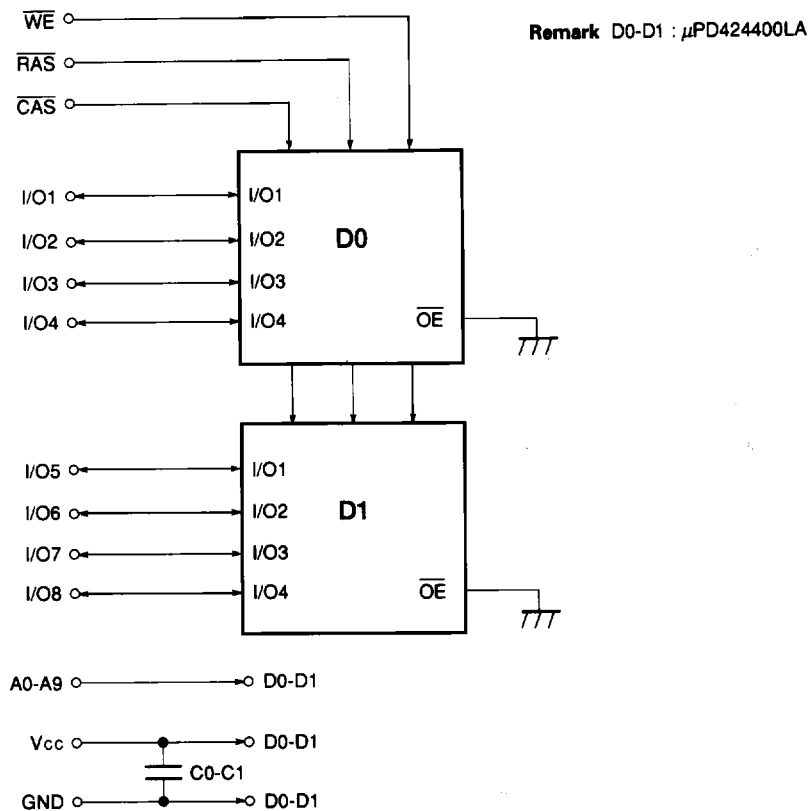
[MC-421000A9 series]



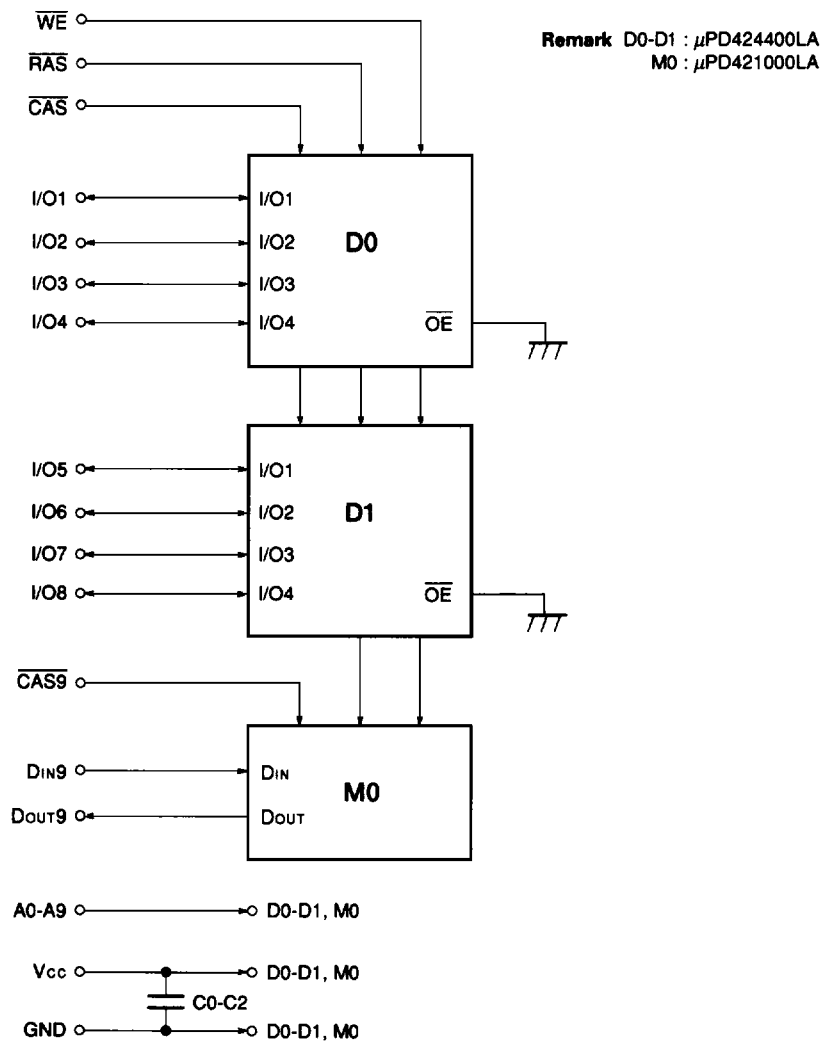
- A0-A9 : Address Inputs
- I/O1-I/O8 : Data Inputs/Outputs
- Din9 : Data Input
- Dout9 : Data Output
- $\overline{\text{RAS}}$: Row Address Strobe
- $\overline{\text{CAS}}$, $\overline{\text{CAS9}}$: Column Address Strobe
- $\overline{\text{WE}}$: Write Enable
- Vcc : Power Supply
- GND : Ground
- NC : No Connection

Block Diagrams

[MC-421000A8 series]



[MC-421000A9 series]



Electrical Specifications Notes1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		-1.0 to +7.0	V
Supply voltage	V_{CC}		-1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D	MC-421000A8	2	W
		MC-421000A9	3	
Operating temperature	T_{OP1}		0 to +70	°C
Storage temperature	T_{stg}		-55 to +125	°C

Remark Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		$V_{CC}+1.0$	V
Low level input voltage	V_{IL}		-1.0		+0.8	V
Ambient temperature	T_a		0		70	°C

Capacitance ($T_a = +25\text{ }^{\circ}\text{C}$, $f = 1\text{ MHz}$)

[MC-421000A8 series]

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	A0-A9, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$			24	pF
Data Input/Output capacitance	$C_{I/O}$	I/O1-I/O8			12	pF

[MC-421000A9 series]

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0-A9, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$			31	pF
	C_{I2}	$\overline{\text{CAS9}}$, D_{IN9}			17	pF
Data Input/Output capacitance	$C_{I/O}$	I/O1-I/O8			12	pF
Data Output capacitance	C_O	D_{OUT9}			17	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)
[MC-421000A8 series]

Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC(MIN.)}}$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	240	mA	3,4
			$t_{\text{RAC}} = 70 \text{ ns}$	200		
			$t_{\text{RAC}} = 80 \text{ ns}$	180		
			$t_{\text{RAC}} = 100 \text{ ns}$	160		
Standby current	I _{CC2}	$V_{\text{IH(MIN.)}} \leq \overline{\text{RAS}}, \overline{\text{CAS}}$ $I_o = 0 \text{ mA}$		4	mA	
		$V_{\text{CC}} - 0.2 \text{ V} \leq \overline{\text{RAS}}, \overline{\text{CAS}}$ $I_o = 0 \text{ mA}$		2		
$\overline{\text{RAS}}$ only refresh current	I _{CC3}	$\overline{\text{RAS}}$ Cycling $V_{\text{IH(MIN.)}} \leq \overline{\text{CAS}}$ $t_{\text{RC}} = t_{\text{RC(MIN.)}}$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	240	mA	3,4
			$t_{\text{RAC}} = 70 \text{ ns}$	200		
			$t_{\text{RAC}} = 80 \text{ ns}$	180		
			$t_{\text{RAC}} = 100 \text{ ns}$	160		
Operating current (Fast page mode)	I _{CC4}	$\overline{\text{CAS}}$ Cycling $\overline{\text{RAS}} \leq V_{\text{IL(MAX.)}}$ $t_{\text{PC}} = t_{\text{PC(MIN.)}}$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	180	mA	3,4
			$t_{\text{RAC}} = 70 \text{ ns}$	160		
			$t_{\text{RAC}} = 80 \text{ ns}$	140		
			$t_{\text{RAC}} = 100 \text{ ns}$	120		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current	I _{CC5}	$\overline{\text{RAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC(MIN.)}}$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	240	mA	3,4
			$t_{\text{RAC}} = 70 \text{ ns}$	200		
			$t_{\text{RAC}} = 80 \text{ ns}$	180		
			$t_{\text{RAC}} = 100 \text{ ns}$	160		
Input leakage current	I _{I(L)}	$V_i = 0 \text{ to } 5.5 \text{ V}$ all other pins not under test = 0 V	-10	+10	μA	
Output leakage current	I _{O(L)}	I/O1-I/O8 are disabled (Hi-Z) $V_o = 0 \text{ to } 5.5 \text{ V}$	-10	+10	μA	
High level output voltage	V _{OH}	$I_o = -5.0 \text{ mA}$	2.4		V	
Low level output voltage	V _{OL}	$I_o = +4.2 \text{ mA}$		0.4	V	

[MC-421000A9 series]

Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ $I_O = 0 \text{ mA}$	$t_{RAC} = 60 \text{ ns}$	330	mA	3,4
			$t_{RAC} = 70 \text{ ns}$	280		
			$t_{RAC} = 80 \text{ ns}$	250		
			$t_{RAC} = 100 \text{ ns}$	220		
Standby current	I_{CC2}	$V_{IH(MIN.)} \leq \overline{RAS}$, $\overline{CAS}$	$I_O = 0 \text{ mA}$	6	mA	
		$V_{CC} - 0.2 \text{ V} \leq \overline{RAS}$, $\overline{CAS}$	$I_O = 0 \text{ mA}$	3		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $V_{IH(MIN.)} \leq \overline{CAS}$ $t_{RC} = t_{RC(MIN.)}$ $I_O = 0 \text{ mA}$	$t_{RAC} = 60 \text{ ns}$	330	mA	3,4
			$t_{RAC} = 70 \text{ ns}$	280		
			$t_{RAC} = 80 \text{ ns}$	250		
			$t_{RAC} = 100 \text{ ns}$	220		
Operating current (Fast page mode)	I_{CC4}	$\overline{CAS}$ Cycling $\overline{RAS} \leq V_{IL(MAX.)}$ $t_{PC} = t_{PC(MIN.)}$ $I_O = 0 \text{ mA}$	$t_{RAC} = 60 \text{ ns}$	260	mA	3,4
			$t_{RAC} = 70 \text{ ns}$	230		
			$t_{RAC} = 80 \text{ ns}$	200		
			$t_{RAC} = 100 \text{ ns}$	170		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ $I_O = 0 \text{ mA}$	$t_{RAC} = 60 \text{ ns}$	330	mA	3,4
			$t_{RAC} = 70 \text{ ns}$	280		
			$t_{RAC} = 80 \text{ ns}$	250		
			$t_{RAC} = 100 \text{ ns}$	220		
Input leakage current	$I_{I(L)}$	$V_I = 0 \text{ to } 5.5 \text{ V}$ all other pins not under test = 0 V	-10	+10	μA	
Output leakage current	$I_{O(L)}$	I/O1-I/O8, D _{out9} are disabled (Hi-Z) $V_O = 0 \text{ to } 5.5 \text{ V}$	-10	+10	μA	
High level output voltage	V_{OH}	$I_O = -5.0 \text{ mA}$	2.4		V	
Low level output voltage	V_{OL}	$I_O = +4.2 \text{ mA}$		0.4	V	

AC Characteristics

(Recommended Operating Conditions unless otherwise noted) Notes 5, 6

[MC-421000A8 series]

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		t _{RAC} = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random Read or Write Cycle Time	t _{RC}	120		140		160		190		ns	7
Fast Page Mode Cycle Time (Read or Write)	t _{PC}	40		45		50		60		ns	7
Access Time from RAS	t _{RAC}		60		70		80		100	ns	8, 9
Access Time from CAS (Falling Edge)	t _{CAC}		15		20		20		25	ns	8, 9
Access Time from Column Address	t _{AA}		30		35		40		50	ns	8, 9
Access Time from CAS Precharge	t _{ACP}		35		40		45		55	ns	9
RAS to Column Address Delay Time	t _{RAD}	15	30	15	35	17	40	17	50	ns	8
CAS to Data Setup Time	t _{CLZ}	0		0		0		0		ns	9
Output Buffer Turn-off Delay Time (CAS)	t _{OFF}	0	15	0	15	0	20	0	25	ns	10
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	3	50	ns	
RAS Precharge Time	t _{RP}	50		60		70		80		ns	
RAS Pulse Width (Random Read, Write Cycle)	t _{RAS}	60	10 000	70	10 000	80	10 000	100	10 000	ns	
RAS Pulse Width (Fast Page Mode)	t _{RASP}	60	125 000	70	125 000	80	125 000	100	125 000	ns	
RAS Hold Time	t _{RSH}	20		20		20		25		ns	
CAS Pulse Width	t _{CAS}	15	10 000	20	10 000	20	10 000	25	10 000	ns	
CAS Hold Time	t _{CSH}	60		70		80		100		ns	
RAS to CAS Delay Time	t _{RCD}	20	40	20	50	25	60	25	75	ns	8
CAS to RAS Precharge Time	t _{CRP}	10		10		10		10		ns	11
CAS Precharge Time	t _{CPN}	10		10		10		10		ns	
CAS Precharge Time (Fast Page Mode)	t _{CP}	10		10		10		10		ns	
RAS Precharge CAS Hold Time	t _{RPC}	10		10		10		10		ns	
RAS Hold Time from CAS Precharge	t _{RHCP}	35		40		45		55		ns	
Row Address Setup Time	t _{ASR}	0		0		0		0		ns	
Row Address Hold Time	t _{RAH}	10		10		12		12		ns	
Column Address Setup Time	t _{ASC}	0		0		0		0		ns	
Column Address Hold Time	t _{CAH}	15		15		15		20		ns	
Column Address Lead Time Referenced to RAS	t _{RAL}	30		35		40		50		ns	
Read Command Setup Time	t _{RCS}	0		0		0		0		ns	
Read Command Hold Time Referenced to RAS	t _{RRH}	10		10		10		10		ns	12
Read Command Hold Time Referenced to CAS	t _{RCH}	0		0		0		0		ns	12
Write Command Hold Time Referenced to CAS	t _{WCH}	15		15		15		20		ns	13
Data-in Setup Time	t _{DS}	0		0		0		0		ns	14
Data-in Hold Time	t _{DH}	15		15		15		20		ns	14
WE Command Setup Time	t _{WCS}	0		0		0		0		ns	15
CAS Setup Time for CAS before RAS Refresh	t _{CSR}	10		10		10		10		ns	
CAS Hold Time for CAS before RAS Refresh	t _{CHR}	15		15		15		20		ns	
WE Setup Time	t _{WBR}	10		10		10		10		ns	
WE Hold Time	t _{WHR}	15		15		15		20		ns	
Refresh Time	t _{REF}		16		16		16		16	ms	

[MC-421000A9 series]

(1/2)

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		t _{RAC} = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random Read or Write Cycle Time	t _{RC}	120		140		160		190		ns	7
Read Write Cycle Time	t _{RWC}	145		155		190		225		ns	7
Fast Page Mode Cycle Time (Read or Write)	t _{PC}	40		45		50		60		ns	7
Read Modify Write Cycle Time (Fast Page Mode)	t _{PRWC}	65		70		75		90		ns	7
Access Time from $\overline{\text{RAS}}$	t _{RAC}		60		70		80		100	ns	8, 9
Access Time from $\overline{\text{CAS}}$ (Falling Edge)	t _{CAC}		20		20		20		25	ns	8, 9
Access Time from Column Address	t _{AA}		30		35		45		50	ns	8, 9
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}		35		40		45		55	ns	9
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	15	30	15	35	17	40	17	50	ns	8
$\overline{\text{CAS}}$ to Data Setup Time	t _{CLZ}	0		0		0		0		ns	9
Output Buffer Turn-off Delay Time ($\overline{\text{CAS}}$)	t _{OFF}	0	15	0	15	0	20	0	25	ns	10
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	50		60		70		80		ns	
$\overline{\text{RAS}}$ Pulse Width (Random Read, Write Cycle)	t _{RAS}	60	10 000	70	10 000	80	10 000	100	10 000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t _{RASP}	60	125 000	70	125 000	80	125 000	100	125 000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSR}	20		20		20		25		ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	20	10 000	20	10 000	20	10 000	25	10 000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSR}	60		70		80		100		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	20	40	20	50	25	60	25	75	ns	8
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	10		10		10		10		ns	11
$\overline{\text{CAS}}$ Precharge Time	t _{CPN}	10		10		10		10		ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	t _{CP}	10		10		10		10		ns	
$\overline{\text{RAS}}$ Precharge $\overline{\text{CAS}}$ Hold Time	t _{RPC}	10		10		10		10		ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	35		40		45		55		ns	
Row Address Setup Time	t _{ASR}	0		0		0		0		ns	
Row Address Hold Time	t _{RAH}	10		10		12		12		ns	
Column Address Setup Time	t _{ASC}	0		0		0		0		ns	
Column Address Hold Time	t _{CAH}	15		17		20		20		ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	t _{RAL}	30		35		45		50		ns	
Read Command Setup Time	t _{RCS}	0		0		0		0		ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{RRH}	10		10		10		10		ns	12
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		0		0		ns	12
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	15		15		15		20		ns	13
Write Command Pulse Width	t _{WP}	15		15		15		20		ns	13
Data-in Setup Time	t _{DS}	0		0		0		0		ns	14
Data-in Hold Time	t _{DH}	15		15		20		20		ns	14
$\overline{\text{WE}}$ Command Setup Time	t _{WCS}	0		0		0		0		ns	15
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{CWD}	20		20		20		25		ns	15
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{RWD}	60		70		80		100		ns	15

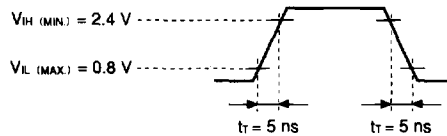
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Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		t _{RAC} = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
CAS Precharge Delay Time Referenced to $\overline{WE}$ (Fast Page Mode)	t _{CPWD}	55		60		70		85		ns	15
Column Address Delay Time Referenced to $\overline{WE}$	t _{AWD}	30		35		45		50		ns	15
Write Command Lead Time Referenced to $\overline{RAS}$	t _{RWL}	20		20		25		30		ns	
Write Command Lead Time Referenced to CAS	t _{CWL}	15		15		15		20		ns	
CAS Setup Time for CAS before $\overline{RAS}$ Refresh	t _{CSR}	10		10		10		10		ns	
CAS Hold Time for CAS before $\overline{RAS}$ Refresh	t _{CHR}	15		15		15		20		ns	
$\overline{WE}$ Setup Time	t _{WSR}	10		10		10		10		ns	
$\overline{WE}$ Hold Time	t _{WHR}	15		15		15		20		ns	
Refresh Time	t _{REF}		16		16		16		16	ms	

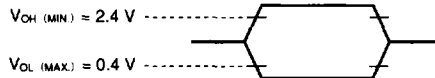
Notes

1. All voltages are referenced to GND.
2. After power-up, wait more than 100 μ s and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles to initialize the internal circuit.
3. Icc1 , Icc3 , Icc4 and Icc5 depend on trc and tpc . Specified values are obtained with outputs open.
4. Address can be changed once or less while $\text{RAS} = \text{VIL}$ and $\text{CAS} = \text{VIH}$.
5. AC measurements assume $\text{tr} = 5$ ns.
6. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



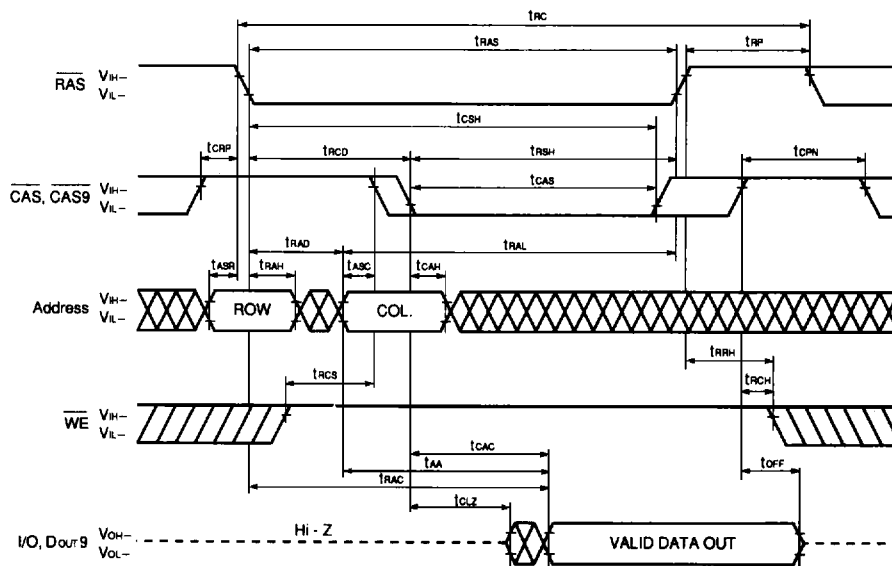
7. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($T_a = 0$ to 70°C) is assured.
8. In random read cycle, the access time is changed by the conditions of trAD and trCD as follows.

Condition	Access Time
$\text{trAD} \leq \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	trAC (MAX.)
$\text{trAD} > \text{trAD (MAX.)}$ and $\text{trCD} \leq \text{trCD (MAX.)}$	tAA (MAX.)
$\text{trCD} > \text{trCD (MAX.)}$	tCAC (MAX.)

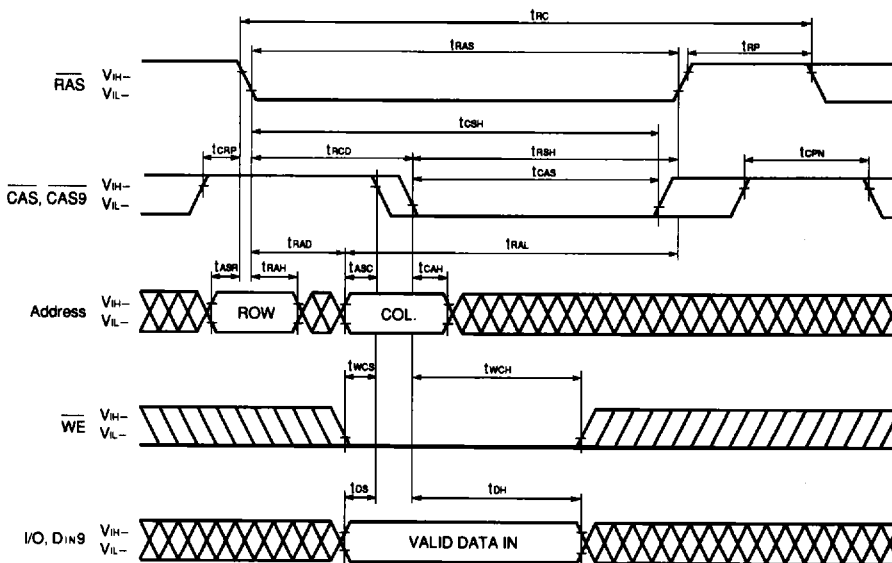
trAD (MAX.) and trCD (MAX.) indicate the points which the access time changes and are not the limits of operation.

9. Loading conditions are 2 TTL and 100 pF.
10. toff (MAX.) defines the time at which the output achieves the open-circuit condition and is not referenced to VOH or VOL .
11. tCRP (MIN.) requirement should be applicable for $\overline{\text{RAS}}$ / $\overline{\text{CAS}}$ cycles preceded by any cycles.
12. Either trCH (MIN.) or trRH (MIN.) must be satisfied for a read cycle.
13. tWP (MIN.) is applicable for late write cycle or read modify write cycle. In early write cycles, twCH (MIN.) should be satisfied.
14. tDS (MIN.) and tDH (MIN.) are referenced to $\overline{\text{CAS}}$ falling edge in early write cycles and to $\overline{\text{WE}}$ falling edge in late write or read modify write cycles.
15. If $\text{twCS} \geq \text{twCS (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $\text{trWD} \geq \text{trWD (MIN.)}$, $\text{tcWD} \geq \text{tcWD (MIN.)}$, $\text{tAWD} \geq \text{tAWD (MIN.)}$ and $\text{tcpWD} \geq \text{tcpWD (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above condition is met, the state of the data out is indeterminate.

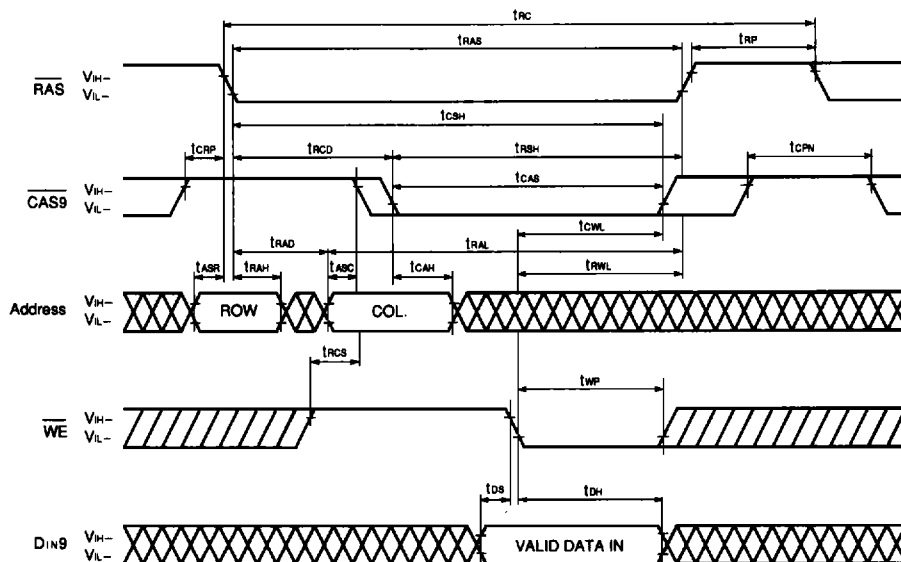
Read Cycle



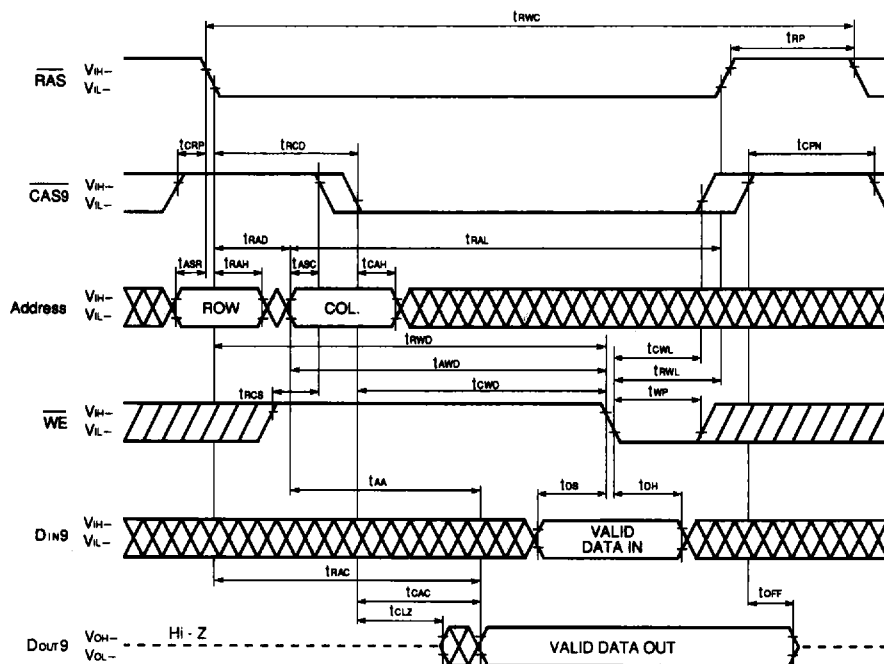
Early Write Cycle



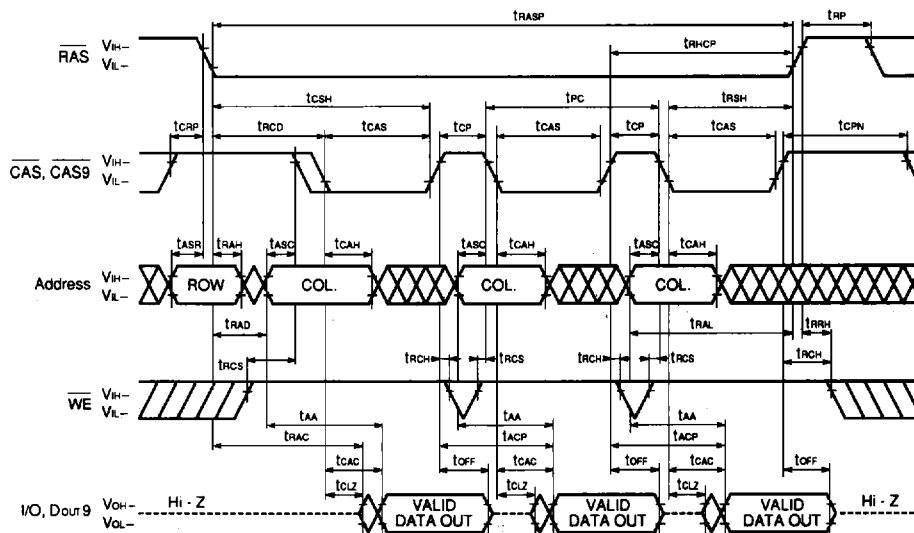
Late Write Cycle (Only for the MC-421000A9 series)



Read Modify Write Cycle (Only for the MC-421000A9 series)

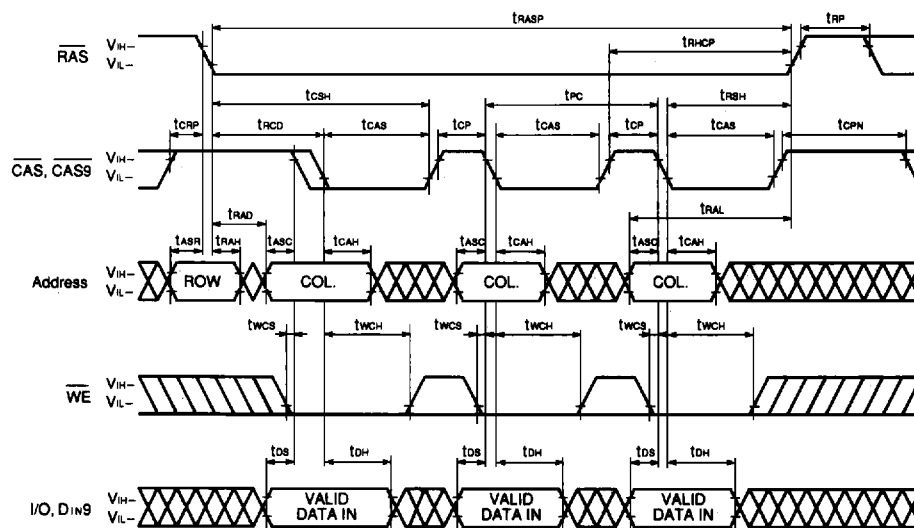


Fast Page Mode Read Cycle



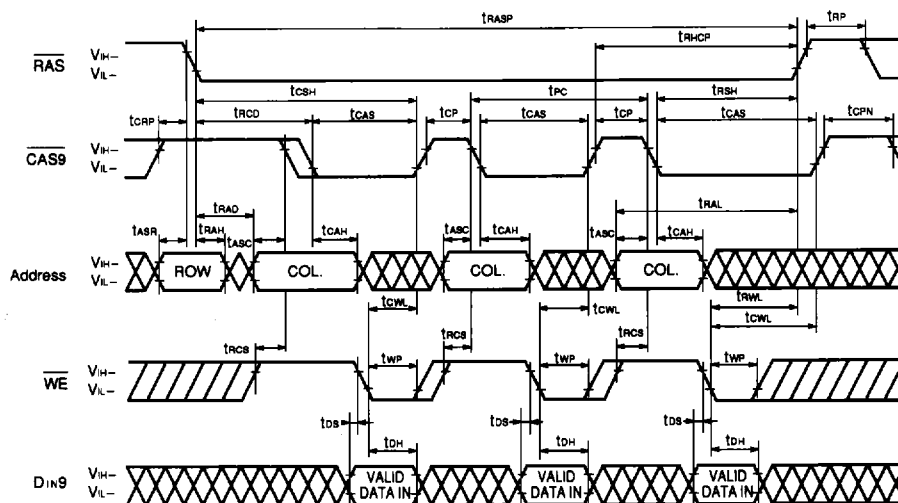
Remark In the fast page mode, read, write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Fast Page Mode Early Write Cycle



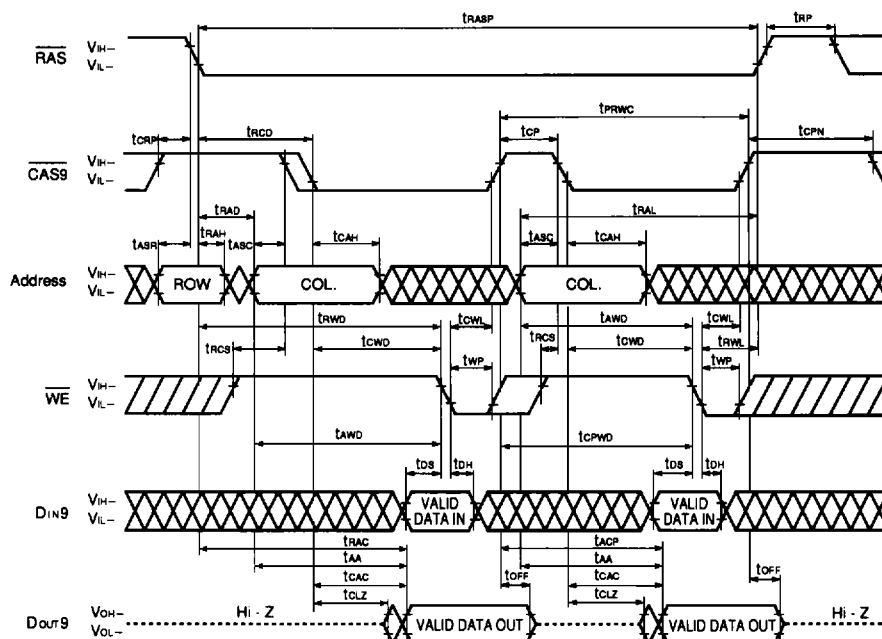
Remark In the fast page mode, read, write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Fast Page Mode Late Write Cycle (Only for the MC-421000A9 series)



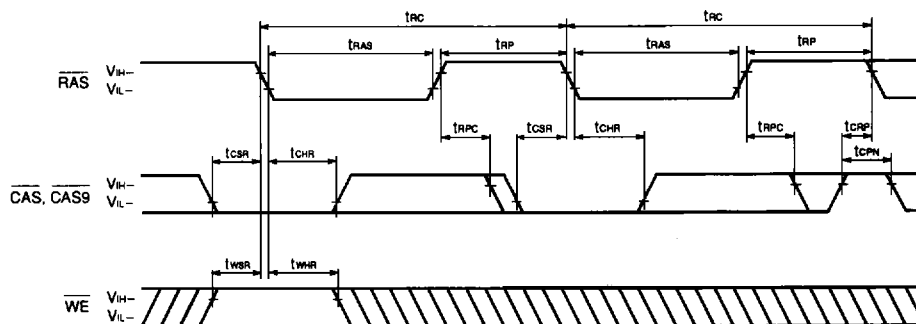
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

Fast Page Mode Read Modify Write Cycle (Only for the MC-421000A9 series)



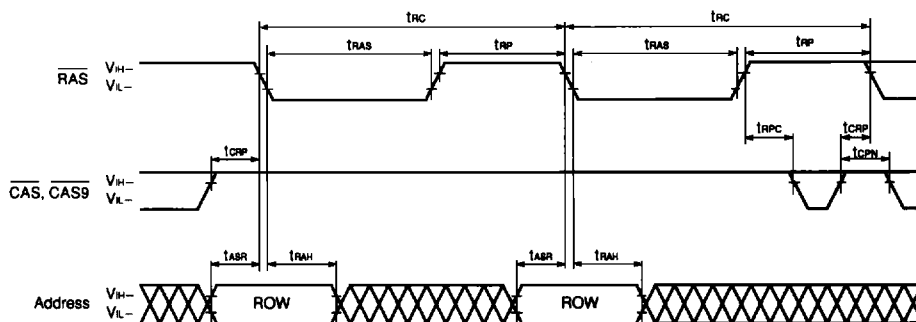
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

CAS Before RAS Refresh Cycle



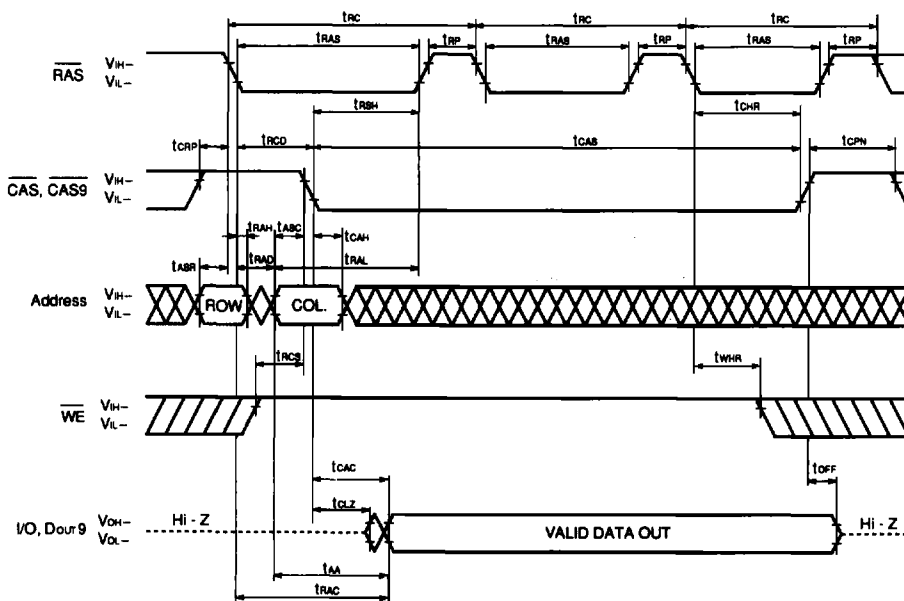
Remark Address, D_{in9} = Don't care I/O, D_{out9} = Hi-Z

RAS Only Refresh Cycle



Remark $\overline{\text{WE}}$, D_{in9} = Don't care I/O, D_{out9} = Hi-Z

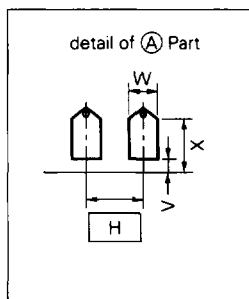
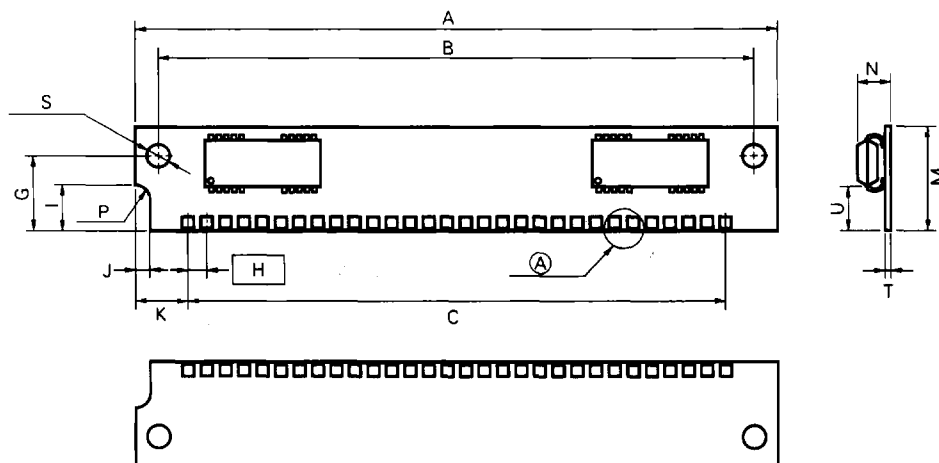
Hidden Refresh Cycle



Remark D1K9 = Don't care

MC-421000A8BA, 421000A8FA

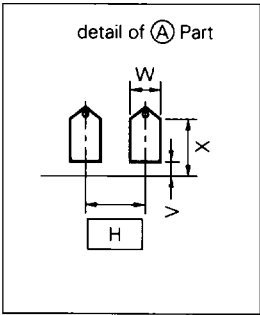
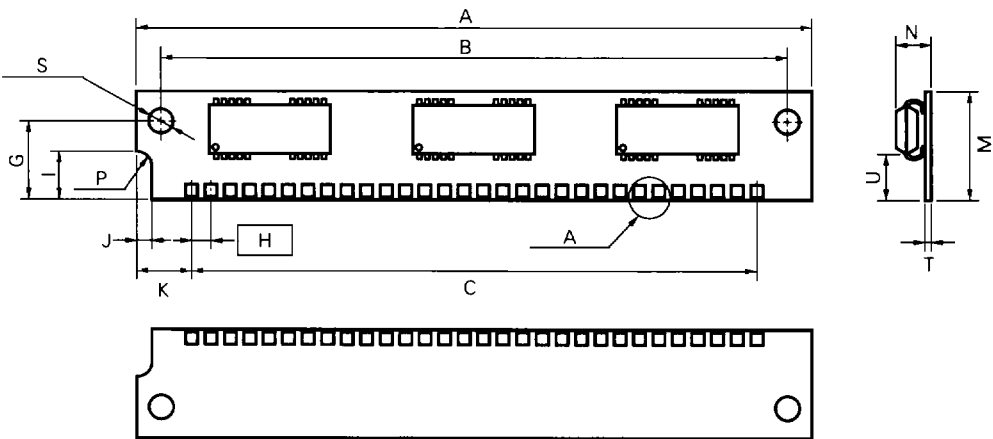
30 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)



M30B-100A4-2

ITEM	MILLIMETERS	INCHES
A	88.9±0.13	3.500±0.006
B	82.14	3.234
C	73.66	2.900
G	10.16	0.400
H	2.54 (T.P.)	0.100 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	7.62	0.300
M	16.51	0.65
N	5.08 MAX.	0.200 MAX.
P	R 2.0	R 0.079
S	Ø3.18	Ø0.125
T	1.27±0.08	0.050±0.004
U	4.86 MIN.	0.191 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.8±0.05	0.071 ^{+0.002} _{-0.003}
X	2.1 MIN.	0.082 MIN.

MC-421000A9BA, 421000A9FA
30 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)



M30B-100A5-2

ITEM	MILLIMETERS	INCHES
A	88.9±0.13	3.500±0.006
B	82.14	3.234
C	73.66	2.900
G	10.16	0.400
H	2.54 (T.P.)	0.100 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	7.62	0.300
M	16.51	0.65
N	5.08 MAX.	0.200 MAX.
P	R 2.0	R 0.079
S	φ3.18	φ0.125
T	1.27±0.08	0.050±0.004
U	4.86 MIN.	0.191 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.8±0.05	0.071 ^{+0.002} _{-0.003}
X	2.1 MIN.	0.082 MIN.