

Triple Bidirectional Latched Bus Transceiver

FAST Products

FEATURES

- Latching Transceiver
- High drive open collector output current with minimum output swing
- Compatible with Test Mode (TM) Bus specification
- Controlled output ramp
- Multiple package options

DESCRIPTION

The 74F777 is a triple bidirectional latched Bus transceiver and is intended to provide the electrical interface to a high performance wired-OR bus. This bus has a loaded characteristics impedance range of 20 to 50 ohms and is terminated on each end with a 30 to 40 ohm resistor.

The 74F777 is a triple bidirectional transceiver with open collector B and 3-state A port output drivers. A latch function is provided for the A port signals. The B port output driver is designed to sink 100 mA from 2 volts to minimize crosstalk and ringing on the bus.

A separate output threshold clamp voltage (V_X) is provided to prevent the A port output High level from exceeding future high density processor supply voltage levels. For 5 volt systems, V_X is simply tied to V_{CC} .

Triple Bidirectional Latched Bus Transceiver (3-State + Open Collector)

Objective Specification

TYPE	TYPICAL PROPAGATION DELAY	MAX SUPPLY CURRENT (TOTAL)
74F777	ns	mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0^\circ C$ to $+70^\circ C$
20-Pin Ceramic DIP (300mil) ¹	N74F777F
20-Pin PLCC ¹	N74F777A

NOTE:

1. Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

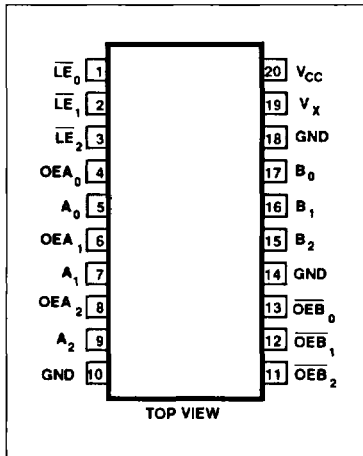
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_2$	PNP latched inputs	3.5/0.117	70 μ A/70 μ A
$B_0 - B_2$	Data inputs with threshold circuitry	5.0/0.167	100 μ A/100 μ A
$OEA_0 - OEA_2$	A Output Enable inputs (active High)	1.0/0.033	20 μ A/20 μ A
$OEB_0 - OEB_2$	B Output Enable inputs (active Low)	1.0/0.033	20 μ A/20 μ A
$LE_0 - LE_2$	Latch Enable inputs (active Low)	1.0/0.033	20 μ A/20 μ A
$A_0 - A_2$	3-State outputs	150/40	3mA/24mA
$B_0 - B_2$	Open Collector outputs	OC*/166.7	OC*/100mA

NOTES:

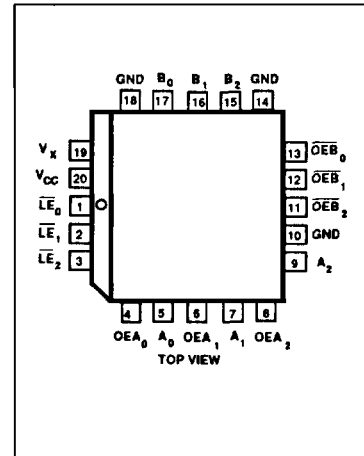
One (1.0) FAST Unit Load is defined as: 20 μ A in the High state and 0.6mA in the Low state.

* OC = Open Collector

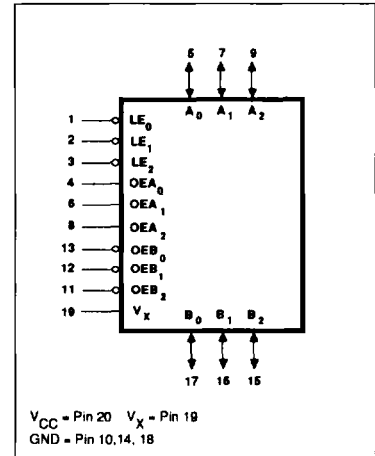
PIN CONFIGURATION



PIN CONFIGURATION PLCC



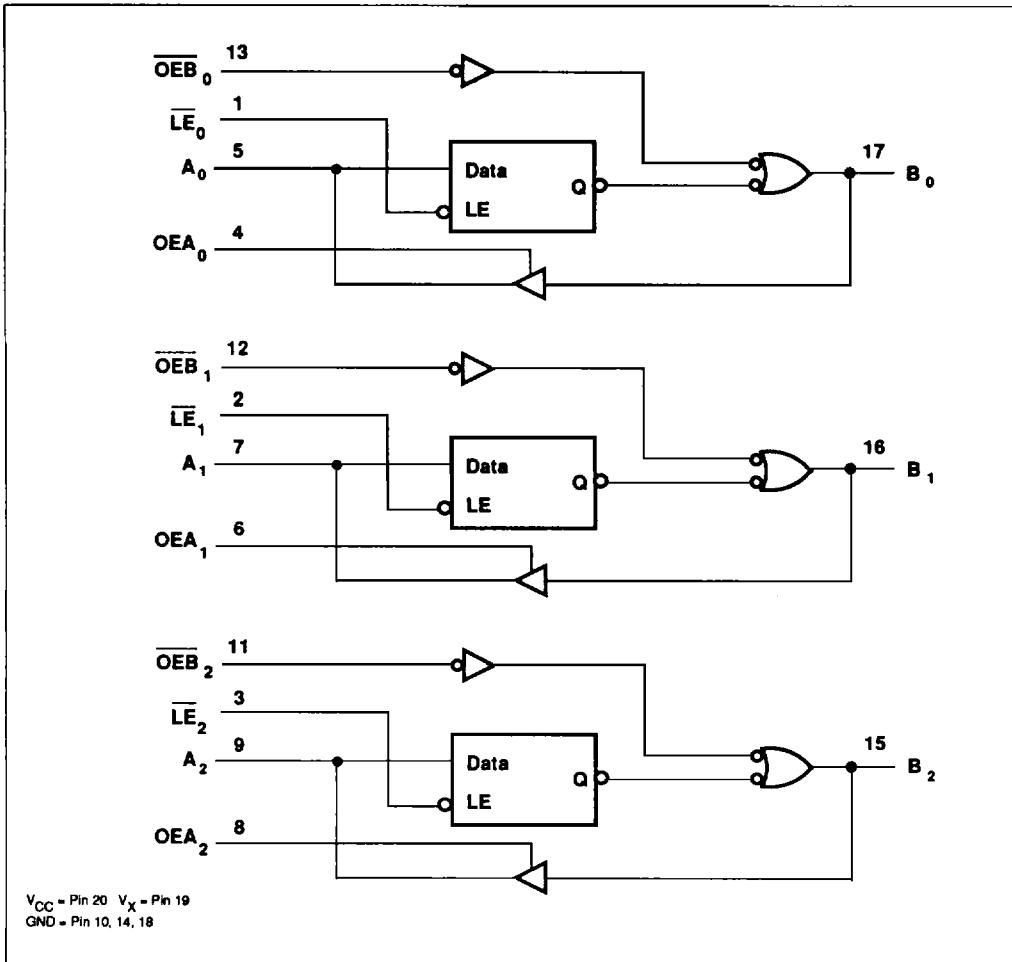
LOGIC SYMBOL



TM-Bus Transceiver

FAST 74F777

LOGIC DIAGRAM



TM-Bus Transceiver

FAST 74F777

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_X	Threshold control	-0.5 to +7.0	V
V_{IN}	Input voltage	$\overline{OE}B_n, OEAn, \overline{LE}_n$	-0.5 to +7.0
		$A_0 - A_2, B_0 - B_2$	-0.5 to 5.5
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to + V_{CC}	V
I_{OUT}	Current applied to output in Low output state	$A_0 - A_2$	48
		$B_0 - B_2$	200
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	Except $B_0 - B_2$	2.0		V
		$B_0 - B_2$	1.6		
V_{IL}	Low-level input voltage	Except $B_0 - B_2$		0.8	V
		$B_0 - B_2$		1.45	
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current	$A_0 - A_2$		-3	mA
I_{OL}	Low-level output current	$A_0 - A_2$		24	mA
		$B_0 - B_2$		100	
V_{OH}	High-level output voltage	$B_0 - B_2$	2.0	4.0	V
T_A	Operating free-air temperature range	0		70	°C

TM-Bus Transceiver

FAST 74F777

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹	LIMITS			UNIT	
			Min	Typ ²	Max		
I_{OH}	High level output current	$B_0 - B_2$ $V_{CC} = \text{MAX}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}, V_{OH} = 2.1\text{V}$			100	μA	
I_{OFF}	Power-off output current	$B_0 - B_2$ $V_{CC} = 0.0\text{V}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}, V_{OH} = 2.1\text{V}$			100	μA	
V_{OH}	High-level output voltage	$A_0 - A_2$ $V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}$	$I_{OH} = -3\text{mA}, V_X = V_{CC}$	2.5	V_{CC}	V	
			$I_{OH} = -0.4\text{mA}, V_X = 3.13\text{V} \& 3.47\text{V}$	2.5	V_X	V	
V_{OL}	Low-level output voltage	$A_0 - A_2$ $V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}$	$I_{OL} = 20\text{mA}, V_X = V_{CC}$		0.5	V	
			$B_0 - B_2$ $V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}$	$I_{OL} = 100\text{mA}$ $I_{OL} = 4\text{mA}$	0.40	1.15	V
V_{IK}	Input clamp voltage	$A_0 - A_2$	$V_{CC} = \text{MIN}, I_1 = I_{IK}$		-0.5	V	
		Except $A_0 - A_2$	$V_{CC} = \text{MIN}, I_1 = I_{IK}$		-1.2	V	
I_I	Input current at maximum input voltage	$\overline{OEB}_n, \overline{OEA}_n, \overline{LE}_n$	$V_{CC} = 0.0\text{V}, V_I = 7.0\text{V}$		100	μA	
		$A_0 - A_2, B_0 - B_2$	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$		1	mA	
I_{IH}	High-level input current	$\overline{OEB}_n, \overline{OEA}_n, \overline{LE}_n$	$V_{CC} = \text{MAX}, V_I = 2.7\text{V}, B_n - A_n = 0\text{V}$		20	μA	
		$B_0 - B_2$	$V_{CC} = \text{MAX}, V_I = 2.1\text{V}$		100	μA	
I_{IL}	Low-level input current	$\overline{OEB}_n, \overline{OEA}_n, \overline{LE}_n$	$V_{CC} = \text{MAX}, V_I = 0.5\text{V}$		-20	μA	
		$B_0 - B_2$	$V_{CC} = \text{MAX}, V_I = 0.3\text{V}$		-100	μA	
$I_{OZH} + I_{IH}$	Off-state output current, High-level voltage applied	$A_0 - A_2$	$V_{CC} = \text{MAX}, V_O = 2.7\text{V}$		70	μA	
$I_{OZL} + I_{IL}$	Off-state output current, Low-level voltage applied	$A_0 - A_2$	$V_{CC} = \text{MAX}, V_O = 0.5\text{V}$		-70	μA	
I_X	High-level control current		$V_{CC} = \text{MAX}, V_X = V_{CC}, \overline{LE} = \overline{OEA}_n = \overline{OEB}_n = 2.7\text{V}, A_0 - A_2 = 2.7\text{V}, B_0 - B_2 = 2.0\text{V}$	-100	100	μA	
			$V_{CC} = \text{MAX}, V_X = 3.13\text{V} \& 3.47\text{V}, \overline{LE} = \overline{OEA}_n = 2.7\text{V}, \overline{OEB}_n = A_0 - A_7 = 2.7\text{V}, B_0 - B_2 = 2.0\text{V}$	-10	10	mA	
I_{OS}	Short-circuit output current ³	$A_0 - A_2$ only	$V_{CC} = \text{MAX}, B_n = 1.6\text{V}, \overline{OEA}_n = 2.0\text{V}, \overline{OEB}_n = 2.7\text{V}$	-60	-150	mA	
I_{CC}	Supply current (total)	I_{CCH}	$V_{CC} = \text{MAX}$		70	100	mA
		I_{CCL}	$V_{CC} = \text{MAX}, V_{IL} = 0.5\text{V}$		100	145	mA
		I_{CCZ}	$V_{CC} = \text{MAX}, V_{IL} = 0.5\text{V}$		80	100	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type. Unless otherwise specified, $V_X = V_{CC}$ for all test conditions.
- All typical values are at $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
- Due to test equipment limitations, actual test conditions are for $V_{IH} = 1.6\text{V}$ and $V_{IL} = 1.3\text{V}$.

TM-Bus Transceiver

FAST 74F777

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			$T_A = +25^\circ\text{C}$ $V_{CC} = 5\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay B to A	Waveform 1, 2	5.5 6.0	8.5 8.5	12.0 11.5	4.5 6.0	13.5 12.0	ns
t_{PZH} t_{PZL}	Output Enable time from High or Low OEA _n to A	Waveform 4.5	8.0 8.5	10.5 12.5	13.5 16.0	7.0 8.5	16.5 19.5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low OEA _n to A	Waveform 4.5	2.0 2.0	3.0 3.0	8.0 8.0	2.0 2.0	8.5 8.5	ns
t_{TLH} t_{THL}	Transition time, B Port 0.8V to 1.8 V, 1.8V to 0.8V	Test Circuit and Waveform	0.5 0.5	2.5 2.0	5.0 5.0	0.5 0.5	6.0 6.0	ns
SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS					UNIT
			$T_A = +25^\circ\text{C}$ $V_{CC} = 5\text{V}$ $C_D = 30\text{pF}$ $R_U = 9\Omega$			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_D = 30\text{pF}$ $R_U = 9\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A to B	Waveform 1, 2	1.5 3.5	4.0 6.0	7.0 9.0	1.0 2.5	9.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay LE _n to B	Waveform 1, 2	3.0 4.0	5.0 6.0	8.0 9.0	2.0 3.0	10.0 10.0	ns
t_{PLH} t_{PHL}	Enable/disable time OEB _n to B	Waveform 1, 2	2.5 3.0	4.5 7.5	7.5 10.5	1.5 3.0	8.5 11.0	ns
t_{TLH} t_{THL}	Transition time, B Port 1.3V to 1.7 V, 1.7V to 1.3V	Test Circuit and Waveform	0.5 0.5	2.0 2.0	4.5 4.5	0.5 0.5	4.5 4.5	ns

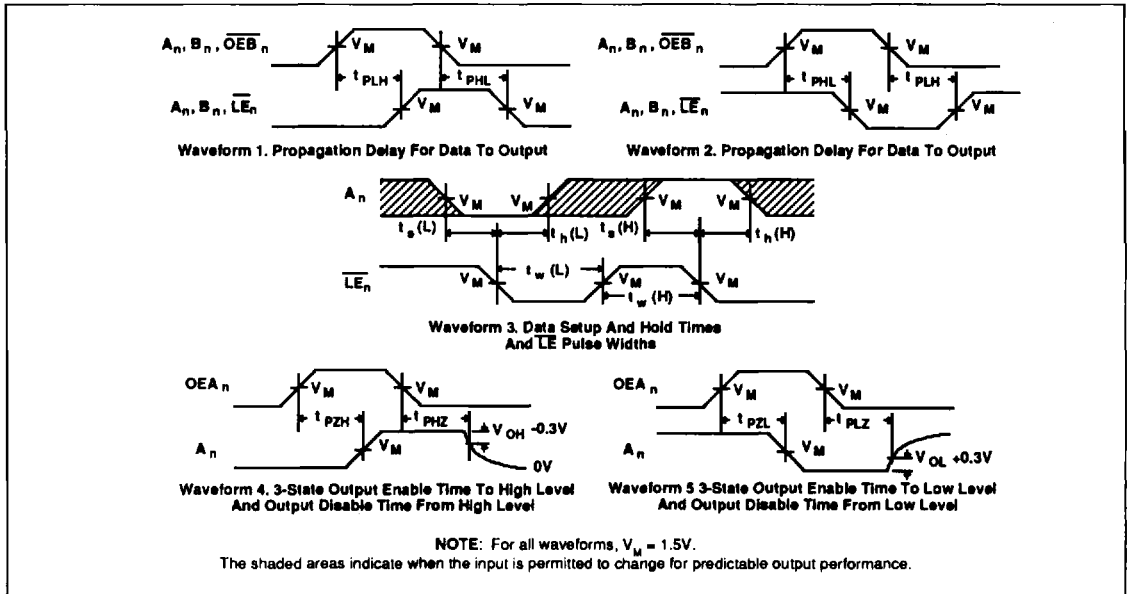
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25^\circ\text{C}$ $V_{CC} = 5\text{V}$ $C_L = 30\text{pF}$ $R_U = 9\Omega$			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 30\text{pF}$ $R_U = 9\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time A to LE	Waveform 3	5.0 5.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time A to LE	Waveform 3	0.0 0.0			0.0 0.0		ns
$t_w(H)$ $t_w(L)$	LE Pulse width, High or Low	Waveform 3	15.0 15.0			15.0 15.0		ns

TM-Bus Transceiver

FAST 74F777

AC WAVEFORMS



TEST CIRCUIT AND WAVEFORMS

