Si32266/7/8/9

SINGLE-CHIP DUAL PROSLIC® WITH INTEGRATED SERIAL INTERFACE (ISI)

Features

- Two complete FXS channels in 6 x 8 mm
- 3-wire ISI combines PCM, SPI, and interrupt
- Performs all BORSCHT functions
- Ideal for short- or long-loop applications
- Ultra low power consumption
- Internal balanced or unbalanced ringing
- Patented low power ringing
- Adaptive ringing
- Simplified configuration and diagnostics
  - Supported by ProSLIC API
  - GR-909 loop diagnostics
  - Audio diagnostics with loopback
  - Integrated test load
- Wideband voice support
- On-hook transmission
- Loop or ground start operation
- Smooth polarity reversal
- Pulse metering
- Software-programmable parameters:
  - Ringing frequency, amplitude, cadence, and waveshape
  - Two-wire ac impedance
  - Transhybrid balance
  - DC current loop feed (10–45 mA)
  - Loop closure and ring trip thresholds
  - Ground key detect threshold
- Integrated dc-dc controllers with direct connection to MOSFET
- Two high voltage supply options
  - Full tracking (Si32266/7)
  - Tracking shared supplies (Si32268/9)
- DTMF generator/decoder
- A-Law/µ-Law companding, linear PCM
- 3.3 V operation
- Pb-free/RoHS-compliant packaging

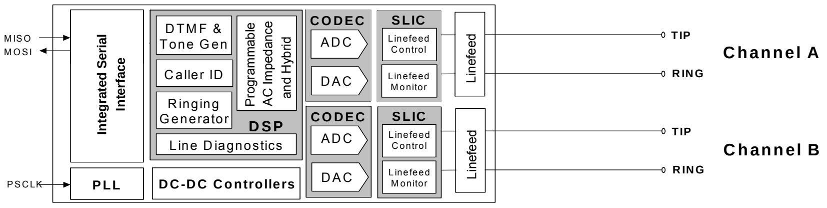
Applications

- VoIP gateways and routers
- xDSL IADs
- Optical Network Terminals/Units (ONT/U)
- Analog Terminal Adapters (ATA)
- Cable eMTA
- Wireless Fixed Terminals (WFT)
- Wireless Local Loop (WLL)
- WiMAX CPE

Description

The Si32266/7/8/9 Dual ProSLIC® devices, in a single package, implement two complete foreign exchange station (FXS) telephony interfaces. The Si32266/7/8/9 devices operate from a 3.3 V supply and use Silicon Labs' proprietary three-wire digital Integrated Serial Interface (ISI). Built-in dc-dc converter controllers can be used to automatically generate the optimal battery voltage required for each line-state, optimizing efficiency and minimizing heat generation. The Si32266/7 devices are designed to operate with a tracking battery supply for each channel for lowest power consumption. The Si32268/9 devices use shared battery supplies for lowest cost, with an internal dc-dc controller that operates in Tracking Shared Supply (TSS) mode to deliver power consumption lower than typical fixed voltage shared rail designs. Self-testing and metallic loop testing (MLT) (e.g., GR-909) is facilitated by the built-in DSP, monitor ADC, and test load. The devices are available with linefeed voltage ratings of –110 V (Si32266/8) or –140 V (Si32267/9) to support high voltage ringing, and both devices support wideband audio for better-than-PSTN voice quality. All Si32266/7/8/9 devices are available in a 6 x 8 mm 50-pin QFN package.

Functional Block Diagram



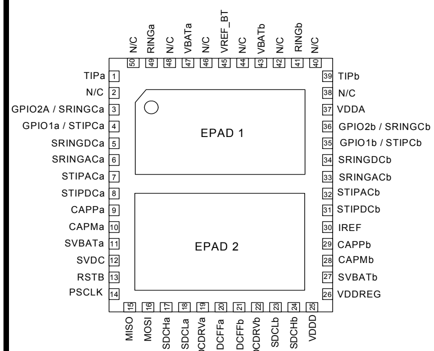
Si32266/7/8/9

Ordering Information

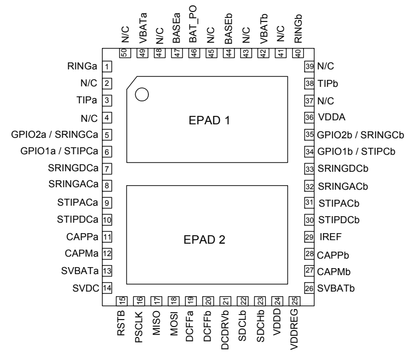
See page 42.

Pin Assignments

Si32266/7



Si32268/9



Patents pending

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1. Electrical Specifications

Table 1. Recommended Operating Conditions[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A	F-grade	0	25	70	°C
		G-grade	–40	25	85	°C
Silicon Junction Temperature, QFN-50	T_{JHV}	Linefeed Die	—	—	145[2]	°C
Supply Voltage, Si3226x	V_{DDD}, V_{DDA}		3.13	3.3	3.47	V
Battery Voltage, Si32266/8[3]	V_{BAT}		–110	—	–15	V
Battery Voltage, Si32267/9[3]	V_{BAT}		–140	—	–15	V

Notes:

1. All minimum and maximum specifications apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.
2. Except during ringing.
3. Operation at minimum voltage dependent upon loop conditions and dc-dc converter configuration.

Table 2. AC Characteristics

(V_{DD} = 3.13 to 3.47 V, T_A = 0 to 70 °C)

Parameter	Test Condition	Min	Typ	Max	Unit
TX/RX Performance					
Overload Compression	2-Wire – PCM	Figure 4	—	—	
Single Frequency Distortion (0 dBm0 input)	0 Hz to 4 kHz	—	—	–40	dBm0[5]
	0 Hz to 12 kHz	—	—	–28	dBm0[5]
Signal-to-(Noise + Distortion) Ratio[1]	200 Hz to 3.4 kHz D/A or A/D 8-bit Active off-hook, and OHT, any Z_T	Figure 3	—	—	
Audio Tone Generator Signal-to-Distortion Ratio[1]	0 dBm0, Active off-hook, and OHT, any Z_T	46	—	—	dB
Intermodulation Distortion		—	—	–41	dB
Gain Accuracy[1]	2-Wire to PCM or PCM to 2-Wire 1014 Hz, any gain setting	–0.2	—	0.2	dB
Attenuation Distortion vs. Frequency	0 dBm0[5]	See Figure 5 and 6			
Group Delay vs. Frequency		See Figure 7 and 8			

Notes:

1. Analog signal measured as $V_{TIP} – V_{RING}$. Assumes ideal line impedance matching.
2. The quantization errors inherent in the µ/A-law companding process can generate slightly worse gain tracking performance in the signal range of 3 to –37 dB for signal frequencies that are integer divisors of the 8 kHz PCM sampling rate.
3. V_{DDD}, V_{DDA} = 3.3 V, V_{BAT} = –52 V, no fuse resistors; R_L = 600 Ω, Z_S = 600 Ω synthesized using RS register coefficients.
4. The level of any unwanted tones within the bandwidth of 0 to 4 kHz does not exceed –55 dBm.
5. 0 dBm0 is equal to 0 dBm into 600 Ω.

Table 2. AC Characteristics (Continued)

(V_{DD} = 3.13 to 3.47 V, T_A = 0 to 70 °C)

Parameter	Test Condition	Min	Typ	Max	Unit
Gain Tracking[2]	1014 Hz sine wave, reference level –10 dBm Signal level:				
	3 dB to –37 dB	—	—	0.25	dB
	–37 dB to –50 dB	—	—	0.5	dB
	–50 dB to –60 dB	—	—	1.0	dB
Round-Trip Group Delay	1014 Hz, Within same time-slot	—	450	500	µs
2-Wire Return Loss[3]	200 Hz to 3.4 kHz	26	30	—	dB
Transhybrid Balance[3]	300 Hz to 3.4 kHz	26	30	—	dB
Noise Performance					
Idle Channel Noise[4]	C-Message weighted	—	8	12	dBrnC
	Psophometric weighted	—	–82	–78	dBmP
PSRR from V_{DDD}, V_{DDA} @ 3.3 V	RX and TX, 200 Hz to 3.4 kHz	—	55	—	dB
Longitudinal Performance					
Longitudinal to Metallic/PCM Balance (forward or reverse)	200 Hz to 1 kHz	58	60	—	dB
	1 kHz to 3.4 kHz	53	58	—	dB
Metallic/PCM to Longitudinal Balance	200 Hz to 3.4 kHz	40	—	—	dB
Longitudinal Impedance	200 Hz to 3.4 kHz at TIP or RING	—	50	—	Ω
Longitudinal Current Capability	Active off-hook 60 Hz Reg 73 = 0x0B	—	25	—	mA

Notes:

1. Analog signal measured as $V_{TIP} – V_{RING}$. Assumes ideal line impedance matching.
2. The quantization errors inherent in the µ/A-law companding process can generate slightly worse gain tracking performance in the signal range of 3 to –37 dB for signal frequencies that are integer divisors of the 8 kHz PCM sampling rate.
3. V_{DDD}, V_{DDA} = 3.3 V, V_{BAT} = –52 V, no fuse resistors; R_L = 600 Ω, Z_S = 600 Ω synthesized using RS register coefficients.
4. The level of any unwanted tones within the bandwidth of 0 to 4 kHz does not exceed –55 dBm.
5. 0 dBm0 is equal to 0 dBm into 600 Ω.

Table 3. Power Supply Characteristics

(V_{DD} = 3.3 V, T_A = 0 to 70 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply currents: Reset	I_{DD}	VT and VR = Hi-Z , RST = 0	—	3.5	—	mA
	I_{VBAT}		—	0	—	mA
Supply currents: High Impedance, Open	I_{DD}	VT and VR = Hi-Z	—	23	—	mA
	I_{VBAT}		—	0.6	—	mA
Supply currents: Forward/Reverse, On-hook	I_{DD}	VTR = –48 V, Automatic Power Save Mode enabled	—	10	—	mA
	I_{VBAT}		—	0.4	—	mA
Supply currents: Forward/Reverse, On-hook	I_{DD}	VTR = –48 V, Automatic Power Save Mode disabled	—	35	—	mA
	I_{VBAT}		—	2.2	—	mA
Supply currents: Tip/Ring Open, On-hook	I_{DD}	VT or VR = –48 V, VR or VT = Hi-Z, Automatic Power Save Mode enabled	—	10	—	mA
	I_{VBAT}		—	0.4	—	mA
Supply currents: Tip/Ring Open, On-hook	I_{DD}	VT or VR = –48 V, VR or VT = Hi-Z, Automatic Power Save Mode disabled	—	35	—	mA
	I_{VBAT}		—	1.5	—	mA
Supply currents: Forward/Reverse OHT, On-hook	I_{DD}	VTR =48 V	—	53	—	mA
	I_{VBAT}		—	3	—	mA
Supply currents: Forward/Reverse Active, Off-hook	I_{DD}	ILOOP = 26 mA RLOAD = 200 Ω	—	54	—	mA
	I_{VBAT}		—	2.2 + ILOOP	—	mA
Supply currents: Ringing	I_{DD}	VTR =55V_{RMS} + 0 VDC, balanced, FXO disabled sinusoidal, f = 20 Hz, RLOAD = 5 REN = 1400 Ω	—	40	—	mA
	I_{VBAT}		—	38	—	mA

Notes:

1. All specifications are for a single channel of Si3226x, and based on measurements with all channels in the same operating state.
2. I_{LOOP} is the dc current in the subscriber loop during the off-hook state.

Table 4. Linefeed Characteristics

(V_{DD} = 3.13 to 3.47 V, T_A = 0 to 70 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Maximum Loop Resistance	R_{LOOP}	$R_{DC,MAX}$ = 430 Ω I_{LOOP} = 18 mA, V_{BAT} = –52 V, R_{PROT} = 0 Ω	—	—	2000	Ω
DC Feed Current		Differential	—	—	45	mA
		Common Mode	—	—	30	mA
		Differential + Common Mode	—	—	45	mA
DC Loop Current Accuracy		I_{LIM} = 18 mA	—	—	10	%
DC Open Circuit Voltage Accuracy		Active Mode; V_{OC} = 48 V, $V_{TIP} – V_{RING}$	—	—	4	V
DC Differential Output Resistance	R_{DO}	$I_{LOOP} < I_{LIM}$	160	—	640	Ω
DC On-Hook Voltage Accuracy—Ground Start	V_{OHTO}	$I_{RING}<I_{LIM}$; V_{RING} wrt ground, V_{RING} = –51 V	—	—	4	V
DC Output Resistance—Ground Start	R_{ROTO}	$I_{RING}<I_{LIM}$; RING to ground	160	—	640	Ω
DC Output Resistance—Ground Start	R_{TOTO}	TIP to ground	400	—	—	kΩ
Loop Closure Detect Threshold Accuracy		I_{THR} = 13 mA	—	—	10	%
Ground Key Detect Threshold Accuracy		I_{THR} = 13 mA	—	—	10	%
Ring Trip Threshold Accuracy		AC detection, V_{RING} = 70 Vpk, no offset, I_{TH} = 80 mA	—	—	4	mA
		DC detection, 20 V dc offset, I_{TH} = 13 mA	—	—	1	mA
		DC Detection, 48 V DC offset, R_{loop} = 1500 Ω	—	—	3	mA
Ringing Amplitude*	$V_{RINGING}$	Si32266/8 Open circuit, V_{BAT} = –110 V	—	–108	—	V_{PK}
		Si32267/9 Open circuit, V_{BAT} = –140 V	—	–136	—	V_{PK}
Sinusoidal Ringing Total Harmonic Distortion	R_{THD}	Si32266/8: 60 V_{RMS}, 15 V_{OFFSET}, 0–5 REN	—	1	—	%
		Si32267/9: 55 V_{RMS}, 48 V_{OFFSET}, 0–5 REN				
Ringing Frequency Accuracy		f = 16 Hz to 60 Hz	—	—	1	%
Ringing Cadence Accuracy		Accuracy of ON/OFF times	—	—	50	ms

***Note:** Ringing amplitude is set for 108 or 128 V peak and measured at TIP-RING using no series protection resistance.

Table 4. Linefeed Characteristics (Continued)

(V_{DD} = 3.13 to 3.47 V, T_A = 0 to 70 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Loop Voltage Sense Accuracy		$V_{TIP} – V_{RING}$ = 48 V	—	2	4	%
Loop Current Sense Accuracy		I_{LOOP} = 18 mA	—	7	10	%
Power Alarm Threshold Accuracy		Power Threshold = 1.0 W V_{BAT} = –56 V, I_{LDDD} = 40 mA, R_{LOAD} = 600 Ω	—	15	—	%
Test Load Impedance	R_{TEST}	HVIC_STATE_SPARE[23] = 1; $\lvert V_{T/R} \rvert \leq 50$ V	—	2.2	—	kΩ
Test Load Voltage	V_{TL}	HVIC_STATE_SPARE[23] = 1	±5		±50	V
***Note:** Ringing amplitude is set for 108 or 128 V peak and measured at TIP-RING using no series protection resistance.						

Table 5. Digital I/O Characteristics

(V_{DD} = 3.13 to 3.47 V, T_A = 0 to 70 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	V_{DD}	V
Low Level Input Voltage	V_{IL}		0	—	0.8	V
High Level Output Voltage	V_{OH}	MOSI, GPIO1/STIPC, GPIO2/ SRINGC: I_O = –4 mA	V_{DD} – 0.6	—	—	V
Low Level Output Voltage	V_{OL}	MOSI, GPIO1/STIPC, GPIO2/ SRINGC: I_O = 4 mA	—	—	0.4	V
$\overline{\text{RST}}$ Internal Pullup Current			33	42	80	µA
Input Leakage Current	I_L		—	—	10	µA

Table 6. Charge Pump Characteristics

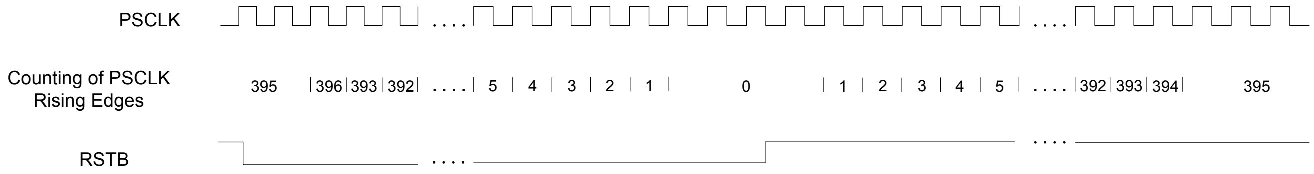
(V_{DD} = 3.13 to 3.47 V, T_A = 0 to 70 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage (DCDRVa/b, DCFFa/b)	V_{CP}		2 x V_{DD} – 1	—	2xV_{DD}	V
Output Current	I_{CP}		—	—	3*	mA
***Note:** Peak drive current capability is >60 mA.						

Table 7. Switching Characteristics—General Inputs*

(V_{DD} = 3.13 to 3.47 V, T_A = 0 to 70 °C, C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
Rise Time, $\overline{RST}$	t_r	—	—	5	ns
$\overline{RST}$ Pulse Width	t_{rl}	396/ PSCLK	—	—	µs
***Note:** All timing (except Rise and Fall time) is referenced to the 50% level of the waveform. Input test levels are V_{IH} = V_{DD} – 0.4 V, V_{IL} = 0.4 V. Rise and Fall times are referenced to the 20% and 80% levels of the waveform.					



Note: The count of PCLK rising edges during reset will be skewed by 1-2 clocks based on the internal sampling of reset.

Figure 1. Reset Timing Diagram

Table 8. Switching Characteristics—ISI

(V_{DDA} = 3.13 to 3.47 V, T_A = 0 to 70 °C, C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
Setup Time, MOSI to PSCLK Fall	t_{su}	7.5	—	—	ns
Hold Time, MOSI to PSCLK Fall	t_h	5	—	—	ns
Delay Time, PSCLK Rise to MISO	t_d	—	—	16	ns
PSCLK Period	t_p	—	40.69	—	ns
PSCLK Duty Cycle		40	50	60	%

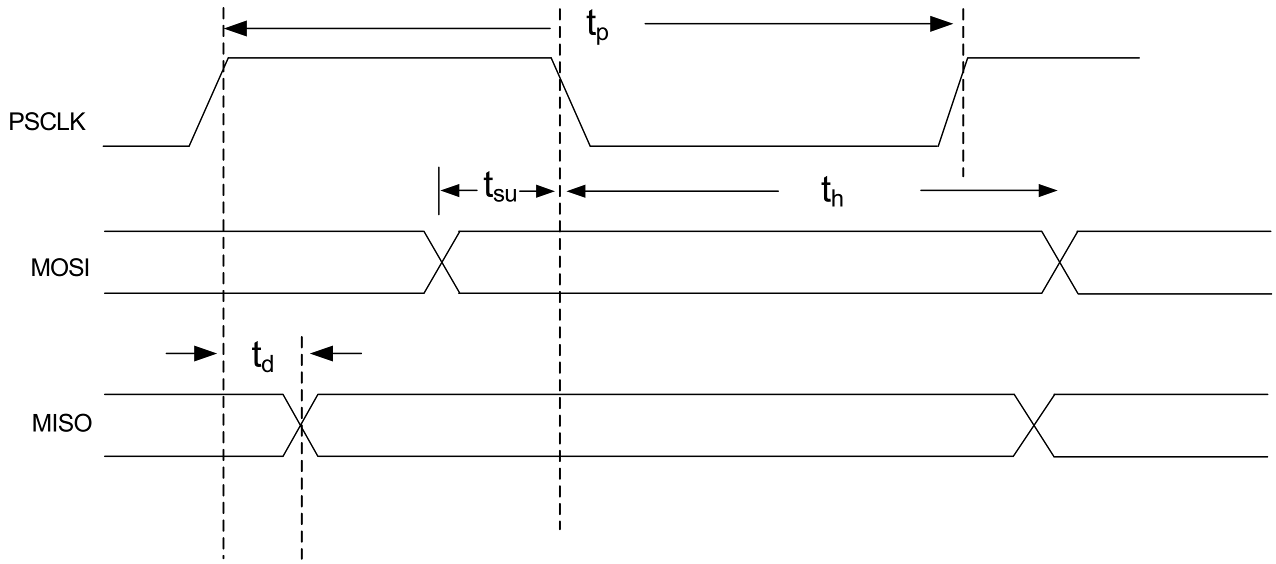


Figure 2. ISI Timing Diagram

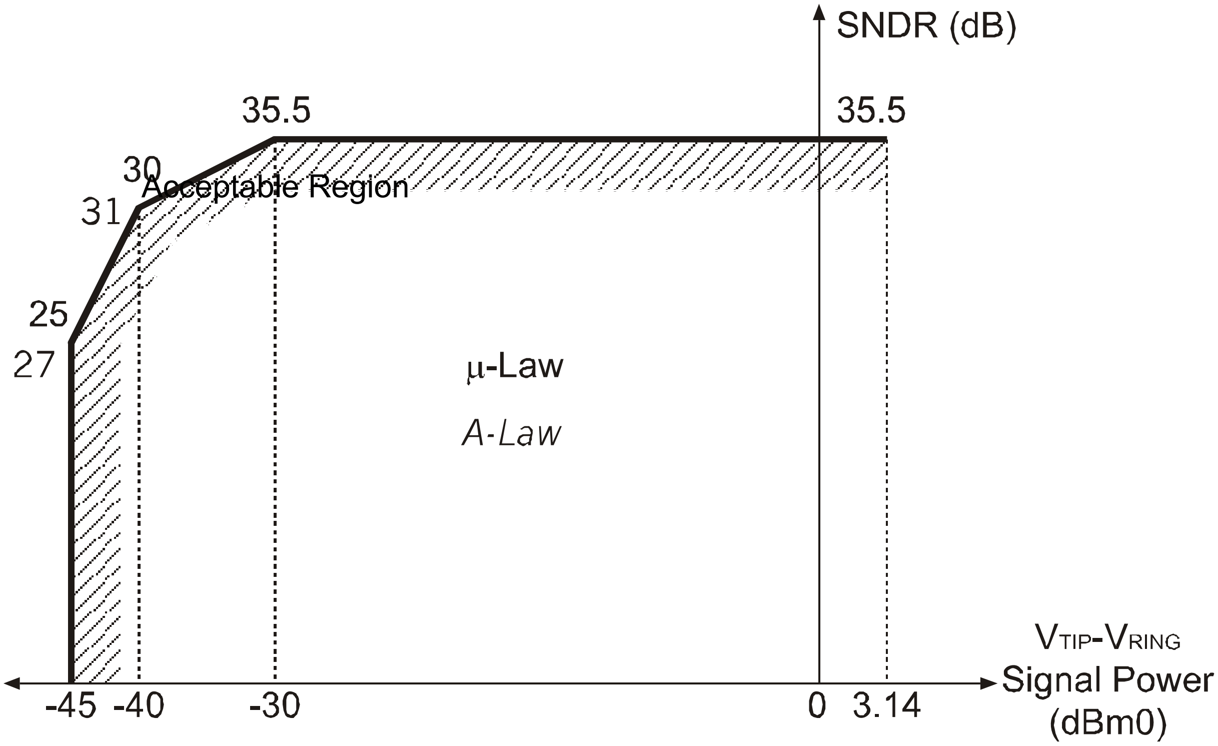


Figure 3. Transmit and Receive Path SNDR

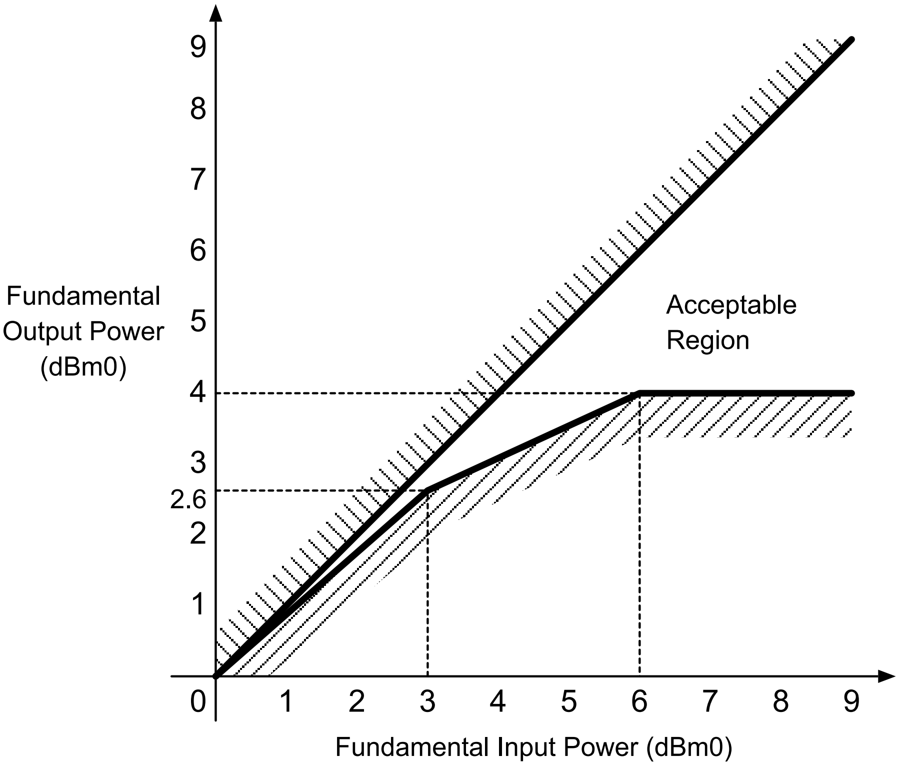


Figure 4. Overload Compression Performance

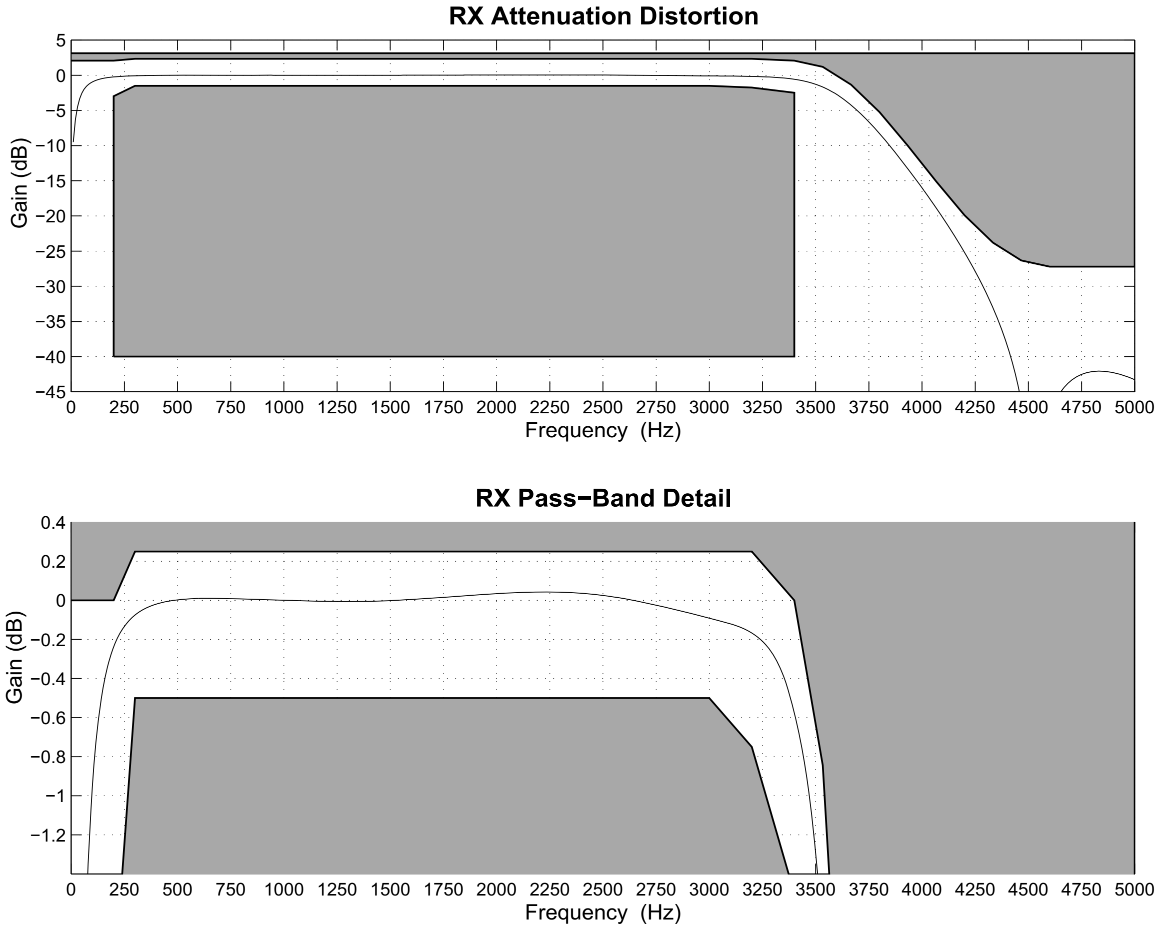


Figure 5. Receive Path Frequency Response

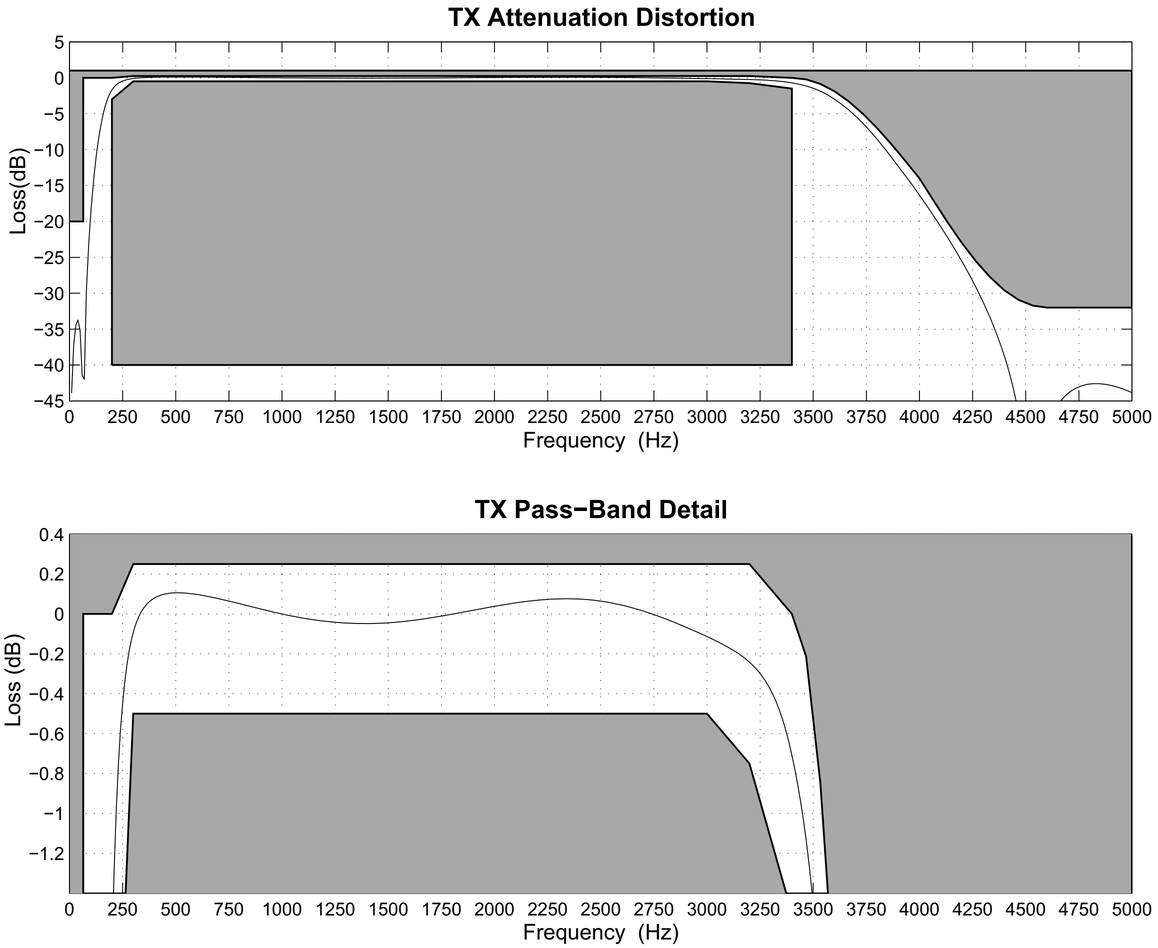


Figure 6. Transmit Path Frequency Response

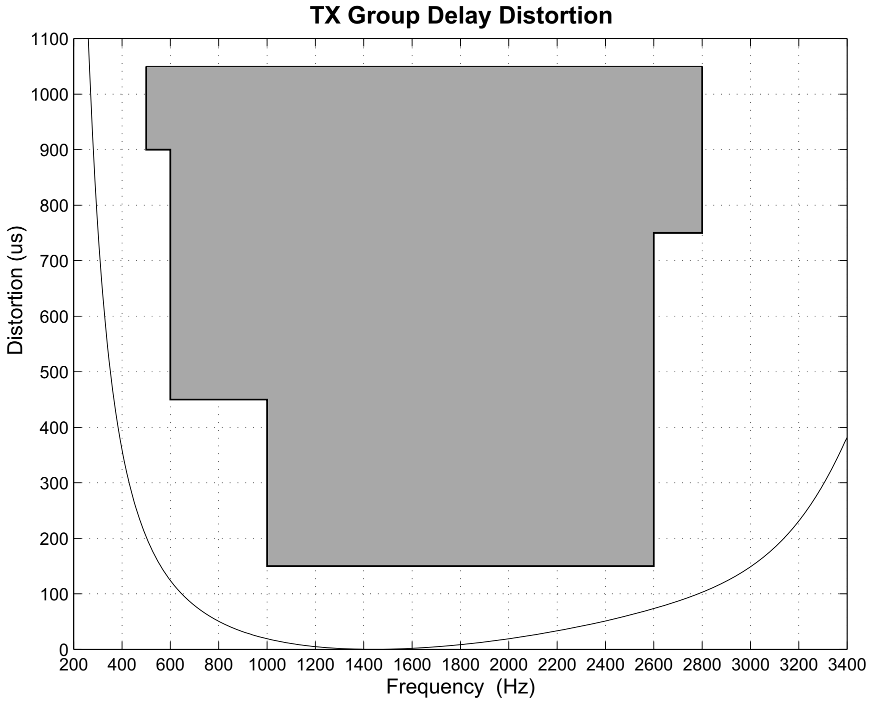


Figure 7. Transmit Group Delay Distortion

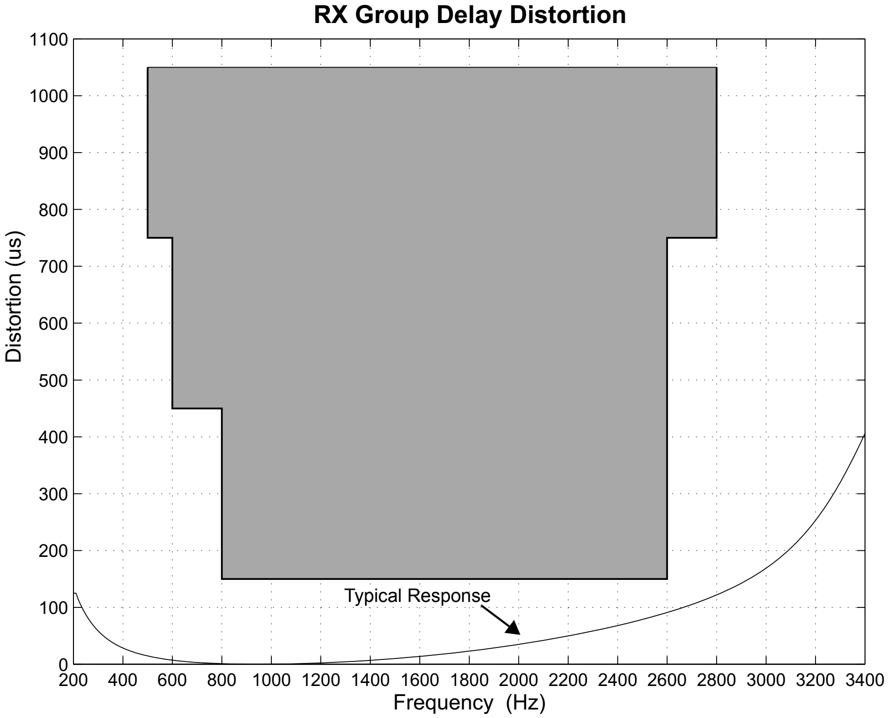


Figure 8. Receive Group Delay Distortion

Table 9. Thermal Conditions

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance, Typical* QFN-50	θ_{JA}		48	°C/W
Maximum Junction Temperature, QFN-50 (Linefeed Die)	T_{JHV}	Continuous	145	°C
Maximum Junction Temperature QFN-50 (Low Voltage Die)	T_{JLV}		125	°C

***Note:** The thermal resistance of an exposed pad package is assured when the recommended printed circuit board layout guidelines are followed correctly. The specified performance requires that the exposed pad be soldered to an exposed copper surface of at least equal size and that multiple vias are added to enable heat transfer between the top-side copper surface and a large internal/bottom copper plane

Table 10. Absolute Maximum Ratings[1]

Parameter	Symbol	Test Condition	Value	Unit
Storage Temperature Range	T_{STG}		–55 to 150	°C
Continuous Power Dissipation[2,3] QFN-50	P_D	$T_A = 85$ °C	1.25	W
Supply Voltage	V_{DDD}, V_{DDA}		–0.5 to 4.0	V
Digital Input Voltage	V_{IND}		–0.3 to 3.6	V
Battery Supply Voltage[4], Si32266/8	V_{BAT}		+0.4 to –115	V
Battery Supply Voltage[4], Si32267/9	V_{BAT}		+0.4 to –142	V
TIP or RING Voltage, Si32266/8[5]	V_{TIP}, V_{RING}		+0.4 to –130	V
TIP or RING Voltage, Si32267/9[5]	V_{TIP}, V_{RING}		+0.4 to –142	V
TIP, RING Current	I_{TIP}, I_{RING}		±100	mA

Notes:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet.
2. Operation of the Si3226x low voltage die above 125 °C junction temperature may degrade device reliability.
3. Si3226x linefeed is equipped with on-chip thermal limiting circuitry that shuts down the circuit when the junction temperature exceeds the thermal shutdown threshold.
4. The dv/dt of the voltage applied to the V_{BAT} pins must be limited to 10 V/µs.
5. Specification requires circuit for surge event as shown in typical application circuit. See “AN381: Si3226x ProSLIC Designer’s Guide.”

2. Typical Application Circuits

2.1. Si32266/7 Flyback Tracking DC-DC Converter

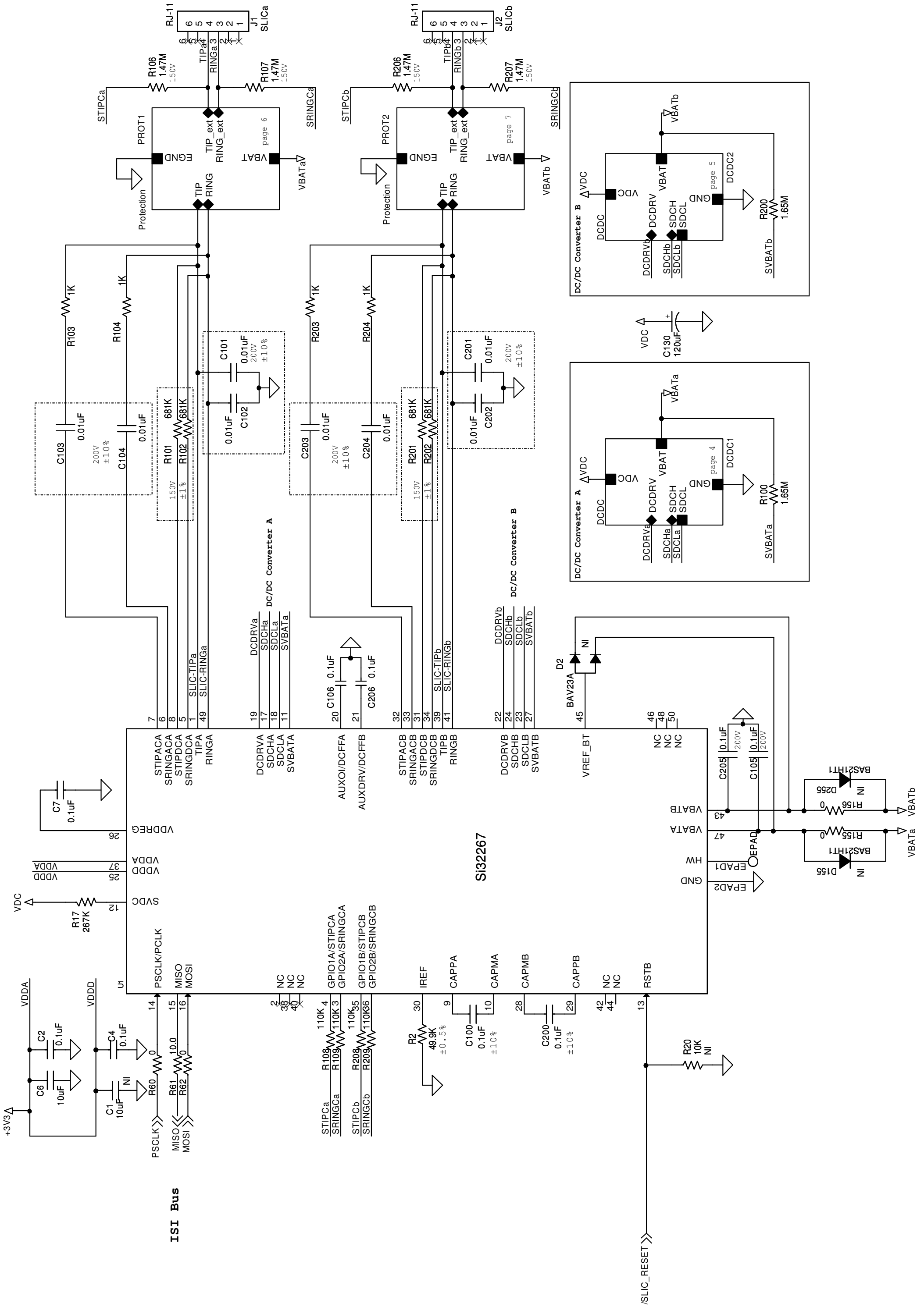


Figure 9. Si32266/7Flyback Tracking DC-DC Converter Top Level Schematic

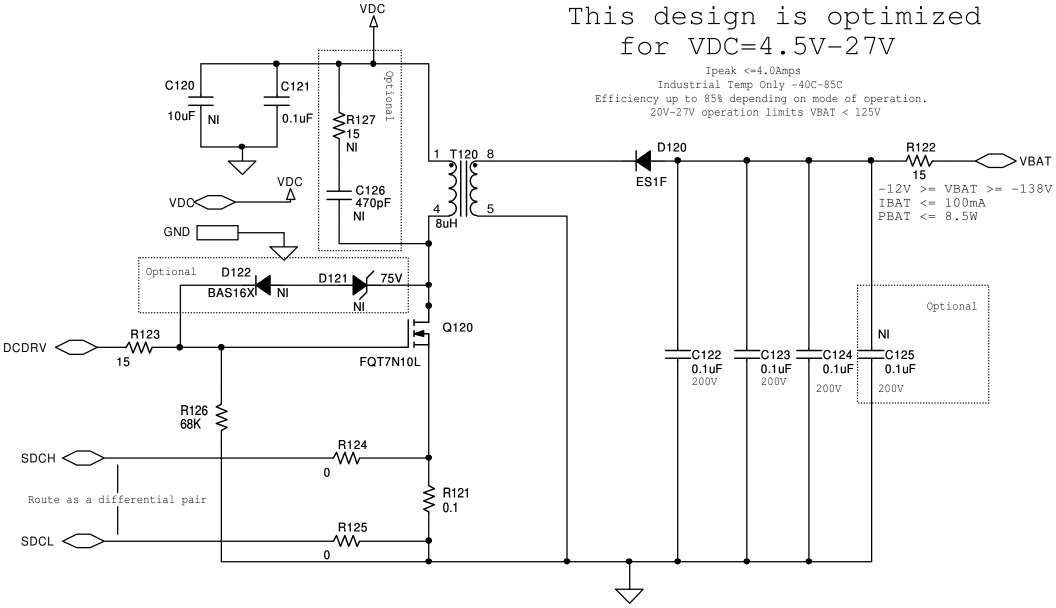


Figure 10. Si32266/7 Flyback Tracking DC DC1

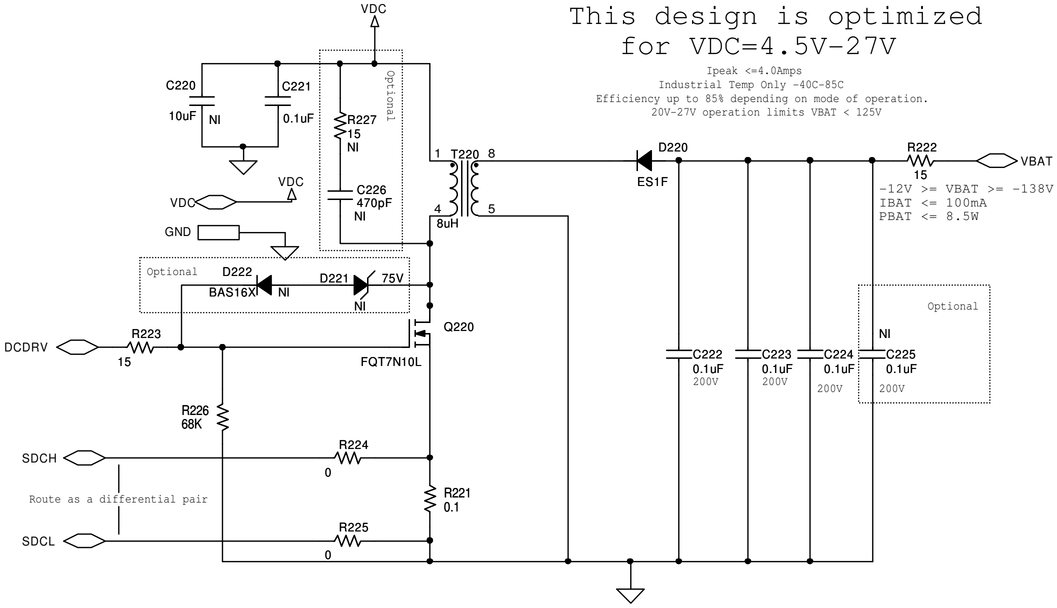


Figure 11. Si32266/7 Flyback Tracking DC DC2

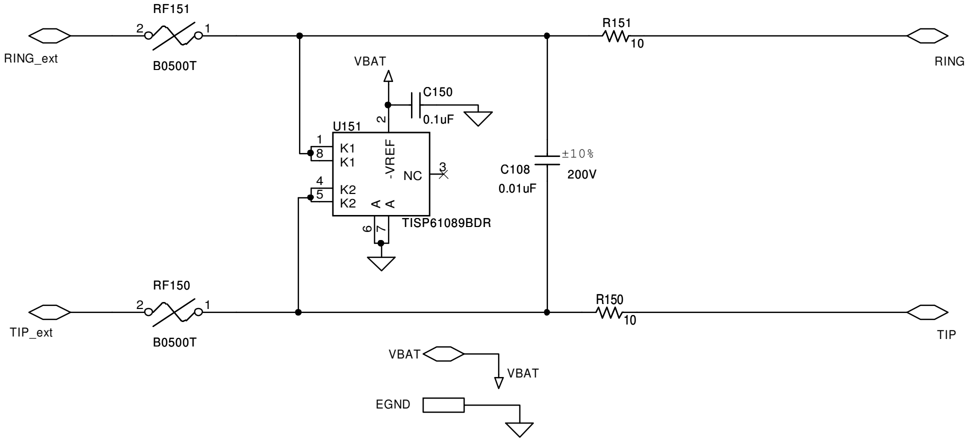


Figure 12. Si32266/7 Flyback Protection 1

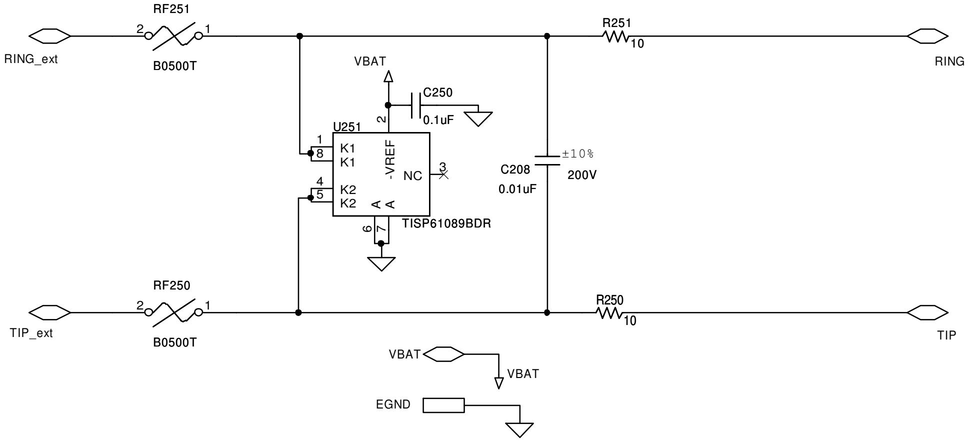


Figure 13. Si32266/7 Flyback Protection 2

2.2. Si32268 TSS DC-DC Converter

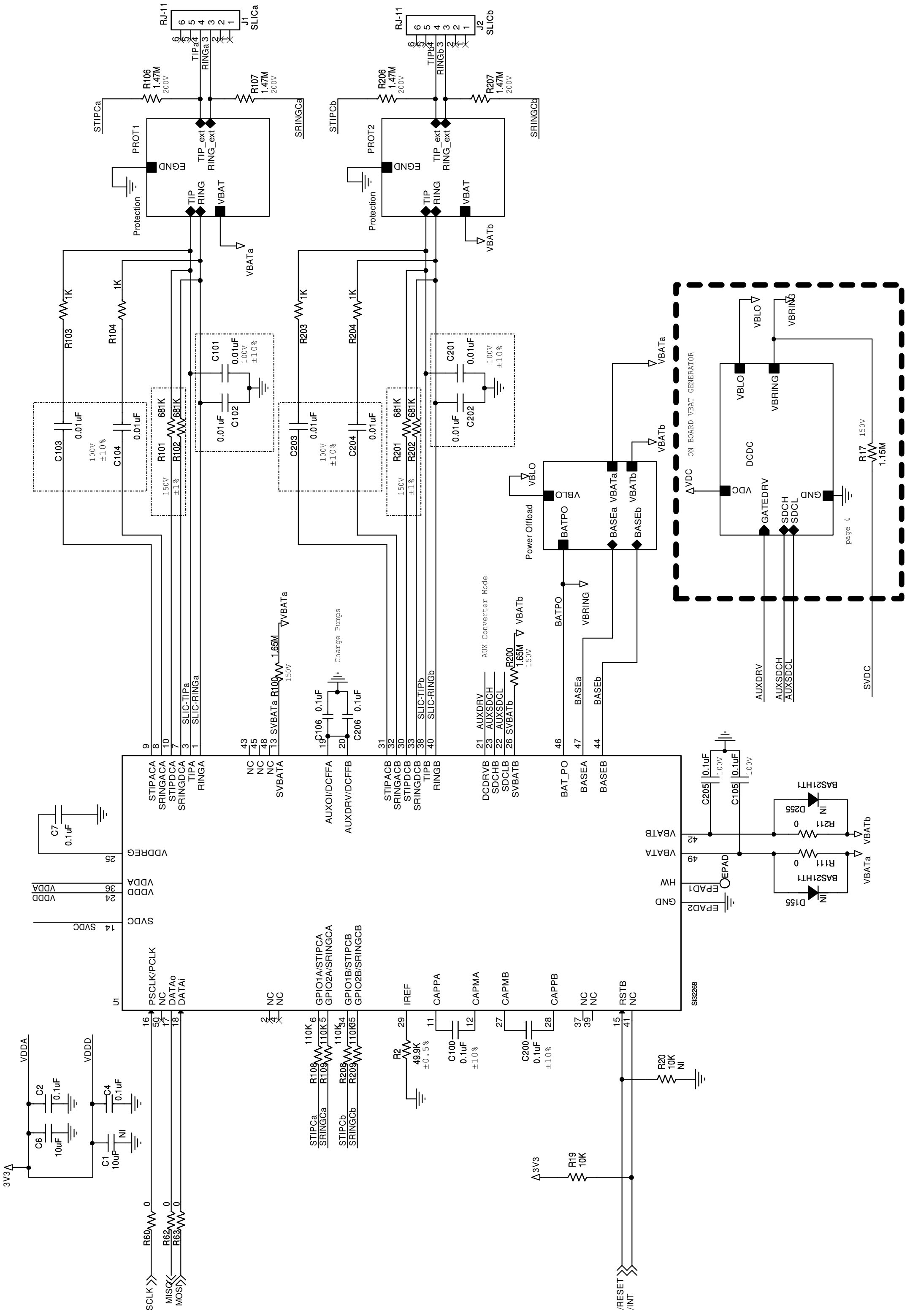
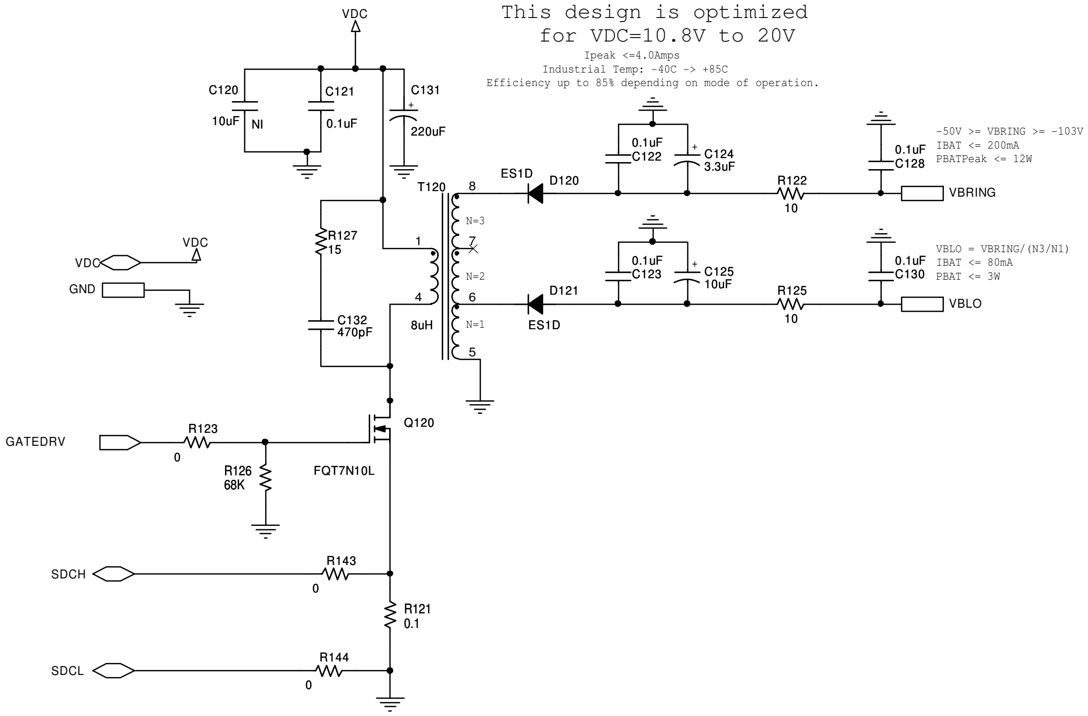


Figure 14. Si32268 TSS DC-DC Converter—Top Level Schematic



This design is optimized
for VDC=10.8V to 20V
Ipeak <=4.0Amps
Industrial Temp: -40C -> +85C
Efficiency up to 85% depending on mode of operation.

Figure 15. Si32268 TSS DC-DC Converter

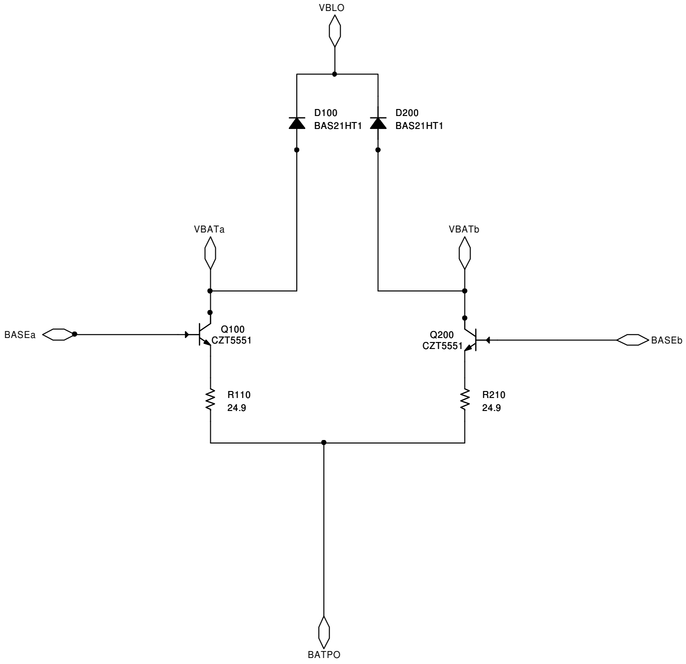


Figure 16. Si32268 TSS Power Offload

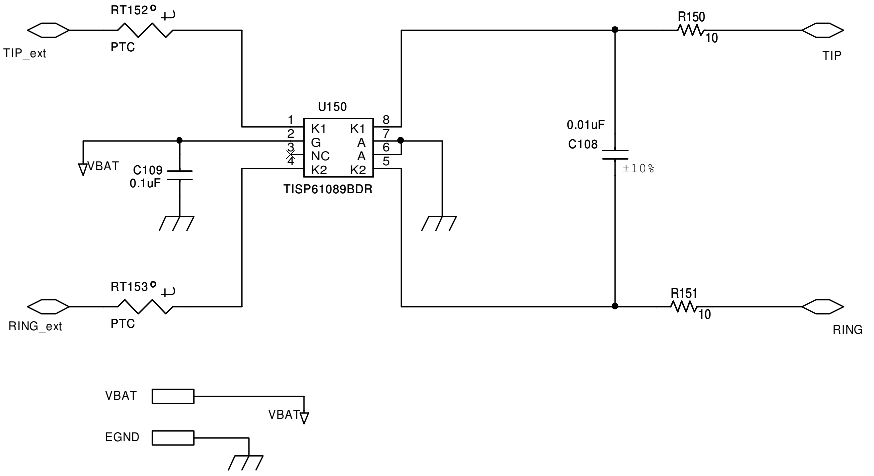


Figure 17. Si32268 TSS Protection 1

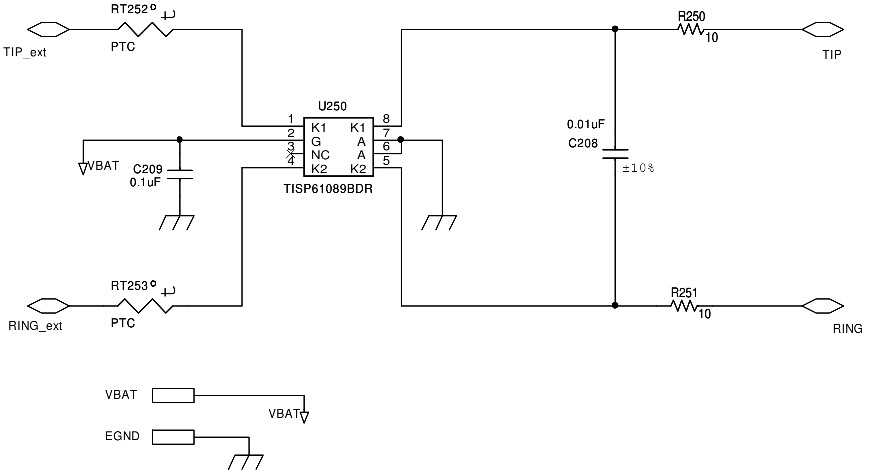


Figure 18. Si32268 TSS Protection 2

3. Bill of Materials

Table 11. Si32267 Flyback Tracking DC-DC Converter Bill of Materials—Top Level

Ref	Value	Rating	Volt	Tol	Type	PCB Footprint	Mfr Part Number	Mfr
C1 (NI)	10uF		6.3V	±20%	X5R	C0603	C0603X5R6R3-106M	Venkel
C120 (NI) C220 (NI)	10uF		25V	±20%	X7R	C1210	C1210X7R250-106M	Venkel
C125 (NI) C225 (NI)	0.1uF		200V	±20%	X7R	C1206	C1206X7R201-104M	Venkel
C126 (NI) C226 (NI)	470pF		100V	±10%	X7R	C0603	C0603X7R101-471K	Venkel
D2 (NI)	BAV23A	400mA	200V		DUAL	SOT23-KKA	BAV23A	Diodes Inc.
C105 C205	0.1uF		200V	±20%	X7R	C1206	C1206X7R201-104M	Venkel
C130	120uF	600mA	63V	±20%	Alum_Elec	C5X10MM-RAD	EEUFC1J121	Panasonic
Q120 Q220	FQT7N10L	1.7A	100V		Nchan	SOT223-GDS	FQT7N10L	Fairchild
RF150 RF151 RF250 RF251	B0500T	0.5A	600V		TelCom	FUSE-B0500T	B0500T	Bourns
R61	10	1/16W		±1%	ThickFilm	R0603	CR0603-16W-10R0F	Venkel
R100 R200	1.65M	1/10W		±1%	ThickFilm	R0805	CR0805-10W-1654F	Venkel
R101 R102 R201 R202	681K	1/10W		±1%	ThickFilm	R0805	CR0805-10W-6813F	Venkel
R103 R104 R203 R204	1K	1/10W		±1%	ThickFilm	R0603	CR0603-10W-1001F	Venkel
R106 R107 R206 R207	1.47M	1/8W		±1%	ThickFilm	R1206	CR1206-8W-1474F	Venkel
R155 R156	0	2A			ThickFilm	R0805	CR0805-10W-000	Venkel
U1	Si32267		-136V		MCM	NBA50N6X8P 0.5	Si32267-C	SiLabs
R17	267K	1/10W		±1%	ThickFilm	R0805	CR0805-10W-2673F	Venkel
R60 R62	0	1A			ThickFilm	R0402	CR0402-16W-000	Venkel
C150 C250	0.1uF		200V	±20%	X7R	C1206	C1206X7R201-104M	Venkel
R2	49.9K	1/16W		±0.5%	ThickFilm	R0603	CR0603-16W-4992D	Venkel
J1 J2	RJ-11				RJ-11	RJ11-6-SMT	5555077-2	AMP

Table 12. Si32267 Flyback Tracking DC-DC Converter Bill of Materials—DC-DC

Ref	Value	Rating	Volt	Tol	Type	PCB Footprint	Mfr Part Number	Mfr
D122 (NI) D222 (NI)	BAS16X	200mA	75V		Single	SOD523	BAS16XV2T1G	On Semi
D155 (NI) D255 (NI)	BAS21HT1	200mA	250V		Single	SOD-323	BAS21HT1	On Semi
R20 (NI)	10K	1/16W		±5%	ThickFilm	R0402	CR0402-16W-103J	Venkel
R127 (NI) R227 (NI)	15	1/2W		±5%	ThickFilm	R1210	CR1210-2W-150J	Venkel
C2 C4 C7 C100 C106 C200 C206	0.1uF		10V	±10%	X7R	C0402	C0402X7R100-104K	Venkel
C6	10uF		6.3V	±20%	X5R	C0603	C0603X5R6R3-106M	Venkel
C108 C208	0.01uF		200V	±10%	X7R	C0805	C0805X7R201-103K	Venkel
C121 C221	0.1uF		50V	±10%	X7R	C0603	C0603X7R500-104K	Venkel
C122 C123 C124 C222 C223 C224	0.1uF		200V	±20%	X7R	C1206	C1206X7R201-104M	Venkel
D120 D220	ES1F	1.0A	300V		Single	DO-214AC	ES1F	Fairchild
R108 R109 R208 R209	110K	1/16W		±1%	ThickFilm	R0402	CR0402-16W-1103F	Venkel
R121 R221	0.1	1/2W		±1%	ThickFilm	R1210	LCR1210-R100F	Venkel
R122 R222	15	1/2W		±5%	ThickFilm	R1210	CR1210-2W-150J	Venkel
R123 R223	15	1/16W		±1%	ThickFilm	R0402	CR0402-16W-15R0F	Venkel
R124 R125 R224 R225	0	1A			ThickFilm	R0402	CR0402-16W-000	Venkel
R126 R226	68K	1/16W		±5%	ThickFilm	R0402	CR0402-16W-683J	Venkel
T120 T220	8uH	4A				XFMR-UTB01701s	UTB01890s	UMEC

Table 13. Si32267 Flyback Tracking DC-DC Converter Bill of Materials—Protection

Ref	Value	Rating	Volt	Tol	Type	PCB Footprint	Mfr Part Number	Mfr
D121 (NI) D221 (NI)	75V	200mW	75V		Zener	SOD-123	BZX384C75-V	Vishay
C101 C102 C103 C104 C201 C202 C203 C204	0.01uF		200V	±10%	X7R	C0805	C0805X7R201-103K	Venkel
R150 R151 R250 R251	10	1/10W		±1%	Thick-Film	R0805	CR0805-10W-10R0F	Venkel
U151 U251	TISP61089BDR		-150V		SLIC	SO8N6.0P1.27	TISP61089BDR	Bourns

Table 14. Si32268 TSS DC-DC Converter Application Circuit Bill of Materials—Top Level

Ref	Value	Rating	Volt	Tol	Type	PCB Footprint	Mfr Part Number	Mfr
C1 (NI)	10uF		6.3V	±20%	X5R	C0603	C0603X5R6R3-106M	Venkel
C120 (NI)	10uF		25V	±20%	X7R	C1210	C1210X7R250-106M	Venkel
D155 (NI) D255 (NI)	BAS21HT1	200mA	250V		Single	SOD-323	BAS21HT1	On Semi
R20 (NI)	10K	1/16W		±5%	ThickFilm	R0402	CR0402-16W-103J	Venkel
C2 C4 C7 C100 C106 C200 C206	0.1uF		10V	±10%	X7R	C0402	C0402X7R100-104K	Venkel
D100 D200	BAS21HT1	200mA	250V		Single	SOD-323	BAS21HT1	On Semi
D120 D121	ES1D	1.0A	200V		Single	DO-214AC	ES1D	Diodes Inc.
RT152 RT153 RT252 RT253	PTC	3A	250V		TelCom	PTC-MF-SM013/250V	MF-SM013/250V	Bourns
R2	49.9K	1/16W		±0.5%	ThickFilm	R0603	CR0603-16W-4992D	Venkel
R17	1.15M	1/10W		±1%	ThickFilm	R0805	CR0805-10W-1154F	Venkel
R19	10K	1/16W		±5%	ThickFilm	R0402	CR0402-16W-103J	Venkel
R60 R62 R63	0	1A			ThickFilm	R0402	CR0402-16W-000	Venkel
R100 R200	1.65M	1/10W		±1%	ThickFilm	R0805	CR0805-10W-1654F	Venkel
R101 R102 R201 R202	681K	1/10W		±1%	ThickFilm	R0805	CR0805-10W-6813F	Venkel
R103 R104 R203 R204	1K	1/10W		±1%	ThickFilm	R0603	CR0603-10W-1001F	Venkel

Table 14. Si32268 TSS DC-DC Converter Application Circuit Bill of Materials—Top Level

Ref	Value	Rating	Volt	Tol	Type	PCB Footprint	Mfr Part Number	Mfr
R106 R107 R206 R207	1.47M	1/8W		±1%	ThickFilm	R1206	CR1206-8W-1474F	Venkel
R108 R109 R208 R209	110K	1/16W		±1%	ThickFilm	R0402	CR0402-16W-1103F	Venkel
R111 R211	0	2A			ThickFilm	R0805	CR0805-10W-000	Venkel
U1	Si32268		–110V		MCM	NBA50N6X8P0.5	Si32268-C	SiLabs

Table 15. Si32268 TSS DC-DC Converter Application Circuit Bill of Materials—DC-DC

Ref	Value	Rating	Volt	Tol	Type	PCB Footprint	Mfr Part Number	Mfr
C105 C205	0.1uF		100V	±20%	X7R	C0603	C0603X7R101-104M	Venkel
C108 C208	0.01uF		100V	±10%	X7R	C0603	C0603X7R101-103K	Venkel
C109 C209	0.1uF		200V	±20%	X7R	C1206	C1206X7R201-104M	Venkel
C121	0.1uF		25V	±20%	X7R	C0603	C0603X7R250-104M	Venkel
C122 C123 C128 C130	0.1uF		100V	±20%	X7R	C0603	C0603X7R101-104M	Venkel
C124	3.3uF		200V	±20%	Alum_Elec	C2.5X6.3MM-RAD	UVR2D3R3MED	Nichicon
C125	10uF		160V	±20%	Alum_Elec	C5X10MM-RAD	ECA2CM100	Panasonic
C132	470pF		100V	±10%	X7R	C0603	C0603X7R101-471K	Venkel
Q100 Q200	CZT5551	2W	180V		NPN	SOT223-BCE	CZT5551	Central Semi
R121	0.1	1/2W		±1%	ThickFilm	R1210	LCR1210-R100F	Venkel
R122 R125	10	1/4W		±1%	ThickFilm	R1206	CR1206-4W-10R0F	Venkel
R123 R143 R144	0	1A			ThickFilm	R0402	CR0402-16W-000	Venkel
R126	68K	1/16W		±5%	ThickFilm	R0402	CR0402-16W-683J	Venkel
R127	15	1/4W		±5%	ThickFilm	R1206	CR1206-4W-150J	Venkel
T120	8uH	5A, 25W				XFMR-UTB01701s	UTB01701s	UMEC

Table 16. Si32268 TSS DC-DC Converter Application Circuit Bill of Materials—Power Offload

Ref	Value	Rating	Volt	Tol	Type	PCB Footprint	Mfr Part Number	Mfr
C131	220uF	555mA	25V	±20%	Alum_Elec	C3.5X8MM-RAD	EEUFC1E221	Panasonic
J1 J2	RJ-11				RJ-11	RJ11-6-SMT	5555077-2	Tyco
R110 R210	24.9	1/4W		±1%	ThickFilm	R1206	CR1206-4W-24R9F	Venkel

Table 17. Si32268 TSS DC-DC Converter Application Circuit Bill of Materials—Protection

Ref	Value	Rating	Volt	Tol	Type	PCB Footprint	Mfr Part Number	Mfr
C6	10uF		6.3V	±20%	X5R	C0603	C0603X5R6R3-106M	Venkel
C101 C102 C103 C104 C201 C202 C203 C204	0.01uF		100V	±10%	X7R	C0603	C0603X7R101-103K	Venkel
Q120	FQT7N10L	1.7A	100V		Nchan	SOT223-GDS	FQT7N10L	Fairchild
R150 R151 R250 R251	10	1/10W		±1%	ThickFilm	R0805	CR0805-10W-10R0F	Venkel
U150 U250	TISP61089BDR		–150V		SLIC	SO8N6.0P1.27	TISP61089BDR	Bourns

4. Functional Description

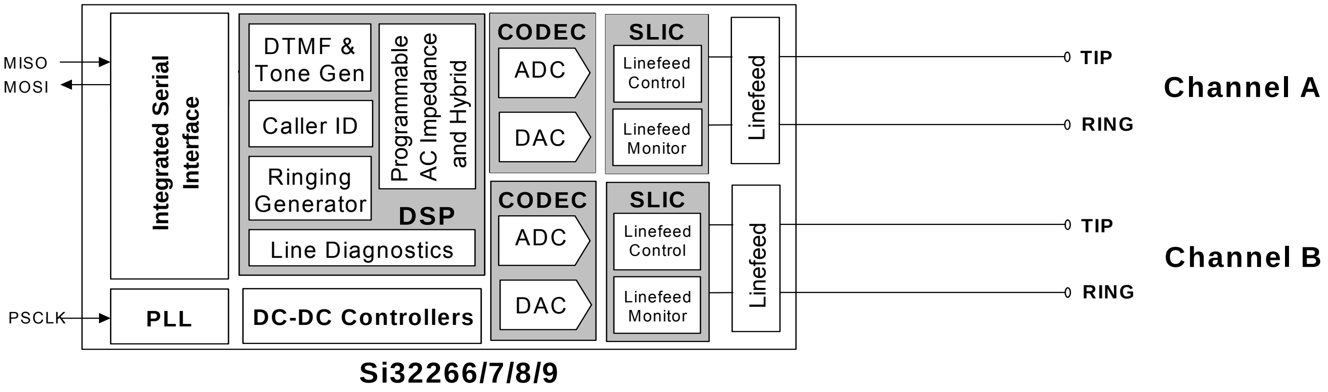


Figure 19. Functional Block Diagram

The Si3226x dual ProSLIC devices provide all SLIC, codec, DTMF detection, and signal generation functions needed for two complete analog telephone interfaces. They perform all battery, over-voltage, ringing, supervision, codec, hybrid, and test (BORSCHT) functions, and also support extensive metallic loop testing capabilities.

The Si3226x devices provide a standard voice-band (200 Hz–3.4 kHz) audio codec and, optionally, an audio codec with both wideband (50 Hz–7 kHz) and standard voiceband modes. The wideband mode provides an expanded audio band with a 16 kHz sample rate for enhanced audio quality while the standard voice-band mode provides standard telephony audio bandwidth.

The Si3226x devices incorporate programmable dc-dc converter controllers that can operate in either battery tracking mode (Si32266/7) or a shared rail mode (Si32268/9). In both the battery tracking and the shared rail modes the dc-dc converter controllers react to line conditions to provide the optimal battery voltage required for each line-state. Multiple Si32268/9 devices can also operate from fixed rail supplies controlled either by one of the integrated dc-dc controllers or by an external dc-dc controller. The Si3226x devices are available with voltage ratings of –110 or –140 V to support a wide range of ringing voltages. See Section "8. Ordering Guide," on page 42 for the voltage rating of each version.

Programmable on-hook voltage, programmable offhook loop current, reverse battery operation, loop or ground start operation, and on-hook transmission are supported. Loop current and voltage are continuously monitored by an integrated monitoring ADC. The Si3226x dual ProSLIC devices support balanced and unbalanced 5 REN ringing with or without a programmable dc offset, and can operate in low power ringing and adaptive ringing modes. The available offset, frequency, waveshape, and cadence options are designed to ring the widest variety of terminal devices and to reduce external controller requirements.

A complete audio transmit and receive path is integrated, including ac impedance and hybrid gain. These features are software-programmable, allowing a single hardware design to meet global requirements.

5. FXS Features

5.1. DC Feed Characteristics

ProSLIC internal linefeed circuitry provides completely programmable dc feed characteristics.

When in the active state, the ProSLIC operates in one of three dc linefeed operating regions: a constant-voltage region, a constant-current region, or a resistive region, as shown in Figure 20. The constant-voltage region has a low resistance, typically 160 Ω. The constant-current region approximates infinite resistance.

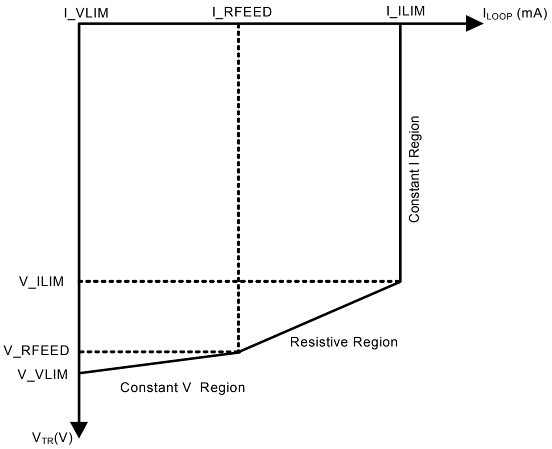


Figure 20. Dual ProSLIC DC Feed Characteristics

5.2. Linefeed Operating States

The linefeed interface includes nine different register-programmable operating states as listed in Table 18. The Open state is the default condition in the absence of any preloaded register settings. The device may also automatically enter the open state in the event of a linefeed fault condition.

5.3. Line Voltage and Current Monitoring

The ProSLIC continuously monitors the TIP, RING, and battery voltages and currents via an on-chip ADC and stores the resulting values in individual RAM locations. Additionally, the loop voltage (V_{TIP}–V_{RING}), loop current, and longitudinal current values are calculated based on the TIP and RING measurements and are stored in unique register locations for further processing. The ADC updates all registers at a rate of 2 kHz or greater.

5.4. Power Monitoring and Power Fault Detection

The Si3226x line monitoring functions are used to continuously protect against excessive power conditions. The Si3226x contains on-chip, analog sensing diodes that turn off the device when a preset temperature threshold is exceeded.

If the Si3226x detects a fault condition or overpower condition, it automatically sets that line to the open state and generates a "power alarm" interrupt.

The interrupt can be masked, but masking the automatic transition to open is not recommended.

The various power alarms and linefeed faults supporting automatic intervention are described below.

1. Total power exceeded.
2. Excessive foreign current or voltage on TIP and/or RING.
3. Thermal shutdown event.

5.5. Thermal Overload Shutdown

If the die temperature exceeds the maximum junction temperature threshold (TJmax) of 145 or 200 °C, depending on the operating state, the device has the ability to shut itself down to a low-power state without user intervention.

Table 18. Linefeed Operating States

Linefeed State	Description
Open	Output is high-impedance and all line supervision functions are powered down. Audio is not transmitted. This is the default state after powerup or following a hardware reset. This state can also be used in the presence of line fault conditions and to generate open switch intervals (OSIs). This state is used in line diagnostics mode as a high impedance state during linefeed testing. A power fault condition may also force the device into the open state.
Forward Active Reverse Active	Linefeed circuitry and audio are active. In Forward Active state, the TIP lead is more positive than the RING lead; in Reverse Active state, the RING lead is more positive than the TIP lead. Loop closure and ground key detect circuitry are active.
Forward OHT Reverse OHT	Provides data transmission during an on-hook loop condition (e.g., transmitting caller ID data between ringing bursts). Linefeed circuitry and audio are active. In Forward OHT state, the TIP lead is more positive than the RING lead; in Reverse OHT state, the RING lead is more positive than the TIP lead.
TIP Open	Provides an active linefeed on the RING lead and sets the TIP lead to high impedance (>400 kΩ) for ground start operation in forward polarity. Loop closure and ground key detect circuitry are active.
RING Open	Provides an active linefeed on the TIP lead and sets the RING lead to high impedance (>400 kΩ) for ground start operation in reverse polarity. Loop closure and ground key detect circuitry are active.
Ringing	Drives programmable ringing signal onto TIP and RING leads with or without dc offset.
Line Diagnostics	The channel is put into diagnostic mode. In this mode, the channel has special diagnostic resources available.

5.6. Loop Closure Detection

The Si3226x provides a completely programmable loop closure detection mechanism. The loop closure detection scheme provides two unique thresholds to allow hysteresis, and also includes a programmable debounce filter to eliminate false detection. A loop closure detect status bit provides continuous status, and a maskable interrupt bit is also provided.

5.7. Ground Key Detection

The Si3226x provides a ground key detect mechanism using a programmable architecture similar to the loop closure scheme. The ground key detect scheme provides two unique thresholds to allow hysteresis and also includes a programmable debounce filter to eliminate false detection. A ground key detect status bit provides continuous status, and a maskable interrupt bit is also provided.

5.8. Ringing Generation

The Si3226x provides the ability to generate a programmable sinusoidal or trapezoidal ringing waveform, with or without dc offset. The ringing frequency, wave shape, cadence, and offset are all register-programmable. Three ringing modes are supported: balanced, unbalanced, and low-power ringing (LPR). Figure 21 illustrates the fundamental differences between the three ringing modes.

The dual ProSLIC's adaptive ringing capability allows further power savings to be realized in systems designed for long loop applications. In a long loop system, it may be necessary to generate a large ringing voltage to ensure that sufficient voltage is presented to a phone at the far end of the loop. However, in situations when a short loop is connected to an FXS interface that was designed with the ability to ring long loops, the large ringing voltage in combination with a low resistance load will result in excessive and unnecessary power consumption. Silicon Labs' Si3226x dual ProSLICs eliminate this unnecessary power consumption with their adaptive ringing capability. The ProSLIC automatically senses when excessive power is being consumed in the line feed circuit (due to the lower resistance of a short loop) and will iteratively reduce the ringing amplitude to a voltage that is appropriate for the load.

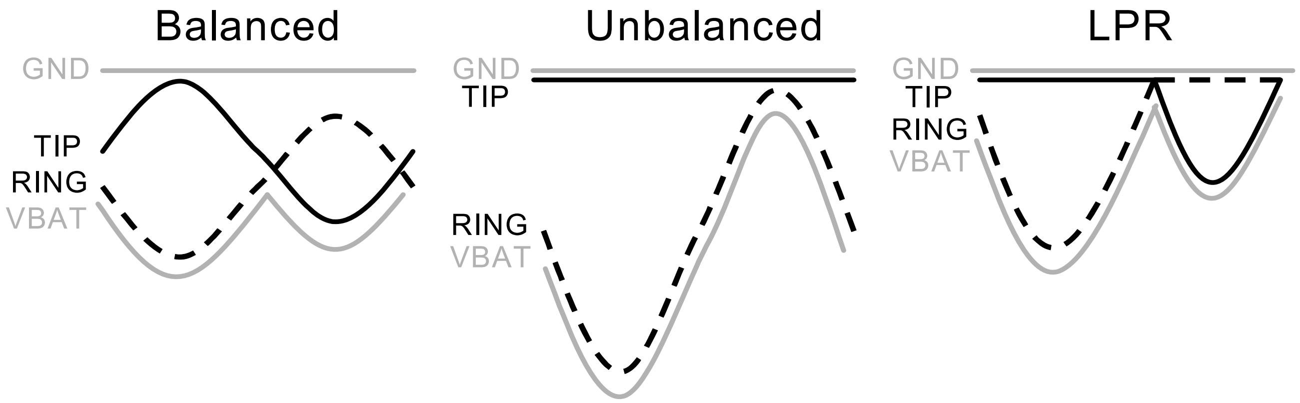


Figure 21. Ringing Modes

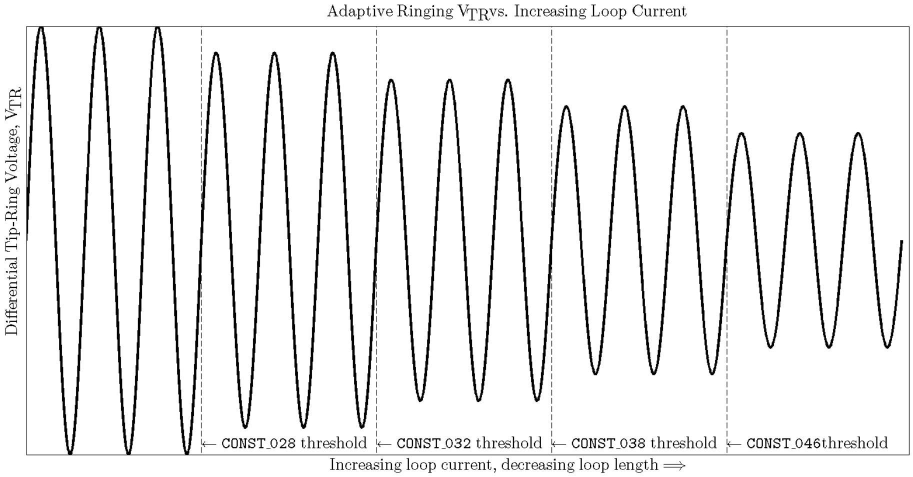


Figure 22. Adaptive Ringing

5.9. Polarity Reversal

The Si3226x supports polarity reversal for message waiting and various other signaling modes. The ramp rate can be programmed for a smooth or abrupt transition to accommodate different application requirements.

5.10. Two-Wire Impedance Synthesis

The ac two-wire impedance synthesis is generated on-chip using a DSP-based scheme to optimally match the output impedance of the Si3226x to the reference impedance. Most real or complex two-wire impedances can be generated by using the coefficient generator software to simulate the desired line conditions and generate the required register coefficients.

5.11. Transhybrid Balance Filter

The trans-hybrid balance function is implemented on-chip using a DSP-based scheme to effectively cancel the reflected receive path signal from the transmit path. The coefficient generator software is used to optimize the filter coefficients.

5.12. Tone Generators

The Si3226x includes two digital tone generators that allow a wide variety of single- or dual-tone frequency and amplitude combinations. Each tone generator has its own set of registers that hold the desired frequency, amplitude, and cadence to allow generation of DTMF and call progress tones for different requirements. The tones can be directed to either receive or transmit paths.

5.13. DTMF Detection

The Dual ProSLIC performs DTMF detection.

5.14. Pulse Metering

The pulse metering system for the Si3226x is designed to inject a 12 or 16 kHz billing tone into the audio path with maximum amplitude of 0.5 V_{RMS} at TIP and RING into a 200 Ω ac load impedance. The tone is generated in the DSP via a table lookup that guarantees spectral purity by not allowing drift. The tone will ramp up until it reaches a host-programmed threshold, at which point it will maintain that level until instructed to ramp down, thus creating a trapezoidal envelope.

See AN381 for additional details and considerations on Pulse Metering.

5.15. DC-DC Controller

The Si32266/7 integrated line feeds are designed to work with a tracking high voltage input, one for each channel. The Si32266/7 integrates two dc-dc controllers that can be used to control external tracking dc-dc converters to generate high voltage supplies to the SLIC channels. The Si32266/7 VBATa and VBATb inputs are each directly connected to the high voltage output of two tracking dc-dc converters, one for channel A and one for channel B. The VBAT voltage for each channel is optimized to minimize power consumption by closely tracking the SLIC state, even tracking the ringing waveforms (see Section“2.1. Si32266/7 Flyback Tracking DC-DC Converter” for schematics).

The Si32268/9 integrated line feeds are designed to work with two high voltage supplies shared by both channels. The Si32268/9 integrates a single dc-dc controller that can be used to control a single external dc-dc converter to generate two high voltage supplies shared by both SLIC channels. The single flyback dc-dc converter generates two rails using two taps on the dc-dc converter's transformer. External power offloading transistors are used to lower the power dissipated inside the Si32268/8 devices by shunting excess power away from the ProSLIC. In tracking shared supply (TSS) mode, in a two channel implementation, the dc-dc converter is controlled by the integrated dc-dc controller which allows the high voltage and low voltage outputs from the dc-dc converter to track the combined state of the two channels of the Si3226x ProSLIC, including the ringing waveforms. Using the same schematic, the TSS mode of operation reduces system power consumption significantly when compared to typical fixed rail shared supply designs (see Section “2.2. Si32268 TSS DC-DC Converter” for schematics).

The dc-dc controller outputs DCDRVa/b are driven by an internal charge pump which allows them to connect directly to the gate of the N-channel MOSFET switch of a dc-dc converter. This connection eliminates the need for the MOSFET pre-drive circuit that is required when VTH is greater than VDD. See Table 6.

5.16. Wideband Audio

The Si3226x dual ProSLIC devices support a software-selectable wideband (50 Hz–7 kHz) and narrowband (200 Hz–3.4 kHz) audio codec. The wideband mode provides an expanded audio band at a 16-bit, 16 kHz sample rate for enhanced audio quality while maintaining standard telephony audio compatibility. In wideband operation, two time slots are used to transmit the wideband signal and each slot contains 8-bits of the 16-bit sample. These two time slots are transmitted and received half a frame apart, but within the same 8 kHz frame.

5.17. In-Circuit and Metallic Loop Testing

A rich set of features is provided for in-circuit testing of the FXS system and the connected telephone line (MLT):

- Tone generators
- Audio diagnostic filters
- Digital and analog loop-back modes
- Internal test load
- Monitor ADC
- DSP algorithms

Using these facilities, it is possible to test the Si3226x dc-dc converter, codec, line-feed, PCM bus interface, DSP, SPI bus interface, and call progress state-machine as well as testing the connected telephone line and external protection circuitry.

The audio diagnostic filters on the FXS are intended to provide programmable filtering of the TX digital audio signal and calculate the peak and/or average signal power of the filters' outputs. The signal powers are then compared to programmable thresholds. The programmable filters can be used to band-pass filter a certain tone or notch out certain tones, so that the signal power measurements are frequency selective. This filtering is useful in a telephony system because it can measure harmonic distortion, intermodulation, noise, etc.

The Si3226x incorporates an internal test load with a 2.2 kΩ nominal value that can be connected across Tip/Ring (Figure 23). The audio diagnostics system and built-in test load can be used to test the FXS interface (Si3226x) itself without requiring an external load, a connected line, or any relays. This facility can be used for production and in-service testing of such things as:

- Dial tone draw/break
- Audio quality measurements
- Pulse digit detection
- DC feed
- Ringtrip
- Polarity reversal
- Transmission loss

MLT, e.g., GR-909, is facilitated by the built-in DSP, monitor ADC, and test load. They provide the ability to detect multiple fault conditions within the CPE as well as on the Tip/Ring pair (T-R). Thirteen different measured and/or calculated parameters are reported by the Monitor ADC. Host software for use in conjunction with the ProSLIC API is available from Silicon Labs. Typical MLT tests include:

- Hazardous Potential Test – This checks for ac voltage > 50 V_{RMS} or dc voltage > 135 V between Tip and Ground (T-G) or Ring and Ground (R-G).
- Foreign Electromotive Force Test – Checks T-G or R-G for ac voltage > 10 V_{RMS} or dc voltage > 6 V. Uses same threshold as for hazardous voltage test.
- Resistive Faults Test – Checks for dc resistance from T-R, T-G or R-G. Any measurement < 150 kΩ is considered a resistive fault.
- Receiver-Off-Hook Test – Distinguishes between a T-R resistive fault and an off-hook condition.
- Ringers Test – Measures the magnitude of the connected ring load (REN) across T-R. Results are > 0.175 REN and < 5 REN for a valid load
- AC Line Impedance (line length) – T-R, T-G, and R-G. Generates a tone at several specific frequencies (audio band) and measures the reflected signal amplitude (complex spectrum) that comes back (with transhybrid balance filter disabled). The reflected signal is then used to calculate the line impedance based on certain assumptions of wire gauge, etc.
- Line Capacitance – T-R, T-G, R-G. Generates a linear ramp function with polarity reversal, and measures the time constant.

Diagnostic information is available even in the presence of fault conditions that cause the system's protection devices (fuses, PTCs, etc.) to open. A high-impedance sensing path (pins SRINGC and STIPC) can be used to measure the conditions on Tip/Ring even when the FXS system is effectively disconnected from the line. No relay is required and this sensing path inherently meets Dielectric Withstand per GR-49 (> 1000 V).

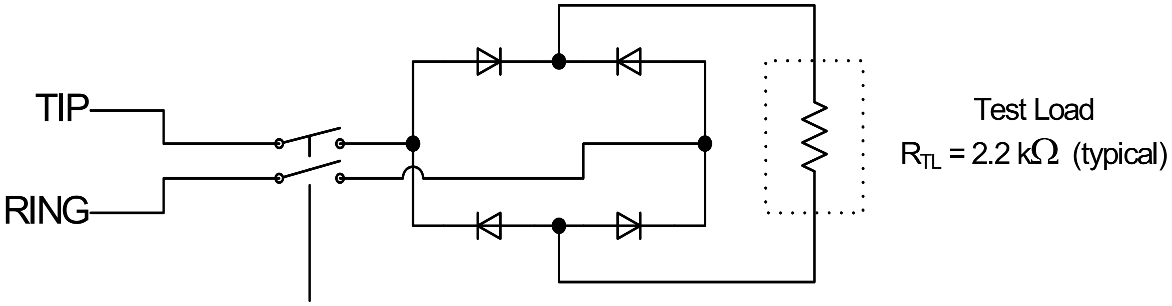


Figure 23. Si32266/7/8/9 Internal Test Load Circuit

6. Integrated Serial Interface

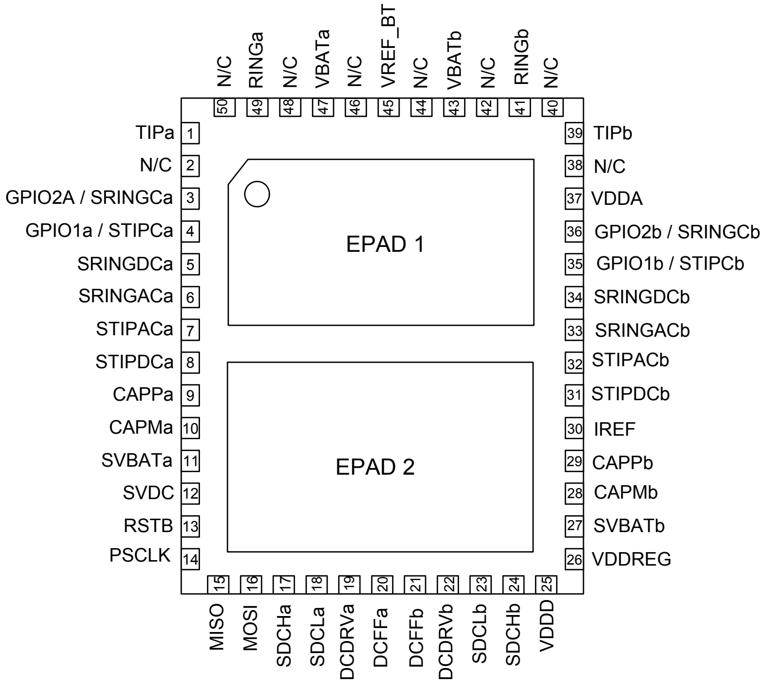
The Si32266/7/8/9 devices' integrated serial interface (ISI) is a three-wire proprietary interface which serializes SPI and PCM communications, reducing the SoC interface from nine wires to three (PSCLK, MISO, MOSI). SPI communications and PCM data transfers are embedded in the serial data. The host side of the ISI is integrated onto selected SoCs from several vendors.

ISI is a point to point interface, it is not possible to daisy chain more than one ISI ProSLIC device.

Both µ-255 Law (µ-Law) and A-law companding formats are supported in addition to 16-bit linear data mode with no companding.

7. Pin Descriptions

7.1. Si32266/7 Pin Assignments

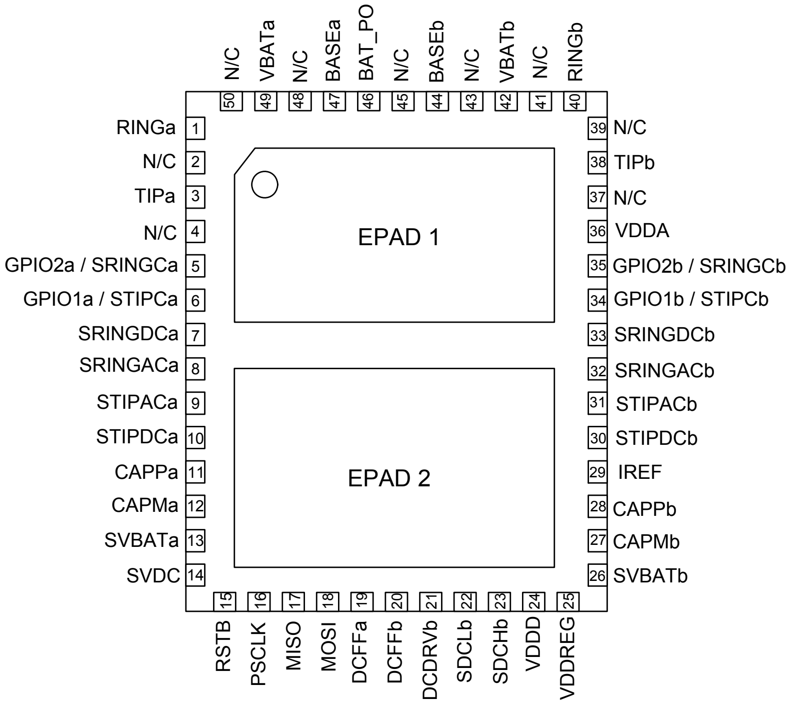


Pin #	Pin Name	Description
1	TIPa	**TIP Terminal—Channel A.** Connect to the TIP lead of the channel A subscriber loop.
2	N/C	**No Connect.** This pin should be left unconnected.
3	GPIO2a/SRINGCa	**General Purpose I/O** or **RING Coarse Sense Input—Channel A.** RING channel A Voltage sensing outside protection circuit.
4	GPIO1a/STIPCa	**General Purpose I/O** or **TIP Coarse Sense Input—Channel A.** TIP channel A voltage sensing outside protection circuit.
5	SRINGDCa	**RING DC Sense Input—Channel A.** Analog dc input to sense voltage on the channel A RING lead.
6	SRINGACa	**RING AC Sense Input—Channel A.** Analog ac input to sense voltage on the channel A RING lead.
7	STIPACa	**TIP AC Sense Input—Channel A.** Analog ac input to sense voltage on the channel A TIP lead.
8	STIPDCa	**TIP DC Sense Input—Channel A.** Analog dc input to sense voltage on the channel A TIP lead.
9	CAPPa	**SLIC Stabilization Capacitor—Channel A.** Capacitor used in low pass filter.
10	CAPMa	**SLIC Stabilization Capacitor—Channel A.** Capacitor used in low pass filter.
11	SVBATa	**VBAT Sense—Channel A.** Input to sense voltage on V_{BAT}.

Pin #	Pin Name	Description
12	SVDC	**DC-DC Input Voltage Sensor.** Senses VDC input to dc-dc converters.
13	$\overline{\text{RST}}$	**Reset Input.** Active low input. Hardware reset used to place all control registers in the default state.
14	PSCLK	**ISI Clock Input.** Clock input for ISI bus timing.
15	MISO	**ISI Data Output.** Output data to ISI.
16	MOSI	**ISI Data Input.** Input data from ISI.
17	SDCHa	**DC Monitor—Channel A.** DC-DC converter monitor input used to detect overcurrent situations in the converter.
18	SDCLa	**DC Monitor—Channel A.** DC-DC converter monitor input used to detect overcurrent situations in the converter.
19	DCDRVa	**DC Drive—Channel A.** DC-DC converter control signal output which drives external transistor.
20	DCFFa	**DC Flexible Function—Channel A.** DC-DC controller flexible function I/O—channel A.
21	DCFFb	**DC Flexible Function—Channel B.** DC-DC controller flexible function I/O—channel B.
22	DCDRVb	**DC Drive—Channel B.** DC-DC converter control signal output which drives external transistor.
23	SDCLb	**DC Monitor—Channel B.** DC-DC converter monitor input used to detect overcurrent situations in the converter.
24	SDCHb	**DC Monitor—Channel B.** DC-DC converter monitor input used to detect overcurrent situations in the converter.
25	VDDD	**IC Voltage Supply.** Digital power supply for internal digital circuitry.
26	VDDREG	**Regulated Core Power Supply.**
27	SVBATb	**VBAT Sense—Channel B.** Input to sense voltage on V_{BAT}.
28	CAPMb	**SLIC Stabilization Capacitor—Channel B.** Capacitor used in low pass filter.
29	CAPPb	**SLIC Stabilization Capacitor—Channel B.** Capacitor used in low pass filter.
30	IREF	**Current Reference Input.** Connects to an external resistor used to provide a high accuracy reference current.
31	STIPDCb	**TIP DC Sense Input—Channel B.** Analog dc input to detect voltage on the channel B TIP lead.

Pin #	Pin Name	Description
32	STIPACb	**TIP AC Sense Input—Channel B.** Analog ac input to sense voltage on the channel B TIP lead.
33	SRINGACb	**RING AC Sense Input—Channel B.** Analog ac input to sense voltage on the channel B RING lead.
34	SRINGDCb	**RING DC Sense Input—Channel B.** Analog dc input to sense voltage on the channel B RING lead.
35	GPIO1b/STIPCb	**General Purpose I/O** or **TIP Coarse Sense Input—Channel B.** TIP channel A voltage sensing outside protection circuit.
36	GPIO2b/SRINGCb	**General Purpose I/O** or **RING Coarse Sense Input—Channel B.** RING channel A Voltage sensing outside protection circuit.
37	VDDA	**Analog Supply Voltage.** Analog power supply for internal analog circuitry.
38	N/C	**No Connect.** This pin should be left unconnected.
39	TIPb	**TIP Terminal—Channel B.** Connect to the TIP lead of the channel B subscriber loop.
40	N/C	**No Connect.** This pin should be left unconnected.
41	RINGb	**RING Terminal—Channel B.** Connect to the RING lead of the channel B subscriber loop.
42	N/C	**No Connect.** This pin should be left unconnected.
43	VBATb	**Battery Voltage Supply—Channel B.** Connect to battery supply for Channel B.
44	N/C	**No Connect.** This pin should be left unconnected.
45	VREF_BT	**Protection Reference Voltage.** Provides a reference trigger voltage for battery tracking protection.
46	N/C	**No Connect.**
47	VBATa	**Battery Voltage Supply—Channel A.** Connect to battery supply for Channel A.
48	N/C	**No Connect.** This pin should be left unconnected.
49	RINGa	**RING Terminal—Channel A.** Connect to the RING lead of the channel A subscriber loop.
50	N/C	**No Connect.** This pin should be left unconnected.
ep2	EPAD2	**Exposed paddle.** Connect to ground.
ep1	EPAD1	**Exposed paddle.** Connect to electrically-isolated low thermal impedance inner layer and/or backside thermal plane using multiple thermal vias.

7.2. Si32268/9 Pin Assignments



Pin #	Pin Name	Description
1	RINGa	**Ring Terminal—Channel A.** Connect to the RING lead of the channel A subscriber loop.
2	N/C	**No Connect.** This pin should be left unconnected.
3	TIPa	**TIP Terminal—Channel A.** Connect to the TIP lead of the channel A subscriber loop.
4	N/C	**No Connect.** This pin should be left unconnected.
5	GPIO2a/SRINGCa	**General Purpose I/O** or **RING Coarse Sense Input—Channel A.** RING channel A Voltage sensing outside protection circuit.
6	GPIO1a/STIPCa	**General Purpose I/O** or **TIP Coarse Sense Input—Channel A.** TIP channel A voltage sensing outside protection circuit.
7	SRINGDCa	**RING DC Sense Input—Channel A.** Analog dc input to sense voltage on the channel A RING lead.
8	SRINGACa	**RING AC Sense Input—Channel A**. Analog ac input to sense voltage on the channel A RING lead.
9	STIPACa	**TIP AC Sense Input—Channel A**. Analog ac input to sense voltage on the channel A TIP lead.
10	STIPDCa	**TIP DC Sense Input—Channel A**. Analog dc input to sense voltage on the channel A TIP lead.
11	CAPPa	**SLIC Stabilization Capacitor—Channel A.** Capacitor used in low pass filter.

Pin #	Pin Name	Description
12	CAPMa	**SLIC Stabilization Capacitor—Channel A.** Capacitor used in low pass filter.
13	SVBATa	**VBAT Sense—Channel A.** Input to sense voltage on V_{BAT}.
14	SVDC	**DC-DC Input Voltage Sensor**. Senses VDC input to dc-dc converters.
15	RSTB	**Reset Input.** Active low input. Hardware reset used to place all control registers in the default state.
16	PSCLK	**ISI Clock Input.** Clock input for ISI timing.
17	MISO	**ISI Data Output.** Output data to ISI.
18	MOSI	**ISI Data Input.** Input data from ISI.
19	DCFFa	**DC Flexible Function—Channel A.** DC-DC controller flexible function I/O—channel A.
20	DCFFb	**DC Flexible Function—Channel B.** DC-DC controller flexible function I/O—channel B.
21	DCDRVb	**DC Drive—Channel B.** DC-DC converter control signal output which drives external transistor.
22	SDCLb	**DC Monitor—Channel B.** DC-DC converter monitor input used to detect overcurrent situations in the converter.
23	SDCHb	**DC Monitor—Channel B.** DC-DC converter monitor input used to detect overcurrent situations in the converter.
24	VDDD	**IC Voltage Supply.** Digital power supply for internal digital circuitry.
25	VDDREG	**Regulated Core Power Supply.**
26	SVBATb	**VBAT Sense—Channel B.** Input to sense voltage on V_{BAT}.
27	CAPMb	**SLIC Stabilization Capacitor—Channel B.** Capacitor used in low pass filter.
28	CAPPb	**SLIC Stabilization Capacitor—Channel B.** Capacitor used in low pass filter.
29	IREF	**Current Reference Input.** Connects to an external resistor used to provide a high accuracy reference current.
30	STIPDCb	**TIP DC Sense Input—Channel B.** Analog dc input to detect voltage on the channel B TIP lead.
31	STIPACb	**TIP AC Sense Input—Channel B.** Analog ac input to sense voltage on the channel B TIP lead.
32	SRINGACb	**RING AC Sense Input—Channel B.** Analog ac input to sense voltage on the channel B RING lead.

Pin #	Pin Name	Description
33	SRINGDCb	**RING DC Sense Input—Channel B.** Analog dc input to sense voltage on the channel B RING lead.
34	GPIO1b / STIPCb	**General Purpose I/O** or **TIP Coarse Sense Input—Channel B.** TIP channel A voltage sensing outside protection circuit.
35	GPIO2b / SRI-NGCb	**General Purpose I/O** or **RING Coarse Sense Input—Channel B.** RING channel A Voltage sensing outside protection circuit.
36	VDDA	**Analog Supply Voltage.** Analog power supply for internal analog circuitry.
37	N/C	**No Connect.** This pin should be left unconnected.
38	TIPb	**TIP Terminal—Channel B.** Connect to the TIP lead of the channel B subscriber loop.
39	N/C	**No Connect.** This pin should be left unconnected.
40	RINGb	**RING Terminal—Channel B.** Connect to the RING lead of the channel B subscriber loop.
41	N/C	**No Connect.** This pin should be left unconnected.
42	VBATb	**Battery Voltage Supply—Channel B.** Connect to battery supply for Channel B.
43	N/C	**No Connect.** This pin should be left unconnected.
44	BASEb	**Offloading Base Control Output—Channel B.** Output to control base of power offloading transistor (fixed rail).
45	N/C	**No Connect.** This pin should be left unconnected.
46	BAT_PO	**Power Offloading Battery Voltage Input.** Output from fixed rail dc-dc converter.
47	BASEa	**Offloading Base Control Output—Channel A.** Output to control base of power offloading transistor (fixed rail).
48	N/C	**No Connect.** This pin should be left unconnected.
49	VBATa	**Battery Voltage Supply—Channel A.** Connect to battery supply for Channel A.
50	N/C	**No Connect.** This pin should be left unconnected.
ep2	EPAD2	**Exposed paddle.** Connect to ground.
ep1	EPAD1	**Exposed paddle.** Connect to electrically-isolated low thermal impedance inner layer and/or backside thermal plane using multiple thermal vias.

8. Ordering Guide

Table 19. Device Ordering Guide[1]

FXS P/N	Description	Package	Max V_{BAT}	Temperature
Si32266-C-FM1	Dual wideband FXS, integrated serial interface, tracking dc-dc	LGA[2]	–110 V	0 to 70 °C
Si32266-C-GM1	Dual wideband FXS, integrated serial interface, tracking dc-dc	LGA[2]	–110 V	–40 to 85 °C
Si32267-C-FM1	Dual wideband FXS, integrated serial interface, tracking dc-dc	LGA[2]	–140 V	0 to 70 °C
Si32267-C-GM1	Dual wideband FXS, integrated serial interface, tracking dc-dc	LGA[2]	–140 V	–40 to 85 °C
Si32268-C-FM1	Dual wideband FXS, integrated serial interface, shared dc-dc	LGA[2]	–110 V	0 to 70 °C
Si32268-C-GM1	Dual wideband FXS, integrated serial interface, shared dc-dc	LGA[2]	–110 V	–40 to 85 °C
Si32269-C-FM1	Dual wideband FXS, integrated serial interface, shared dc-dc	LGA[2]	–140 V	0 to 70 °C
Si32269-C-GM1	Dual wideband FXS, integrated serial interface, shared dc-dc	LGA[2]	–140 V	–40 to 85 °C
Si32266-C-FM	Dual wideband FXS, integrated serial interface, tracking dc-dc	NBA[3]	–110 V	0 to 70 °C
Si32266-C-GM	Dual wideband FXS, integrated serial interface, tracking dc-dc	NBA[3]	–110 V	–40 to 85 °C
Si32267-C-FM	Dual wideband FXS, integrated serial interface, tracking dc-dc	NBA[3]	–140 V	0 to 70 °C
Si32267-C-GM	Dual wideband FXS, integrated serial interface, tracking dc-dc	NBA[3]	–140 V	–40 to 85 °C
Si32268-C-FM	Dual wideband FXS, integrated serial interface, shared dc-dc	NBA[3]	–110 V	0 to 70 °C
Si32268-C-GM	Dual wideband FXS, integrated serial interface, shared dc-dc	NBA[3]	–110 V	–40 to 85 °C
Si32269-C-FM	Dual wideband FXS, integrated serial interface, shared dc-dc	NBA[3]	–140 V	0 to 70 °C
Si32269-C-GM	Dual wideband FXS, integrated serial interface, shared dc-dc	NBA[3]	–140 V	–40 to 85 °C

Notes:

1. Adding the suffix "R" to the part number (e.g. Si32268-C-FMR) denotes tape and reel.
2. LGA - Land Grid Array.
3. NBA - No Ball Array. Not recommended for new designs. This package option must be used only with high T_g PCB material (> 170 °C) when using Pb-free reflow profiles.

Table 20. Evaluation Kit Ordering Guide

Part Number	Supported ProSLIC	Description	V_{BAT} Max	Interface
Si32260PB20SL0-EVB	Si32260[1]	PMOS buck boost dc-dc converter EVB	–110 V	PCM/SPI to Voice Motherboard
Si32260TS20SL0-EVB	Si32260[2]	Tracking Shared Supply (TSS) dc-dc converter EVB	–100 V	PCM/SPI to Voice Motherboard
Si32260QC20SL0-EVB	Si32260[1]	Low cost quasi-Ćuk (MOSFET/ Inductor based) full tracking dc-dc converter EVB	–80 V	PCM/SPI to Voice Motherboard
Si32261FBMB0-EVB	Si32260, Si32261[1]	Flyback (transformer based) full tracking dc-dc converter EVB	–140 V	PCM/SPI to Voice Motherboard
Si32261QC20SL0-EVB	Si32260, Si32261[1]	Quasi-Ćuk (MOSFET/Inductor based) full tracking dc-dc converter EVB	–140 V	PCM/SPI to Voice Motherboard
Si32266PB20SL0-EVB	Si32266	ISI PMOS buck boost dc-dc converter EVB	–110 V	ISI to SoC with ISI
Si32268TS20SL1-EVB	Si32268	Fully isolated ISI Tracking Shared Supply (TSS) dc-dc converter EVB	–100 V	ISI to SoC with ISI

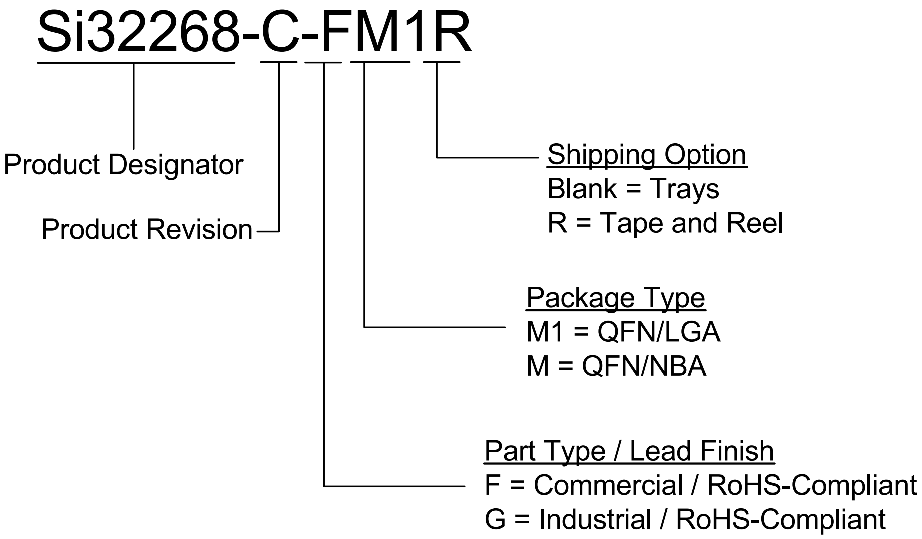
Notes:

1. Can also be used for software development for Si32266 and Si32267 (only the SoC physical interface is different).
2. Can also be used for software development for Si32268 and Si32269 (only the SoC physical interface is different).

9. Product Identification

The product identification number is a finished goods part number or is specified by a finished goods part number, such as a special customer part number.

Example:



10. Package Outlines

10.1. 50-Pin QFN/LGA

Figure 24 illustrates the package details for the Si32266/7/8/9 50-Pin QFN/LGA. Table 22 lists the values for the dimensions shown in the illustration.

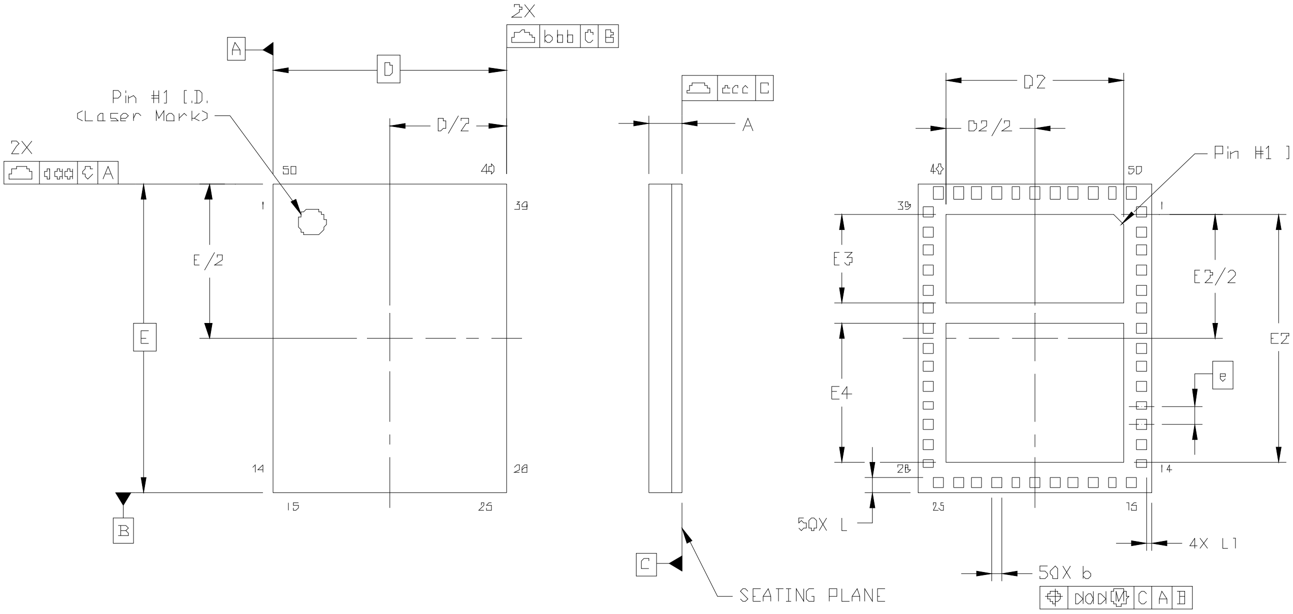


Figure 24. 50-Pin (QFN/LGA Package)

Table 21. 50-Pin QFN/LGA Package Diagram Dimensions

Dimension	Min	Nom	Max	Dimension	Min	Nom	Max
A	0.74	0.84	0.94	E4	3.55	3.60	3.65
b	0.20	0.25	0.30	L	0.35	0.40	0.45
D	6.00 BSC.			L1	0.05	0.10	0.15
D2	4.55	4.60	4.65	aaa	—	—	0.15
e	0.50 BSC.			bbb	—	—	0.15
E	8.00 BSC.			ccc	—	—	0.10
E2	6.35	6.40	6.45	ddd	—	—	0.10
E3	2.25	2.30	2.35				

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10.2. 50-Pin QFN/NBA

Figure 25 illustrates the package details for the Si32266/7/8/9 50-Pin QFN/NBA. Table 22 lists the values for the dimensions shown in the illustration.

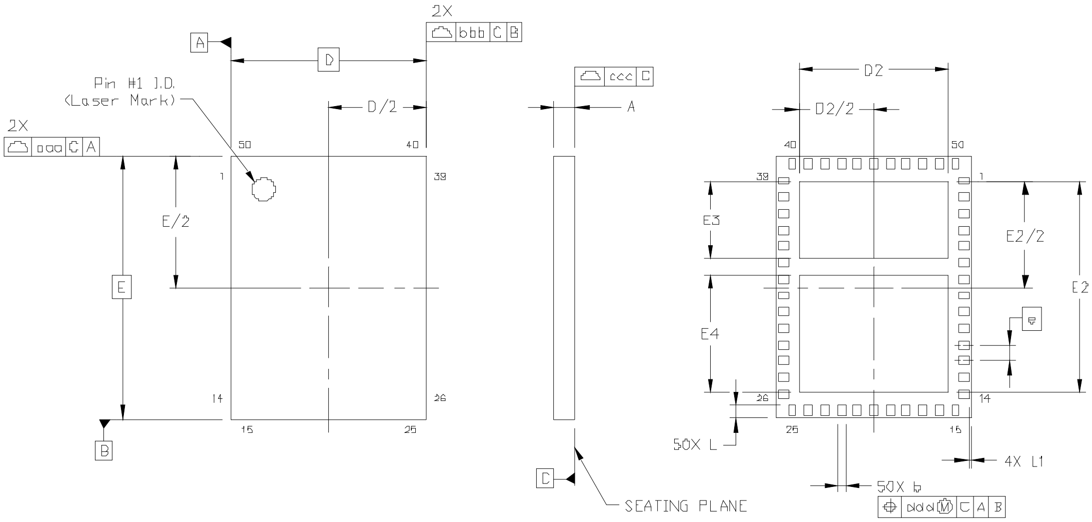


Figure 25. 50-Pin (QFN/NBA Package)

Table 22. 50-Pin QFN/NBA Package Diagram Dimensions

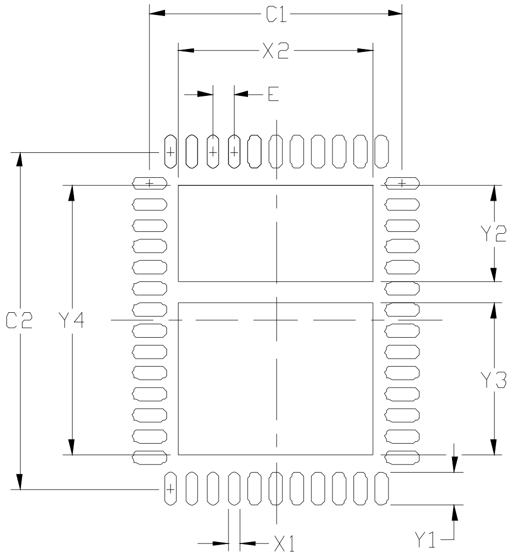
Dimension	Min	Nom	Max	Dimension	Min	Nom	Max
A	0.60	0.65	0.70	E4	3.55	3.60	3.65
b	0.20	0.25	0.30	L	0.35	0.40	0.45
D	6.00 BSC.			L1	0.05	0.10	0.15
D2	4.55	4.60	4.65	aaa	—	—	0.15
e	0.50 BSC.			bbb	—	—	0.15
E	8.00 BSC.			ccc	—	—	0.10
E2	6.35	6.40	6.45	ddd	—	—	0.10
E3	2.25	2.30	2.35				

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

11. PCB Land Pattern: LGA and NBA Packages

11.1. Land Pattern and Solder Mask Design



Dimension	mm
C1	6.00
C2	8.00
E	0.50
X1	0.30
X2	4.60
Y1	0.80
Y2	2.30
Y3	3.60
Y4	6.40

Notes:

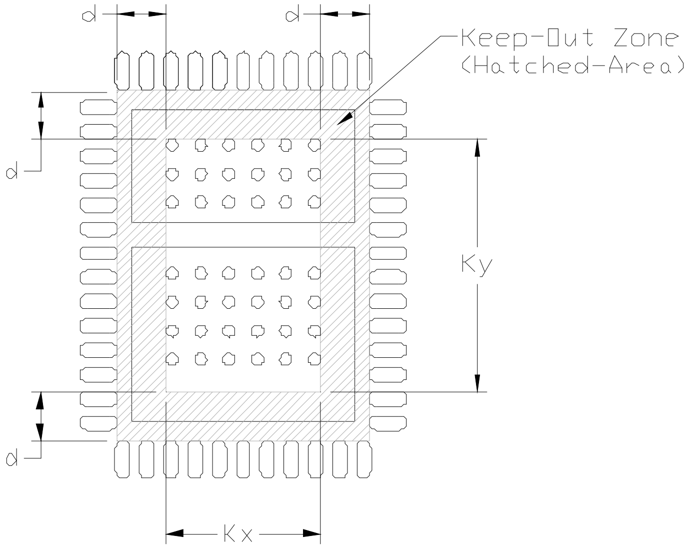
General

1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

11.2. Thermal Via Layout

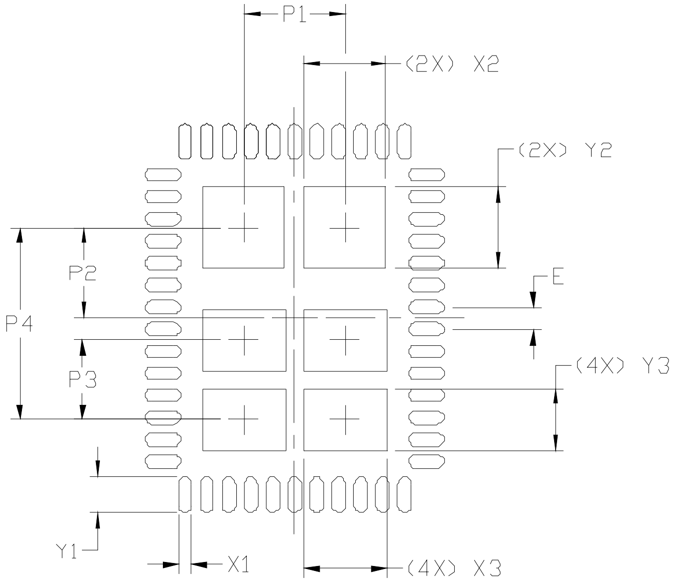


Dimension	Min	Max
d	1.00	—
Kx	—	3.2
Ky	—	5.2

Notes:

1. High-T_g PCB materials ($T_g \geq 170$ °C) are recommended for Pb-Free reflow profiles, per standard industry practice. This is required for reliable board assembly when using the NBA package.
2. The customer's PCB design must provide sufficient thermal dissipation for high power operation of the device. See layout guidelines in Applications Note AN381 for further details.
3. A minimum of eight thermal vias are required in each center pad. The recommended via diameter is 0.20 - 0.30 mm (8 - 12 mils).
4. Thermal vias placed in the center pads **must have** a minimum spacing of 1.0 mm from the edge of the via to the closest pin pad metal (d ≥ 1.0 mm).
5. Vias may be placed as desired within the non-hatched area of the center pads.
6. Vias placed within the center pad areas **must be** either filled or tented on the top side of the board to prevent solder thieving from under the device.

11.3. Stencil Aperture Design



Dimension	mm
E	0.50
P1	2.30
P2	2.05
P3	1.80
P4	4.35
X1	0.30
X2	1.85
X3	1.90
Y1	0.80
Y2	1.85
Y3	1.40

Notes:

Stencil Design

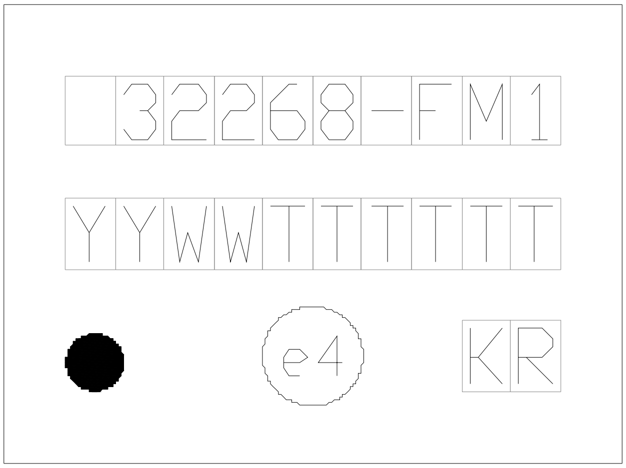
1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).

Card Assembly

3. A No-Clean, Type-3 solder paste is recommended.
4. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
5. Reflow profile measured at device should be ≥ 245 °C for 20s minimum.

12. Top Markings

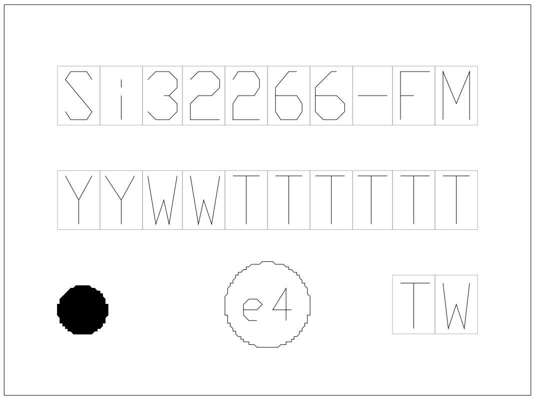
12.1. 50-Pin LGA Top Marking



12.2. 50-Pin LGA Top Marking Explanation

Mark Method:	Laser	
Font Size:	2.0 Point (2.8 mils) Right-Justified	
Line 1 Marking:	Device Part Number	Si32268-FM1
Line 2 Marking:	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the assembly release.
	TTTTTT = Mfg Code	Manufacturing Code from the Assembly Purchase Order form.
Line 3 Marking:	Circle = 0.75 mm Diameter Lower Left-Justified	Pin 1 Identifier
	Circle = 1.3 mm Diameter Center-Justified	“e4” Pb-Free Symbol
	Country of Origin ISO Code Abbreviation	KR

12.3. 50-Pin NBA Top Marking



12.4. 50-Pin NBA Top Marking Explanation

Mark Method:	Laser	
Font Size:	2.0 Point (2.8 mils) Right-Justified	
Line 1 Marking:	Device Part Number	Si32266-FM
Line 2 Marking:	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the assembly release.
	TTTTTT = Mfg Code	Manufacturing Code from the Assembly Purchase Order form.
Line 3 Marking:	Circle = 0.75 mm Diameter Lower Left-Justified	Pin 1 Identifier
	Circle = 1.3 mm Diameter Center-Justified	“e4” Pb-Free Symbol
	Country of Origin ISO Code Abbreviation	TW

NOTES:

DOCUMENT CHANGE LIST:

Revision 0.3 to Revision 1.0

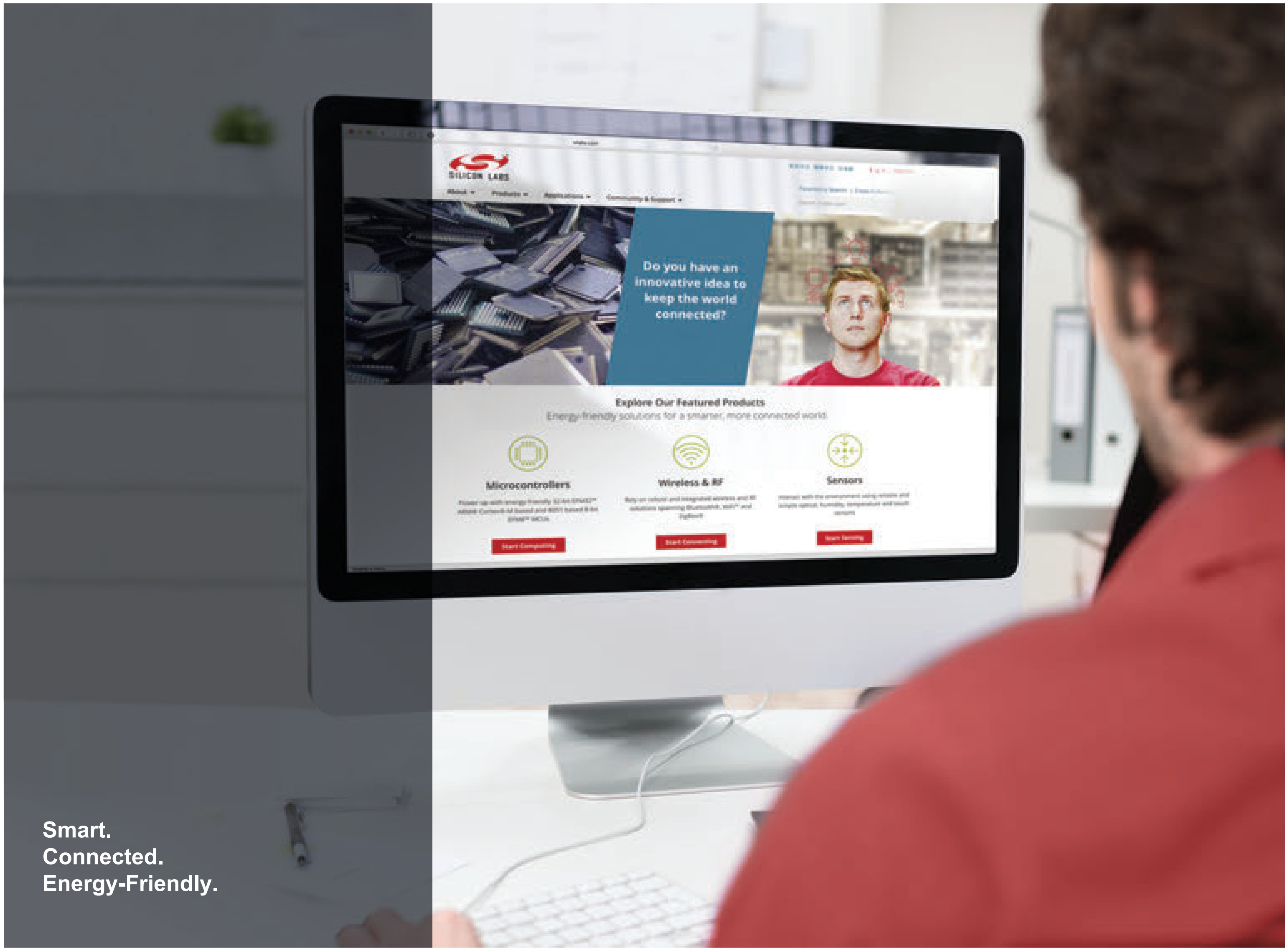
- Added Thermal resistance and continuous power dissipation values.
- Updated the protection schematics for the TSS dc-dc converter application. Pins "A" of the TISP61089BDR are now connected to GROUND, and the pin labeled "G" (the GATE) is now connected to VBAT.
- Updated order of data sheet elements in accordance with new style guide SOPs.
- Cosmetic updates to schematics and BOMs
- Changed test load impedance to 2.2 kΩ (was listed as 5.3 kΩ or 600 Ω).
- Added $\overline{\text{RST}}$ leakage current specs.
- Increased absolute maximum VBAT, TIP, and RING voltages to –142 V (was –140 V).
- Added absolute maximum positive voltage specs for TIP and RING of +0.4 V.

Revision 1.0 to Revision 1.1

- Added LGA package information.

Revision 1.1 to Revision 1.2

- Added ISI and removed PCM/SPI interfaces from feature list.
- Corrected block diagram to remove PCLK
- Corrected title of Figure 2 to be "ISI timing diagram" (not SPI)
- Added ISI boards to EVB ordering guide
- Added note that NBA packages are not recommended for new designs



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