PRIORITY

# QSE™ WAC-488-A

# ATM Quad Switch Element

****Patents Pending****

## DESCRIPTION

The WAC-488-A Quad Switch Element (QSE™) is an advanced communications device that enables the implementation of high performance switching systems. The QSE is a 5 Gbps switch element, combinations of which allow switch fabric implementations that span from 5 Gbps to 320 Gbps. The QSE is a 3.3 V CMOS device that provides a 32 × 32 interconnect. This interconnect is compatible with other QSEs, the IgT WAC-487 ATM Quad Routing Table (QRT™), and the IgT ATM Routing Table (WAC-187) and ATM Switch Element (WAC-188) devices.

The QSE supports both point-to-point (unicast) and point-to-multipoint (multicast) traffic. A switch fabric constructed with QSEs is memoryless for unicast traffic and contains internal cell buffers for multicast traffic.

Unicast traffic is routed in a circuit-switched, cut-through manner. The QSEs send a directed acknowledgment congestion indication (ACK/NACK) feedback signal to the source of the data, thus informing the source if the data successfully propagated through the switch fabric. If the data did not make it through the switch fabric, a Negative Acknowledgment (NACK) signal informs the source where the data was blocked. The switch fabric is designed to run faster than the line data rate (speed-up factor), so the source has time to retransmit cells blocked in previous trials. The speed-up factor, along with IgT's patented randomization algorithm (Evil Twin Switching™), ensure a lower bound on the performance of the switch. Thus, if a multi-stage Clos- or Reverse Delta-type network is constructed from QSE devices, the first one or two switches in the fabric can arbitrarily route unicast data from the inputs to the outputs of the QSEs, thus allowing for cells blocked in the switch fabric on a particular trial to be rerouted so blocking on the following trial is minimized. The remaining QSEs examine a routing tag to determine the destination of the cell.

Multicast traffic is routed in a store-and-forward manner, and cells are replicated in an optimal tree-like fashion. A multipriority backpressure feedback is used to control the flow of multicast cells through the fabric.

All 32 switch fabric input ports contain on-board, clock recovery circuitry. These phase aligners alleviate the need for external phase synchronization circuitry and allow QRT and QSE devices to be physically far apart from each other.

IgT also offers the QSE Device Control Package (WAC-488-DCP) for the QSE device, which is a software package that harnesses the QSE's rich feature set and shortens system development times.

## FEATURES

### Switching Algorithm

- Supports blocking resolution in the switch fabric.
- Guarantees a lower bound on switch performance using a patented randomization algorithm called Evil Twin Switching.
- Determines routes using specified bits in the header (self-routing switch fabric) for unicast traffic.
- Determines output groupings using a lookup table for multicast traffic.

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IgT®
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- Allows output ports to be combined in groups of 1, 2, 4, 8, 16, or 32 for unicast traffic.
- Allows output ports to be combined in groups of 1, 2, or 4 for multicast traffic.

### Multicast Support

- Supports optimal tree-based multicast replication in the switch fabric.
- Supports 128 internal multicast groups, expandable to 32K with external SRAM.
- Provides 64 internal cell buffers for multicast cells.

### Diagnostic/Robustness Features

- Checks the header parity.
- Counts tagged cells.
- Checks for connectivity and stuck-at faults on all switch fabric interconnects.

### I/O Features

- Provides 32 switch fabric interfaces with integrated phase aligner clock recovery circuitry.
- Provides a Start-Of-Cell (SOC) output per four switch element interfaces.
- Provides an external 8-bit Synchronous SRAM (SSRAM) interface for multicast group expansion.
- Provides a demultiplexed address/data CPU interface.
- Provides an IEEE 1149.1 (JTAG) boundary scan test bus.

### Physical Characteristics

- 3.3 V supply voltage.
- 5 V tolerant inputs.
- 596-pin Enhanced Plastic Ball Grid Array (EPBGA) package.
- Operates from a single 66 MHz clock.

Figure 1 shows a QSE system block diagram.

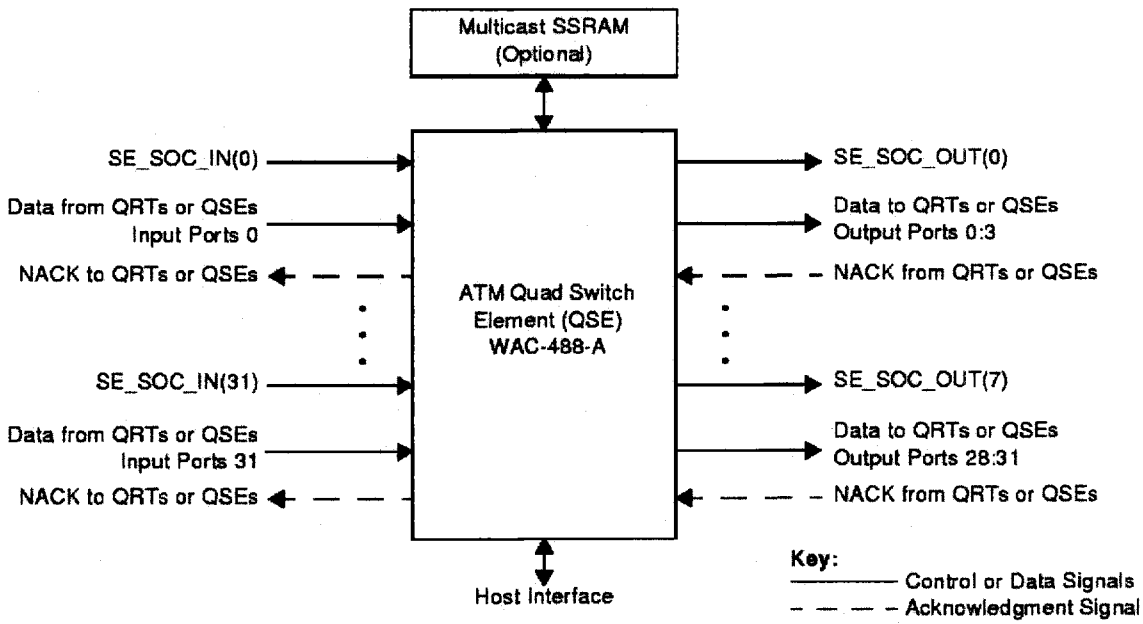


**Figure 1. QSE Interface Block Diagram**