

# DRAM Single-In-Line Memory Module (SIMM)

## 4, 8, 16, and 32 Megabyte

- JEDEC—Standard 72-Lead Single-In-Line Memory Module (SIMM)
- Single 5 V Power Supply, TTL-Compatible Inputs and Outputs
- Extended Data Out (EDO)
- RAS—Only Refresh, CAS before RAS Refresh, Hidden Refresh
- 4MB/8MB: 1024 Cycle Refresh: 16 ms
- 16MB/32MB: 2048 Cycle Refresh: 32 ms

### PART NUMBERS (See Page 23 for Definitions)

Organization	60	70
1M x 32	MB321BJ08TASN60 MB321BJ08TASG60 MB321BT08TASN60 MB321BT08TASG60	MB321BJ08TASN70 MB321BJ08TASG70 MB321BT08TASN70 MB321BT08TASG70
2M x 32	MB322BJ08TASN60 MB322BJ08TASG60 MB322BT08TASN60 MB322BT08TASG60	MB322BJ08TASN70 MB322BJ08TASG70 MB322BT08TASN70 MB322BT08TASG70
4M x 32	MB324CJ00TBSN60 MB324CJ00TBSG60 MB324CT00TBSN60 MB324CT00TBSG60	MB324CJ00TBSN70 MB324CJ00TBSG70 MB324CT00TBSN70 MB324CT00TBSG70
8M x 32	MB328CJ00TBSN60 MB328CJ00TBSG60 MB328CT00TBSN60 MB328CT00TBSG60	MB328CJ00TBSN70 MB328CJ00TBSG70 MB328CT00TBSN70 MB328CT00TBSG70

### KEY TIMING PARAMETERS

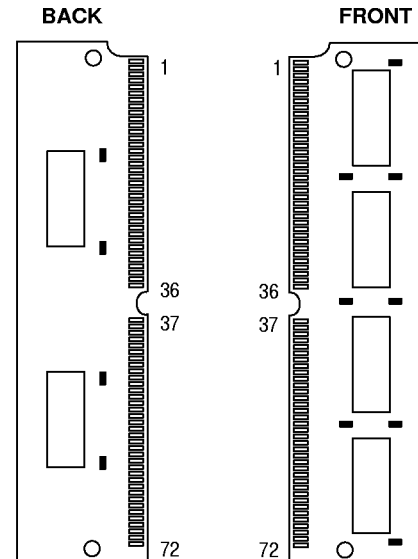
Speed	t <sub>RC</sub> (ns)	t <sub>RAC</sub> (ns)	t <sub>CAC</sub> (ns)	t <sub>AA</sub> (ns)	t <sub>EPC</sub> (ns)
60	104	60	17	30	25
70	124	70	20	35	30

### ADDITIONAL PARAMETERS

Configuration	Speed	Active Power Dissipation (mW) (Max)	Standby Power Dissipation	
			TTL	CMOS
4MB	60	2,035	22	11
	70	1,705		
8MB	60	2,057	44	22
	70	1,727		
16MB	60	4,840	88	44
	70	4,180		
32MB	60	4,928	176	88
	70	4,268		

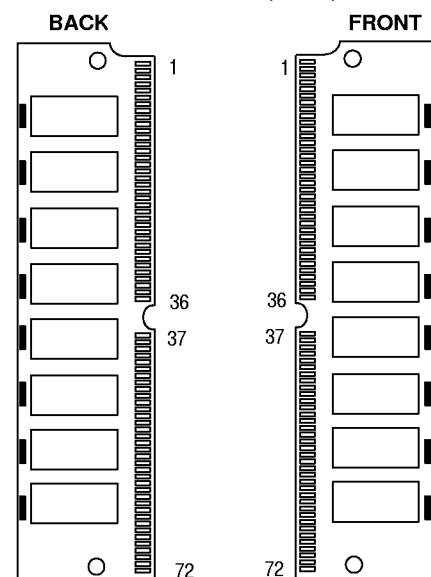
**1, 2, 4, 8M x 32**  
5 V, EDO, Unbuffered

1M x 32 (4MB), 2M x 32 (8MB)  
72-LEAD LOW HEIGHT SIMM



Organization	Comp. Pkg.	Case	Components	
			Front	Back
1M x 32 (4MB)	TSOP	866H-01	2	0
	SOJ	866A-02	2	0
2M x 32 (8MB)	TSOP	866H-01	4	0
	SOJ	866A-02	2	2

4M x 32 (16MB), 8M x 32 (32MB)  
72-LEAD LOW HEIGHT SIMM  
CASE 866-02 (SOJ),  
CASE 866H-01 (TSOP)



BACK NOT POPULATED ON 4M x 32 (16MB)

**PIN ASSIGNMENTS**

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V <sub>SS</sub>	13	A1	25	DQ22	37	NC	49	DQ8	61	DQ13
2	DQ0	14	A2	26	DQ7	38	NC	50	DQ24	62	DQ30
3	DQ16	15	A3	27	DQ23	39	V <sub>SS</sub>	51	DQ9	63	DQ14
4	DQ1	16	A4	28	A7	40	CAS0	52	DQ25	64	DQ31
5	DQ17	17	A5	29	NC	41	CAS2	53	DQ10	65	DQ15
6	DQ2	18	A6	30	V <sub>CC</sub>	42	CAS3	54	DQ26	66	NC
7	DQ18	19	A10*	31	A8	43	CAS1	55	DQ11	67	PD1
8	DQ3	20	DQ4	32	A9	44	RAS0	56	DQ27	68	PD2
9	DQ19	21	DQ20	33	RAS3*	45	RAS1*	57	DQ12	69	PD3
10	V <sub>CC</sub>	22	DQ5	34	RAS2	46	NC	58	DQ28	70	PD4
11	NC	23	DQ21	35	NC	47	W	59	V <sub>CC</sub>	71	NC
12	A0	24	DQ6	36	NC	48	NC	60	DQ29	72	V <sub>SS</sub>

\* A10 is NC on the 4MB and 8MB. RAS1 and RAS3 are NC on the 4MB and 16MB.

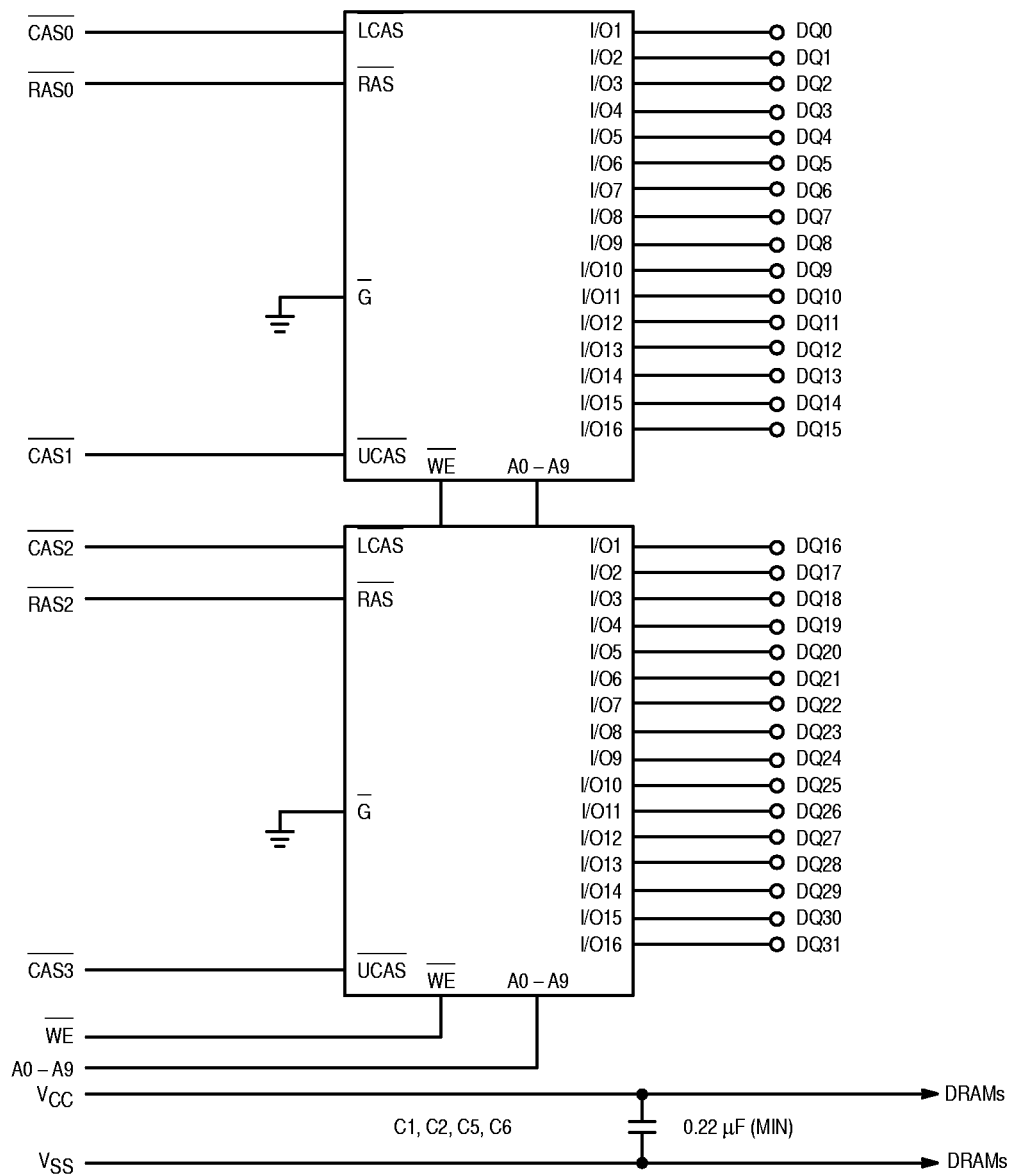
PIN NAMES	
A0 – A10	Address Inputs
CAS0 – CAS3	Column Address Strobe
RAS0 – RAS3	Row Address Strobe
V <sub>CC</sub>	Power
NC	No Connection
DQ0 – DQ31	Data Input/Output
PD1 – PD4	Presence Detect
W	Write Enable
V <sub>SS</sub>	Ground

All power supply and ground pins must be connected for proper operation of the device.

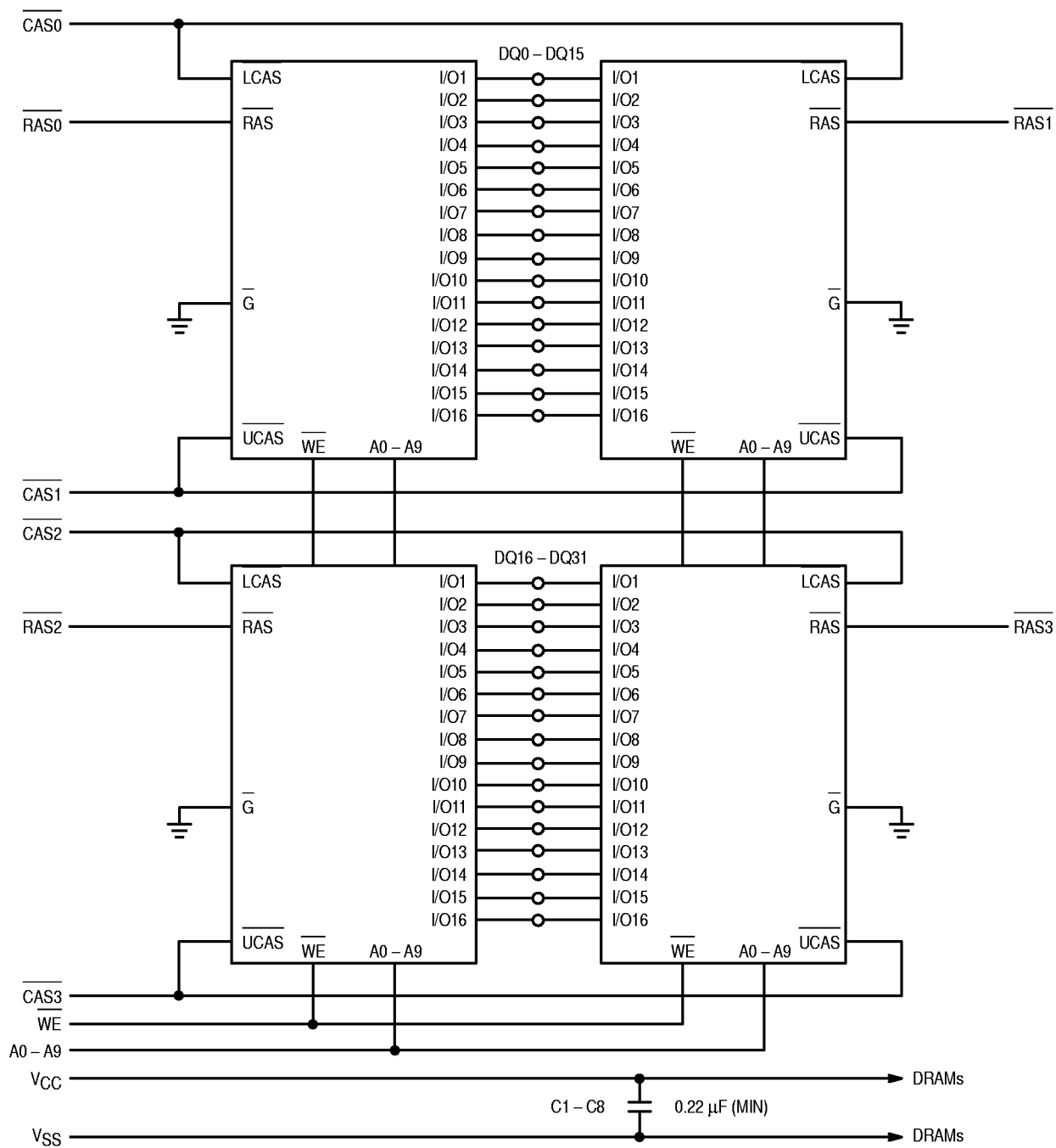
**PRESENCE DETECT**

Pin Names	Speed	4MB	8MB	16MB	32MB
PD1		V <sub>SS</sub>	NC	V <sub>SS</sub>	NC
PD2		V <sub>SS</sub>	NC	NC	V <sub>SS</sub>
PD3	60	NC	NC	NC	NC
	70	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>
PD4	60	NC	NC	NC	NC
	70	NC	NC	NC	NC

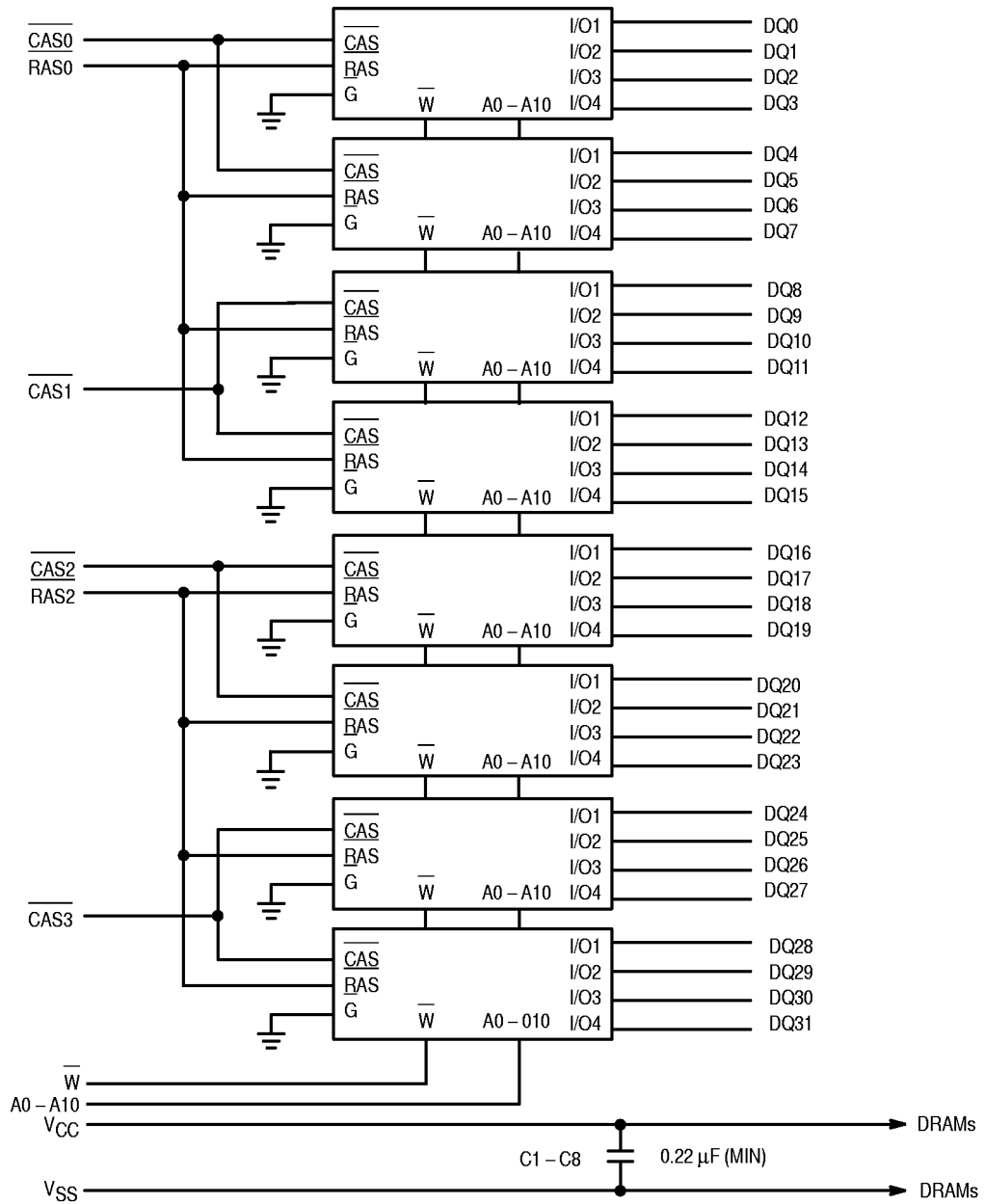
4MB BLOCK DIAGRAM



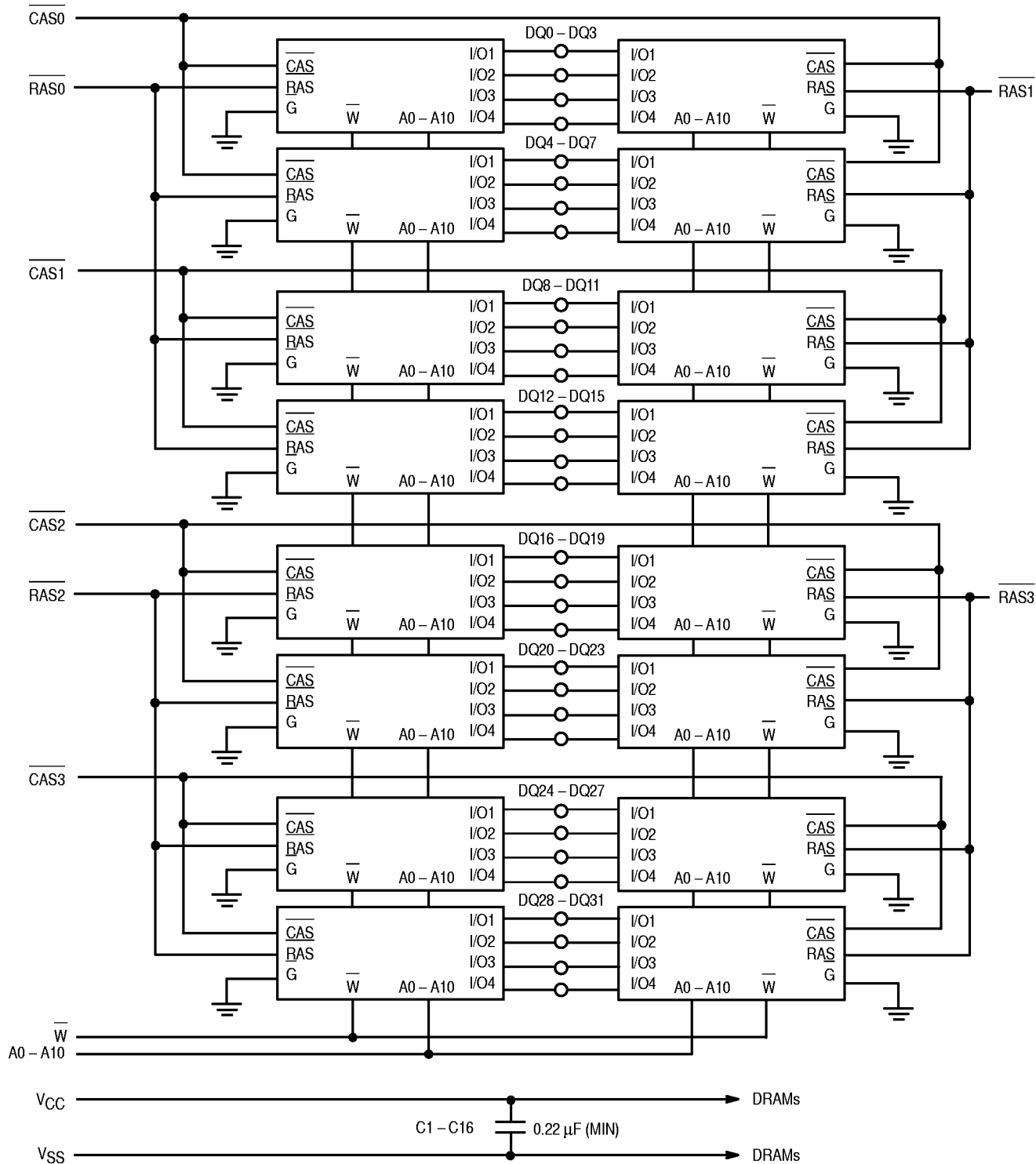
8MB BLOCK DIAGRAM



16MB BLOCK DIAGRAM



32MB BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS** (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC}$	-0.5 to +7	V
Voltage Relative to $V_{SS}$ (for Any Pin Except $V_{CC}$ )	$V_{in}, V_{out}$	-0.5 to $V_{CC} + 0.5$	V
Data Output Current per DQ pin	$I_{out}$	50	mA
Power Dissipation	$P_D$	4MB/8MB 16MB/32MB	W
Operating Temperature Range	$T_A$	0 to +70	°C
Storage Temperature Range	$T_{stg}$	-55 to +125	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

**DC OPERATING CONDITIONS AND CHARACTERISTICS**

( $V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $T_A = 0$  to  $70^\circ\text{C}$ , Unless Otherwise Noted)

**RECOMMENDED OPERATING CONDITIONS** (All Voltages Referenced to  $V_{SS}$ )

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	$V_{CC}$	4.5	5.0	5.5	V
	$V_{SS}$	0	0	0	
Logic High Voltage, All Inputs	$V_{IH}$	2.4	—	$V_{CC} + 0.5$	V
Logic Low Voltage, All Inputs	$V_{IL}$	-0.5*	—	0.8	V
Input Leakage Current ( $V_{SS} \leq V_{in} \leq V_{CC}$ )	$I_{lkg(i)}$	-160	—	+160	$\mu\text{A}$
Output Leakage Current (CAS at Logic 1, $V_{SS} \leq V_{in} \leq V_{CC}$ )	$I_{lkg(o)}$	-20	—	+20	$\mu\text{A}$
Output High Voltage ( $I_{OH} = -2 \text{ mA}$ )	$V_{OH}$	2.4	—	—	V
Output High Voltage ( $I_{OL} = 2 \text{ mA}$ )	$V_{OL}$	—	—	0.4	V

\* 2.0 V at pulse width  $\leq 20 \text{ ns}$ .

**DC CHARACTERISTICS AND SUPPLY CURRENTS** (All voltages Referenced to  $V_{SS}$ )

Characteristic	Symbol	4MB		8MB		16MB		32MB		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$V_{CC}$ Power Supply Current ( $t_{RC} = t_{RC \text{ Min}}$ )	$I_{CC1}$	—	370	—	374	—	880	—	896	mA	1, 2
$V_{CC}$ Power Supply Current (Standby) ( $RAS = CAS = V_{IH}$ )	$I_{CC2}$	—	4	—	8	—	16	—	32	mA	
$V_{CC}$ Power Supply Current During RAS only Refresh Cycles ( $t_{RC} = t_{RC \text{ Min}}$ )	$I_{CC3}$	—	370	—	374	—	880	—	896	mA	1, 2
$V_{CC}$ Power Supply Current During EDO Cycle ( $t_{EPC} = t_{EPC \text{ Min}}$ )	$I_{CC4}$	—	240	—	244	—	760	—	776	mA	1, 2
$V_{CC}$ Power Supply Current (Standby) ( $RAS = CAS = V_{CC} - 0.2 \text{ V}$ )	$I_{CC5}$	—	2	—	4	—	8	—	16	mA	
$V_{CC}$ Power Supply Current During CAS Before RAS Refresh Cycle ( $t_{RC} = t_{RC \text{ Min}}$ )	$I_{CC6}$	—	370	—	374	—	880	—	896	mA	1

## NOTES:

- Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
- Column Address can be changed once or less while  $RAS = V_{IL}$  and  $CAS = V_{IH}$ .

**CAPACITANCE** ( $f = 1.0 \text{ MHz}$ ,  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5 \text{ V}$ , Periodically Sampled Rather Than 100% Tested)

Input Capacitance	Symbol	4MB Max	8MB Max	16MB Max	32MB Max	Unit
Addresses	$C_{in}$	20	30	50	90	pF
WE	$C_{in}$	24	38	66	122	pF
RAS	$C_{in}$	17	17	38	38	pF
CAS	$C_{in}$	17	24	24	38	pF
DQ	$C_{out}$	17	24	17	24	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation:  $C = I \Delta t / \Delta V$ .

## AC OPERATING CONDITIONS AND CHARACTERISTICS

( $V_{CC} = 5 \text{ V} \pm 10\%$ ,  $T_A = 0 \text{ to } 70^\circ\text{C}$ , Unless Otherwise Noted)

**ALL DEVICES: READ, WRITE, AND READ-WRITE CYCLES** (See Notes 1, 2, 3, and 4)

Parameter	Symbol		60		70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Random Read or Write Cycle Time	$t_{RELREL}$	$t_{RC}$	104	—	124	—	ns	5
Access Time from RAS	$t_{RELQV}$	$t_{RAC}$	—	60	—	70	ns	6, 7, 11, 12
Access Time from CAS	$t_{CELQV}$	$t_{CAC}$	—	17	—	20	ns	6, 8, 11
Access Time from Column Address	$t_{AVQV}$	$t_{AA}$	—	30	—	35	ns	6, 9, 12
Access Time from Precharge CAS	$t_{CEHQV}$	$t_{CPA}$	—	35	—	40	ns	6
CAS to Output in Low-Z	$t_{CELQX}$	$t_{CLZ}$	0	—	0	—	ns	
Output Buffer and Turn-Off Delay	$t_{CEHQZ}$	$t_{OFF}$	0	15	0	15	ns	10, 16
Transition Time (Rise and Fall)	$t_T$	$t_T$	1	50	1	50	ns	1
RAS Precharge Time	$t_{REHREL}$	$t_{RP}$	40	—	50	—	ns	
RAS Pulse Width	$t_{RELREH}$	$t_{RAS}$	60	10 k	70	10 k	ns	
RAS Hold Time	$t_{CELREH}$	$t_{RSH}$	10	—	12	—	ns	
CAS Hold Time	$t_{RELCEH}$	$t_{CSH}$	40	—	50	—	ns	
CAS Pulse Width	$t_{CELCEH}$	$t_{CAS}$	10	10 k	12	10 k	ns	
RAS to CAS Delay Time	$t_{RELCEL}$	$t_{RCD}$	14	43	14	50	ns	11
RAS to Column Address Delay Time	$t_{RELAV}$	$t_{RAD}$	12	30	12	35	ns	12

NOTES:

(continued)

- $V_{IH}$  (min) and  $V_{IL}$  (max) are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
- An initial pause of 200  $\mu\text{s}$  is required after power-up followed by 8 RAS cycles before proper device operation is guaranteed. If using the internal refresh counter, a minimum of 8 CAS before RAS refresh cycles, instead of 8 RAS only refresh cycles are required.
- The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ) in a monotonic manner.
- AC measurements  $t_T = 5.0 \text{ ns}$ .
- The specification for  $t_{RC}$  (min),  $t_{RWC}$  (min), and  $t_{EPC}$  (min) is used only to indicate cycle time at which proper operation over the full temperature range ( $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ ) is ensured.
- Measured with a current load equivalent to 2 TTL ( $-200 \mu\text{A}$ ,  $+4 \text{ mA}$ ) loads and 100 pF with the data output trip points set at  $V_{OH} = 2.0 \text{ V}$  and  $V_{OL} = 0.8 \text{ V}$ .
- Assumes that  $t_{RCD} \leq t_{RCD} \text{ (max)}$ .
- Assumes that  $t_{RCD} \geq t_{RCD} \text{ (max)}$ .
- Assumes that  $t_{RAD} \geq t_{RAD} \text{ (max)}$ .
- $t_{OFF}$  (max),  $t_{REZ}$  (max), and  $t_{WEZ}$  (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- Operation within the  $t_{RCD}$  (max) limit ensures that  $t_{RAC}$  (max) can be met.  $t_{RCD}$  (max) is specified as a reference point only; if  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (max) limit, then access time is controlled exclusively by  $t_{CAC}$ .
- Operation within the  $t_{RAD}$  (max) limit ensures that  $t_{RAC}$  (max) can be met.  $t_{RAD}$  (max) is specified as a reference point only; if  $t_{RAD}$  is greater than the specified  $t_{RAD}$  (max), then access time is controlled exclusively by  $t_{AA}$ .

## ALL DEVICES: READ, WRITE, AND READ–WRITE CYCLES (continued)

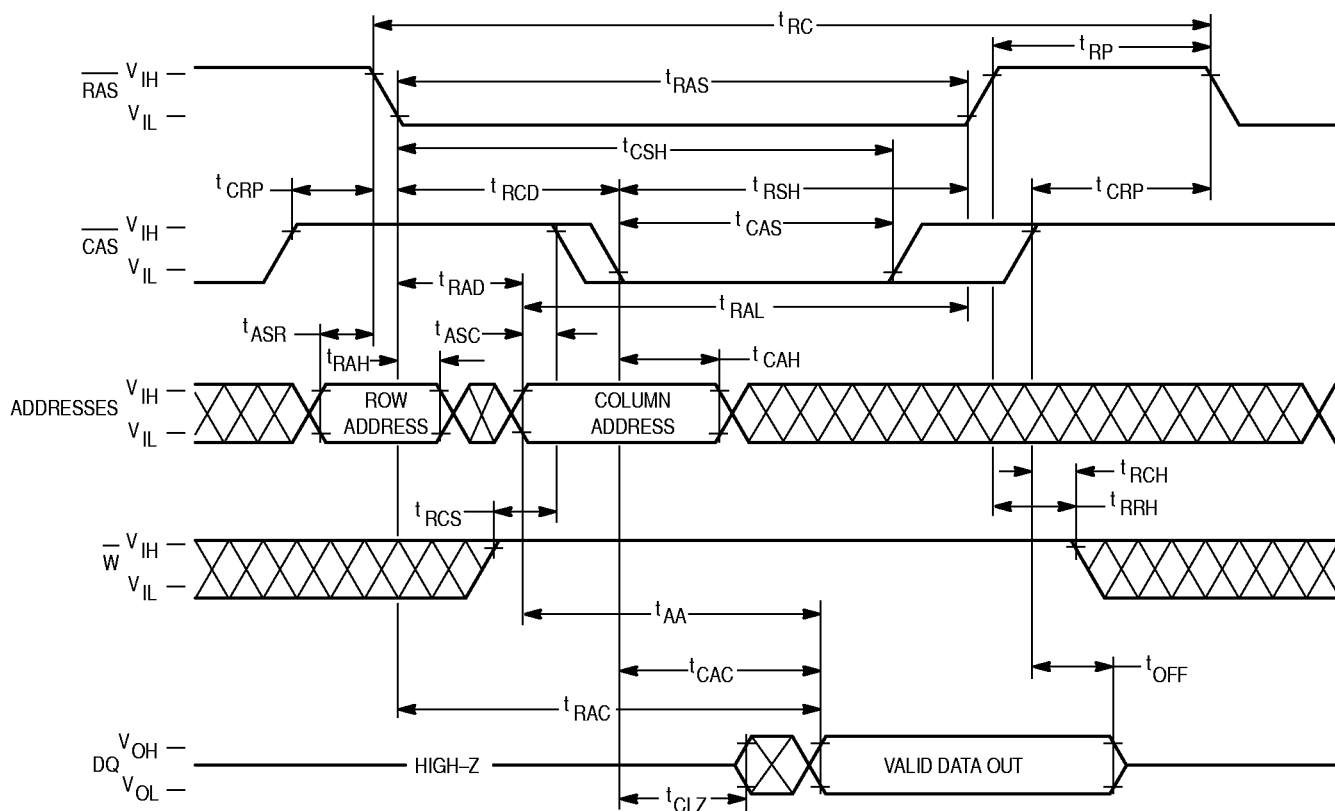
Parameter	Symbol		60		70		Unit	Notes	
	Std	Alt	Min	Max	Min	Max			
CAS to RAS Precharge Time	t <sub>CEHREL</sub>	t <sub>CRP</sub>	5	—	5	—	ns		
CAS Precharge Time	t <sub>CEHCEL</sub>	t <sub>CP</sub>	10	—	12	—	ns		
Row Address Setup Time	t <sub>AVREL</sub>	t <sub>ASR</sub>	0	—	0	—	ns		
Row Address Hold Time	t <sub>RELAX</sub>	t <sub>RAH</sub>	10	—	10	—	ns		
Column Address Setup Time	t <sub>AVCEL</sub>	t <sub>ASC</sub>	0	—	0	—	ns		
Column Address Hold Time	t <sub>CELAX</sub>	t <sub>CAH</sub>	10	—	12	—	ns		
Column Address to RAS Lead Time	t <sub>AVREH</sub>	t <sub>RAL</sub>	30	—	35	—	ns		
Read Command Setup Time	t <sub>WHCEL</sub>	t <sub>RCS</sub>	0	—	0	—	ns		
Read Command Hold Time Referenced to CAS	t <sub>CEHWX</sub>	t <sub>RCH</sub>	0	—	0	—	ns	13	
Read Command Hold Time Referenced to RAS	t <sub>REHWX</sub>	t <sub>RRH</sub>	0	—	0	—	ns	13	
Write Command Hold Time Referenced to CAS	t <sub>CELWH</sub>	t <sub>WCH</sub>	10	—	12	—	ns		
Write Command Pulse Width	t <sub>WLWH</sub>	t <sub>WP</sub>	10	—	12	—	ns		
Write Command to RAS Lead Time	t <sub>WLREH</sub>	t <sub>RWL</sub>	10	—	12	—	ns		
Write Command to CAS Lead Time	t <sub>WLCEH</sub>	t <sub>CWL</sub>	10	—	12	—	ns		
Data In Setup Time	t <sub>DVCEL</sub>	t <sub>DS</sub>	0	—	0	—	ns	14	
Data In Hold Time	t <sub>CELDX</sub>	t <sub>DH</sub>	10	—	12	—	ns	14	
Refresh Period	4MB, 8MB 16MB, 32MB	t <sub>RVRV</sub>	t <sub>RFSH</sub>	—	16 32	—	16 32	ms	
Write Command Setup Time	t <sub>WLCEL</sub>	t <sub>WCS</sub>	0	—	0	—	ns	15	
CAS Setup Time for CAS Before RAS Refresh	t <sub>CELCEL</sub>	t <sub>CSR</sub>	5	—	5	—	ns		
CAS Hold Time for CAS Before RAS Refresh	t <sub>RELCEH</sub>	t <sub>CHR</sub>	10	—	15	—	ns		
RAS Precharge to CAS Active Time	t <sub>REHCEL</sub>	t <sub>RPC</sub>	5	—	5	—	ns		
CAS Precharge Time for CAS Before RAS Counter Test	t <sub>CEHCEL</sub>	t <sub>CPT</sub>	20	—	20	—	ns		
RAS Hold Time from CAS Precharge (EDO)	t <sub>CEHREH</sub>	t <sub>RHCP</sub>	35	—	40	—	ns		
RAS Pulse Width (EDO)	t <sub>RELREH</sub>	t <sub>RASP</sub>	60	100 k	70	100 k	ns		
RAS to Next CAS Delay (EDO)	t <sub>RELCEL</sub>	t <sub>RNCD</sub>	60	—	70	—	ns		
EDO Cycle Time	t <sub>CELCEL</sub>	t <sub>EPC</sub>	25	—	30	—	ns		
Output Data Hold Time	t <sub>CELQZ</sub>	t <sub>COH</sub>	5	—	5	—	ns		
Output Buffer Turn–Off Delay from RAS	t <sub>REHQZ</sub>	t <sub>REZ</sub>	0	15	0	15	ns	10, 16	
Output Buffer Turn–Off Delay from W	t <sub>WLQZ</sub>	t <sub>WEZ</sub>	0	15	0	15	ns	10	
W to Data Delay	t <sub>WLDV</sub>	t <sub>WED</sub>	15	—	15	—	ns		

## NOTES:

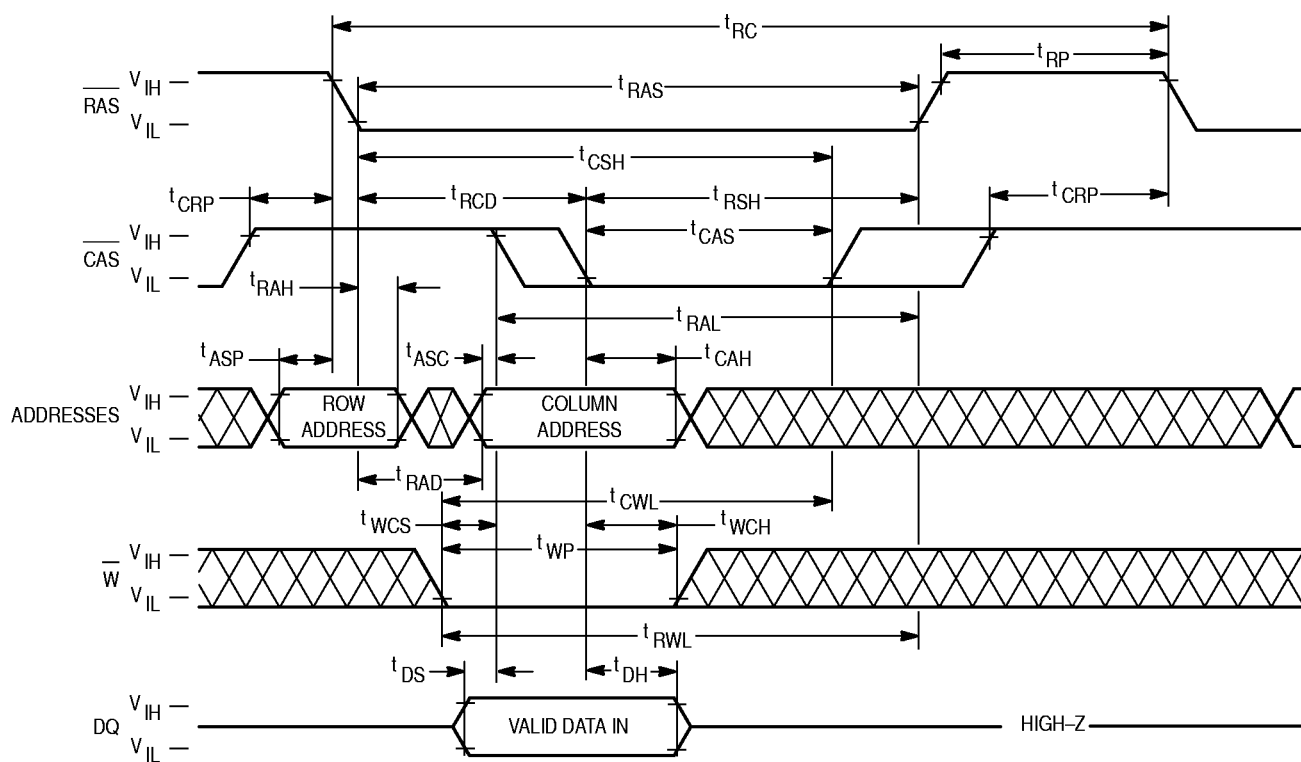
- Either t<sub>RRH</sub> or t<sub>RCH</sub> must be satisfied for a read cycle.
- These parameters are referenced to CAS leading edge in write cycles.
- t<sub>WCS</sub>, t<sub>RWD</sub>, t<sub>CWD</sub>, t<sub>AWD</sub>, and t<sub>CPWD</sub> are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if t<sub>WCS</sub> ≥ t<sub>WCS</sub> (min), the cycle is a write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisfied, the condition of the data out (at access time) is indeterminate.
- If RAS goes high before CAS goes high, the open circuit condition is controlled by CAS going high (t<sub>OFF</sub>). If CAS goes high before RAS goes high, the open circuit condition is controlled by RAS going high (t<sub>REZ</sub>).
- To avoid bus contention and potential damage to the module, RAS0 and RAS1 may not be active low simultaneously. Similarly, RAS2 and RAS3 may not be simultaneously active low.

TIMING DIAGRAMS

READ CYCLE

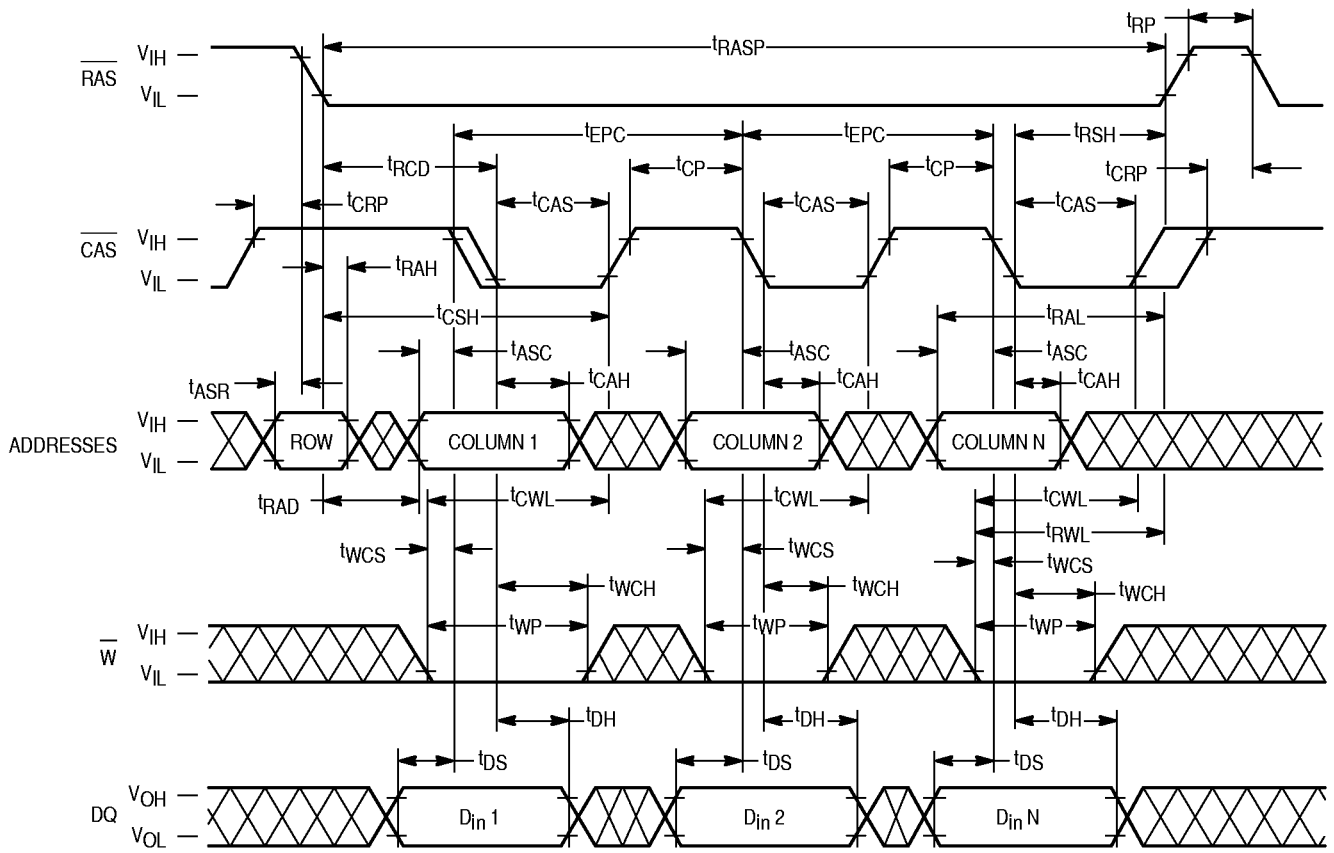


WRITE CYCLE

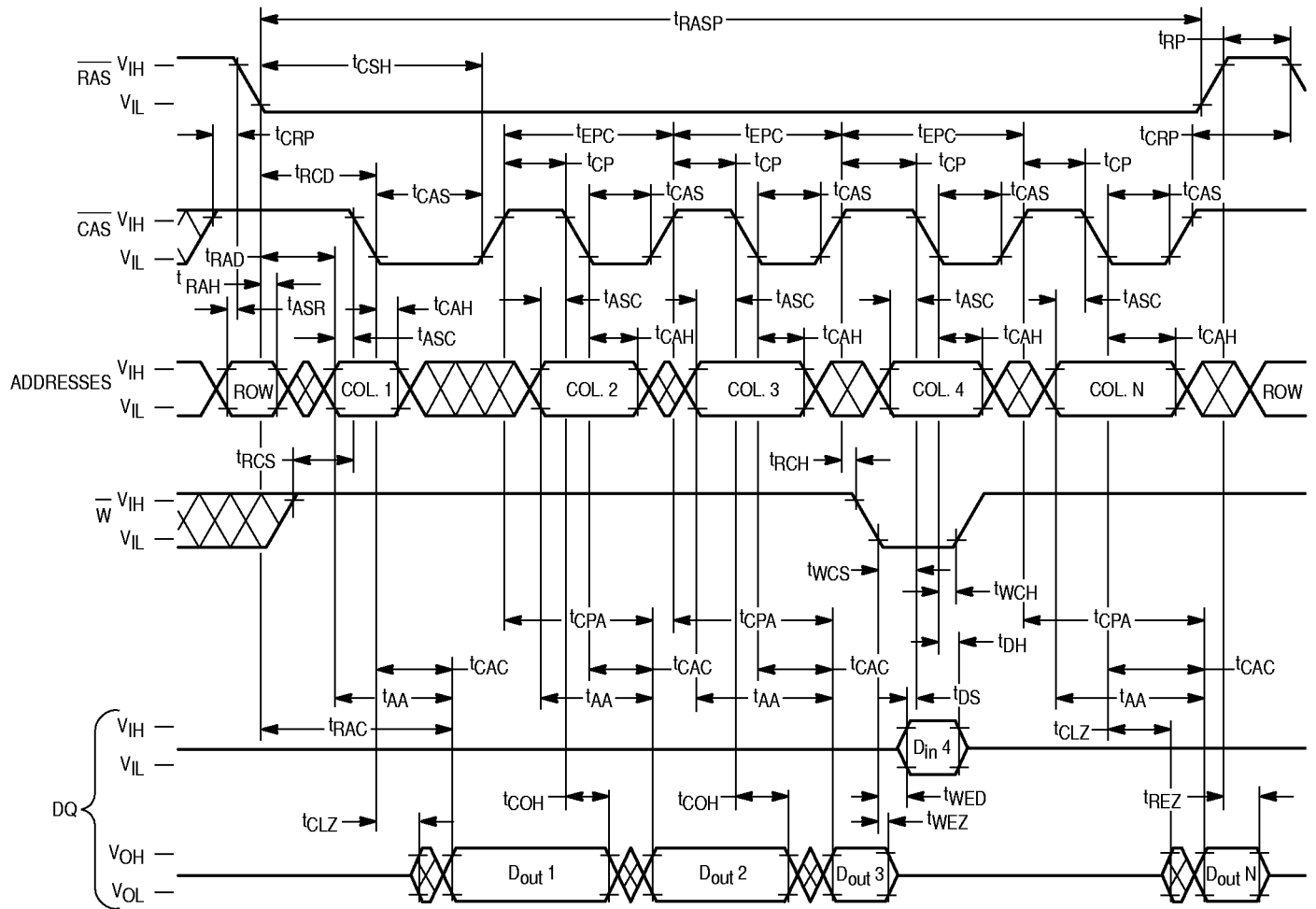




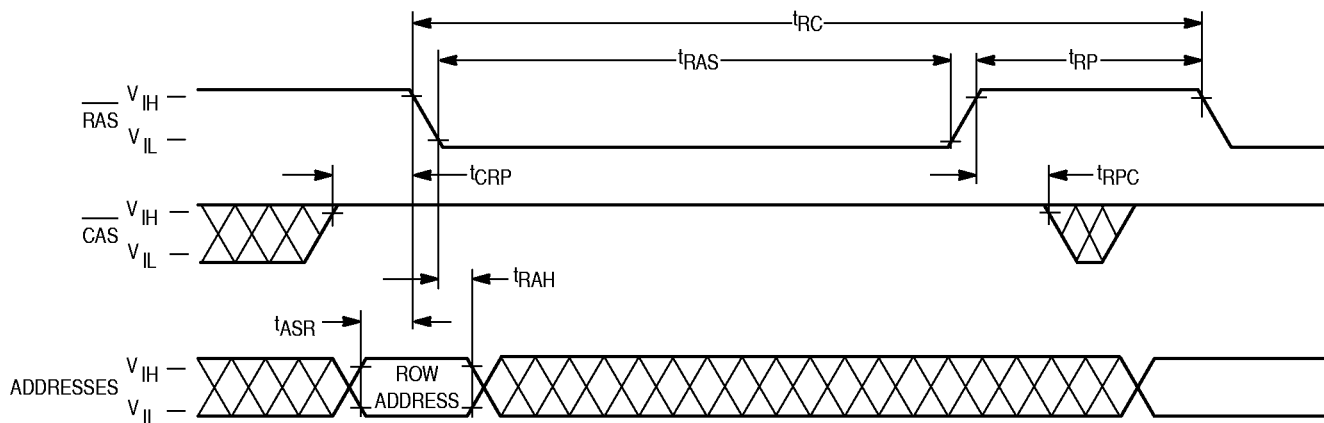
EXTENDED DATA OUT WRITE CYCLE



EXTENDED DATA OUT READ WRITE MIXED CYCLE

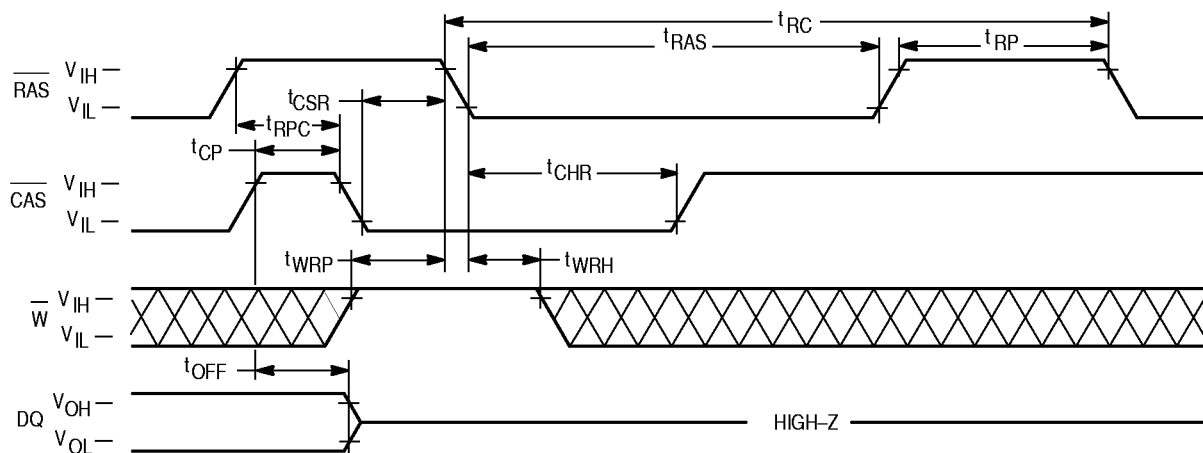


**RAS ONLY REFRESH CYCLE**



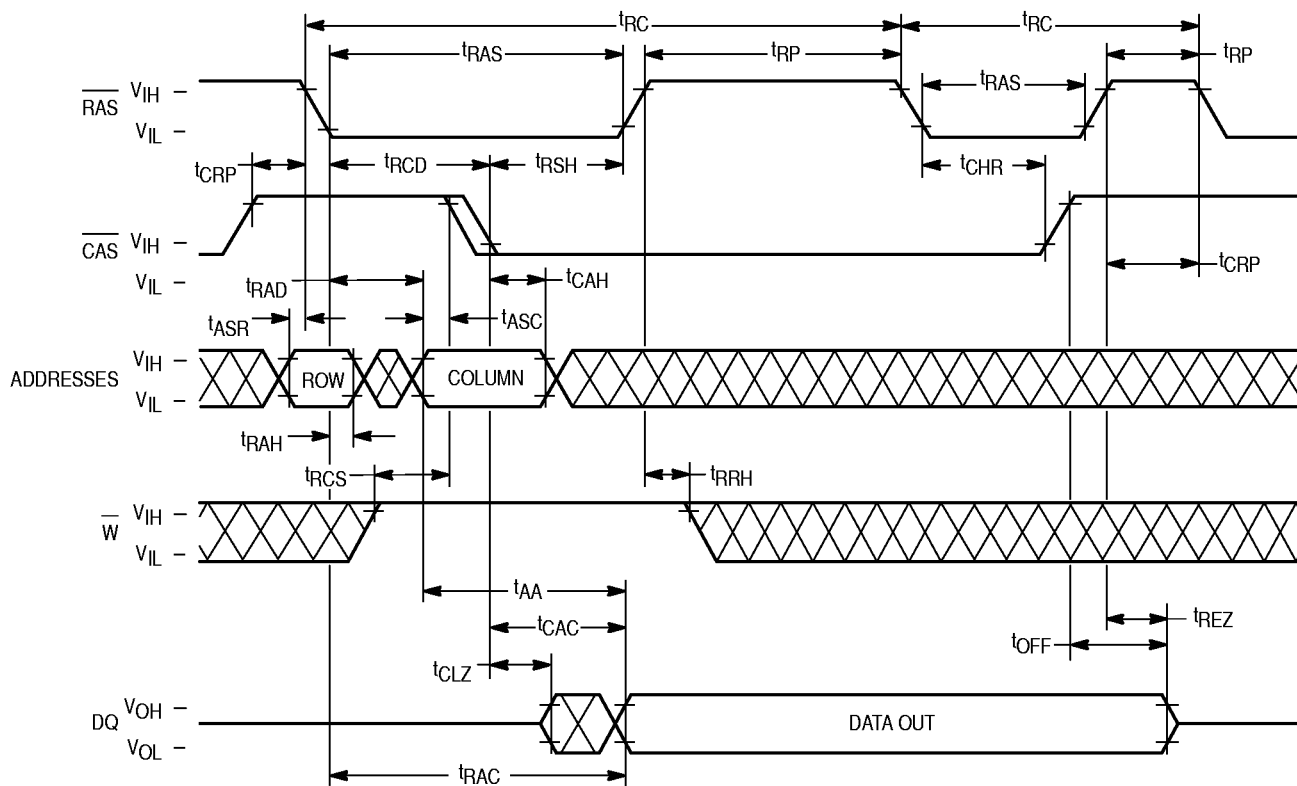
NOTE:  $\bar{W}$  = H or L.  
DQ = Open.

**CAS BEFORE RAS REFRESH CYCLE**

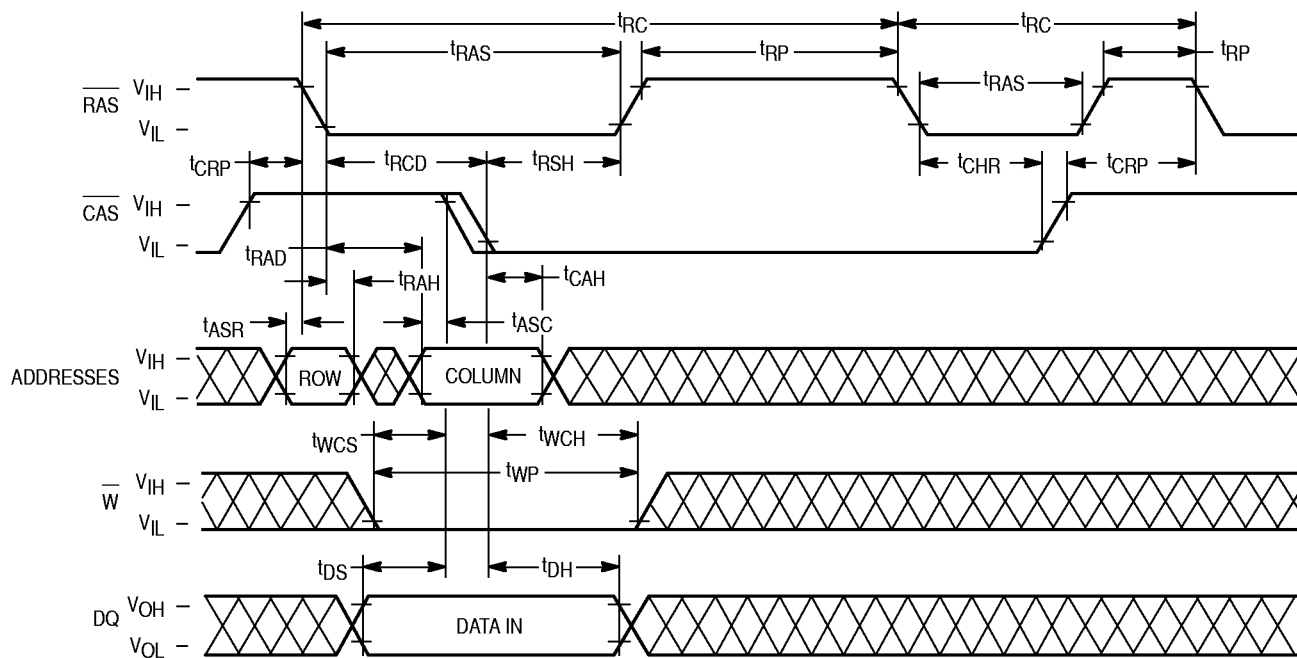


NOTE: Addresses = H or L.  
4MB, 8MB:  $\bar{W}$  = H or L.  
16MB, 32MB:  $\bar{W}$  must be as shown to avoid switching into component test mode.

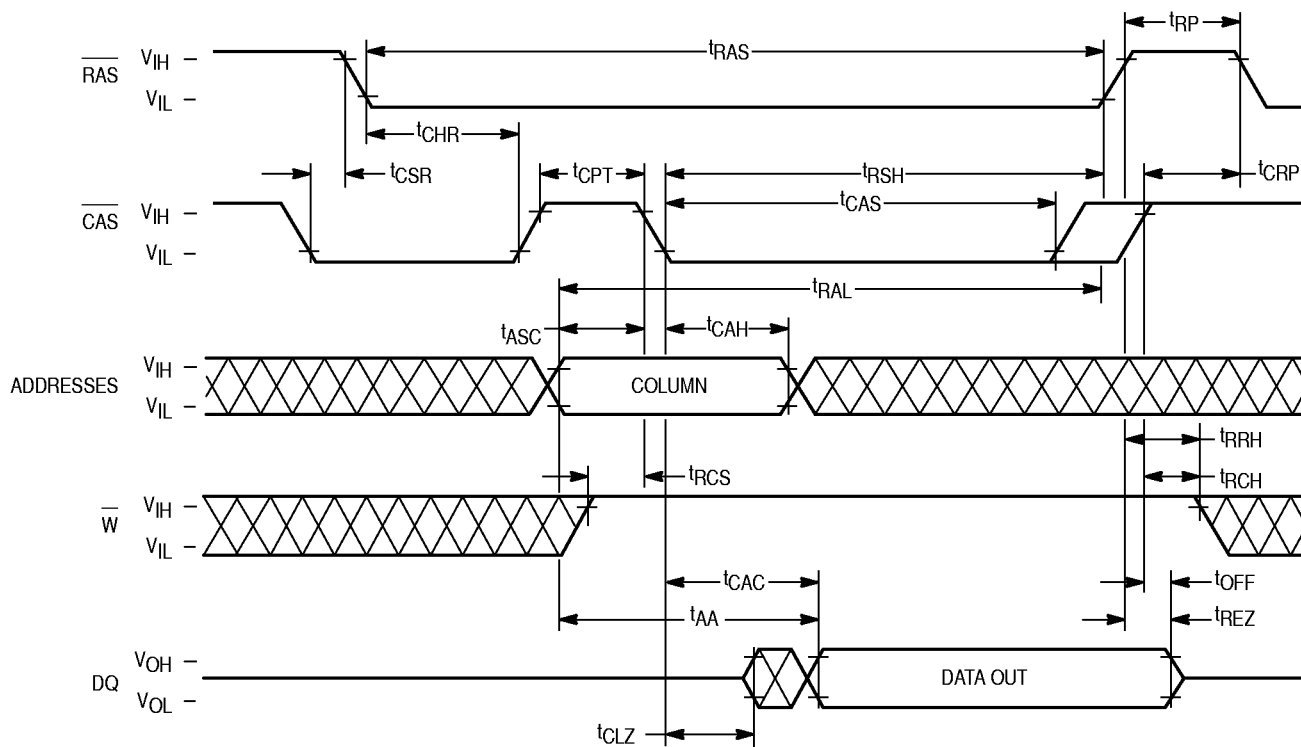
HIDDEN REFRESH CYCLE (READ)



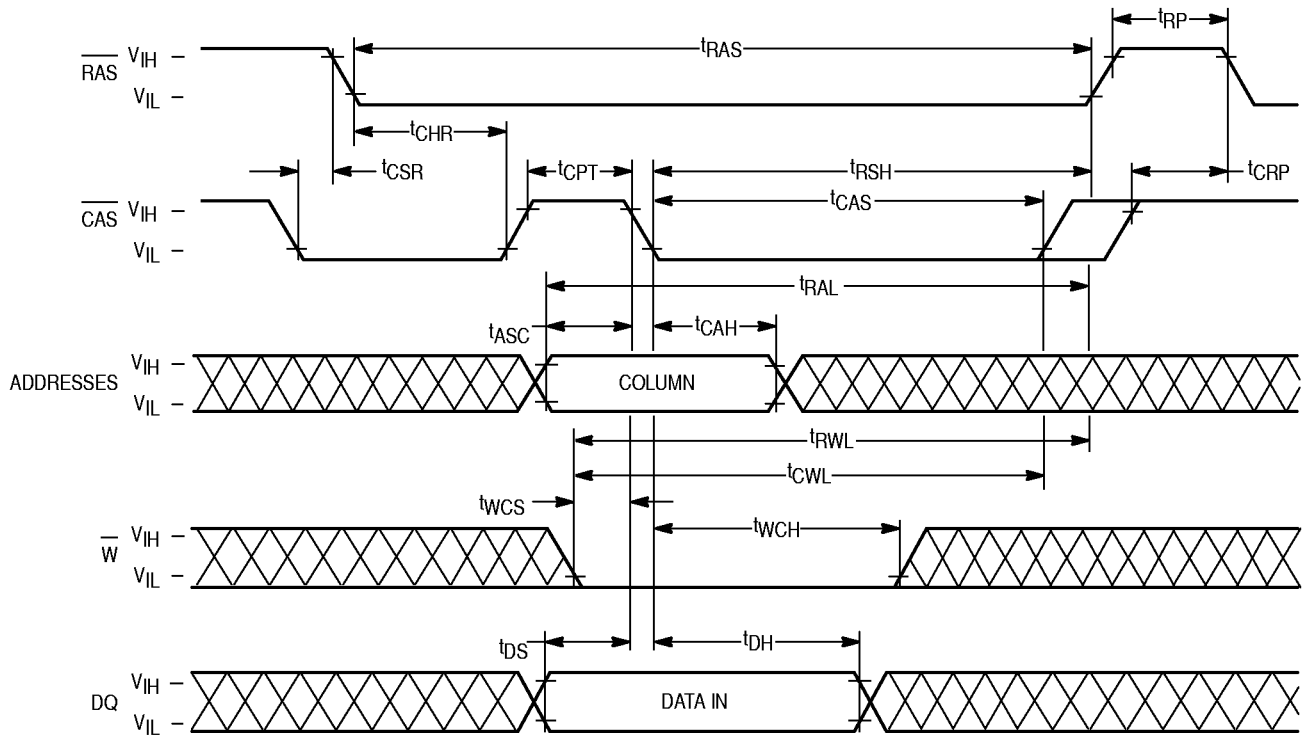
**HIDDEN REFRESH CYCLE (WRITE)**



**CAS BEFORE RAS REFRESH COUNTER TEST READ CYCLE**



CAS BEFORE RAS REFRESH COUNTER TEST WRITE CYCLE



## DEVICE INITIALIZATION

On power-up, an initial pause of 200  $\mu$ s is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the module. During an extended inactive state (greater than 16 ms with the device powered up for the 4MB and 8MB, 32 ms for the 16MB and 32MB), a wake up sequence of eight active cycles is necessary to ensure proper operation.

## ADDRESSING THE RAM

The address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe (RAS) and column address strobe (CAS), into two separate address fields. For the 4MB and 8MB a total of 20 address bits, 10 rows and 10 columns, will decode one of the word locations in the device. For the 16MB and 32MB a total of 22 address bits, 11 rows and 11 columns, will decode one of the word locations in the device. RAS active transition is followed by CAS active transition (active =  $V_{IL}$ ,  $t_{RCD}$  minimum) for all read or write cycles. The delay between RAS and CAS active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external CAS signal is ignored until an internal RAS signal is available. This "gate" feature on the external CAS clock enables the internal CAS line as soon as the row address hold time ( $t_{RAH}$ ) specification is met (and defines  $t_{RCD}$  minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the CAS clock.

There are three other variations in addressing the module: **RAS-only refresh cycle**, **CAS before RAS refresh cycle**, and **page mode**. All three are discussed in separate sections that follow.

## READ CYCLE

The DRAM may be read with either a "normal" random read cycle or an EDO read cycle. The normal read cycle is outlined here, while the EDO mode cycle is discussed in a separate section.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with RAS and CAS active transitions latching the desired bit location. The write (W) input level must be high ( $V_{IH}$ ),  $t_{RCS}$  (minimum) before the CAS active transition, to enable read mode.

Both the RAS and CAS clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. CAS controls read access time: CAS must be active before or at  $t_{RCD}$  maximum to guarantee valid data out (DQ) at  $t_{RAC}$  (access time from RAS active transition). If the  $t_{RCD}$  maximum is exceeded, read access time is determined by the CAS clock active transition ( $t_{CAC}$ ).

The RAS and CAS clocks must remain active for a minimum time of  $t_{RAS}$  and  $t_{CAS}$ , respectively, to complete the read cycle. W must remain high throughout the cycle, and for time  $t_{RRH}$  or  $t_{RCH}$  after RAS or CAS inactive transition, respectively, to maintain the data at that bit location. Once

RAS transitions to inactive, it must remain inactive for a minimum time of  $t_{RP}$  to precharge the internal device circuitry for the next active cycle.

## WRITE CYCLE

The user can write to the DRAM with either a write or an EDO mode write cycle. The write mode is discussed here, while EDO mode write operations are covered in a separate section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of W to active ( $V_{IL}$ ). Write mode is distinguished by the active transition of W, with respect to CAS. Minimum active time  $t_{RAS}$  and  $t_{CAS}$ , and precharge time  $t_{RP}$  apply to write mode, as in the read mode.

A write cycle is characterized by W active transition at minimum time  $t_{WCS}$  before CAS active transition. Data in (DQ) is referenced to CAS in a write cycle. RAS and CAS clocks must stay active for  $t_{RWL}$  and  $t_{CWL}$ , respectively, after the start of the write operation to complete the cycle.

## EDO MODE CYCLES

EDO mode allows fast successive data operations at all column locations on a selected row of the module. Read access time in EDO mode ( $t_{CAC}$ ) is typically half the regular RAS clock access time,  $t_{RAC}$ . EDO mode operation consists of keeping RAS active while toggling CAS between  $V_{IH}$  and  $V_{IL}$ . The row is latched by RAS active transition, while each CAS active transition allows selection of a new column location on the row.

An EDO mode cycle is initiated by a normal read or write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, CAS transitions to inactive for minimum  $t_{CP}$ , while RAS remains low ( $V_{IL}$ ). The second CAS active transition while RAS is low initiates the first EDO mode cycle ( $t_{EPC}$ ). Either a read or write operation can be performed in an EDO mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive EDO mode cycles and performed in any order. The maximum number of consecutive EDO mode cycles is limited by  $t_{RASP}$ . EDO mode operation is ended when RAS transitions to inactive, coincident with or following CAS inactive transition.

## REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits require refresh every  $t_{RFSH}$ .

This is accomplished by cycling through the row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6  $\mu$ s. Burst refresh, a refresh of all rows consecutively, must be performed every  $t_{RFSH}$ .

A normal read or write operation to the RAM will refresh all the bits associated with the particular row decodes. Three other methods of refresh, **RAS-only refresh**, **CAS before RAS refresh**, and **hidden refresh** are available on this device for greater system flexibility.

### RAS-Only Refresh

RAS-only refresh consists of RAS transition to active, latching the row address to be refreshed, while CAS remains high ( $V_{IH}$ ) throughout the cycle. An external counter is employed to ensure that all rows are refreshed within the specified limit.

### CAS Before RAS Refresh

CAS before RAS refresh is enabled by bringing CAS active before RAS. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

### Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding CAS active at the end of a read or write cycle, while RAS cycles inactive for  $t_{RP}$  and back to active, starts the hidden refresh. This is essentially the execution of a CAS before RAS refresh from a cycle in progress (see Figure 1). It is subject to the same conditions with respect to RAS active transition (to prevent test mode cycle) as in CAS before RAS refresh.

### CAS BEFORE RAS REFRESH COUNTER TEST

The internal refresh counter of the device can be tested with a CAS before RAS refresh counter test. This refresh counter test is performed with read and write operations. During this test, the internal refresh counter generates the row address, while the external address input supplies the column address. The entire array is refreshed after completing one cycle for every column, as indicated by the check data written in each row. See CAS before RAS refresh counter test cycle timing diagram.

The test can be performed only after a minimum of 8 CAS before RAS initialization cycles. The test procedure is as follows:

1. Write 0s into all memory cells (normal write mode).
2. Select a column address, and read 0 out of the cell by performing CAS before RAS refresh counter test, read cycle. Repeat this operation for every column.
3. Select a column address, and write 1 into the cell by performing CAS before RAS refresh counter test, write cycle. Repeat this operation for every column.
4. Read 1s (normal read mode), which were written at step three.
5. Repeat steps one through four using complement data.

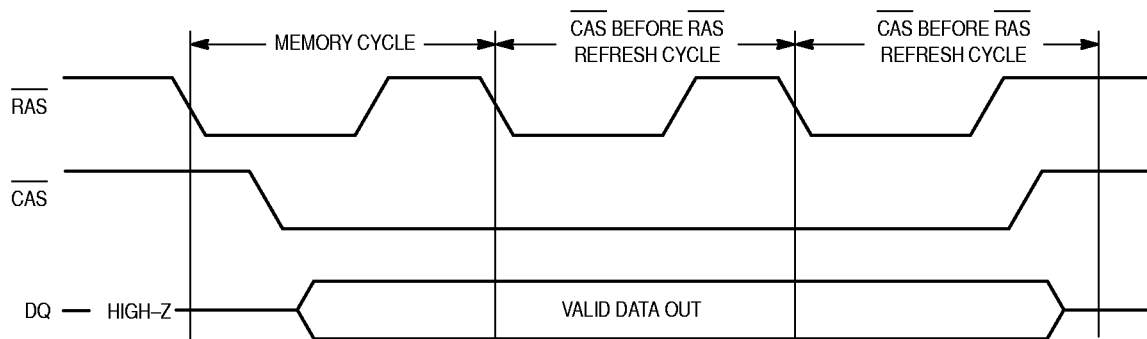
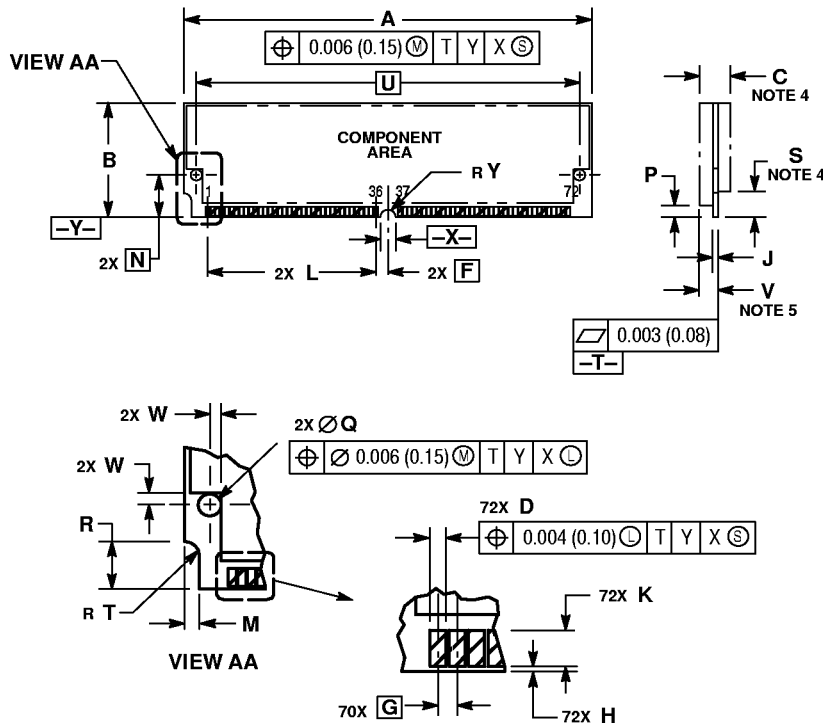


Figure 1. Hidden Refresh Cycle

PACKAGE DIMENSIONS

72-LEAD SIMM  
CASE 866A-02

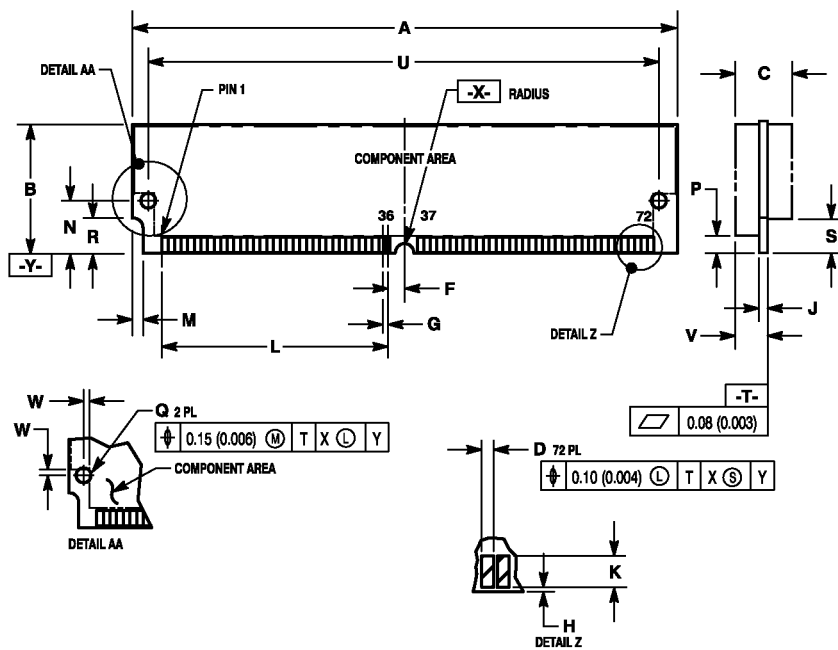


NOTES:

10. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
11. CONTROLLING DIMENSION: INCH.
12. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALIZATION.
13. DIMENSIONS C AND S DEFINE A DOUBLE-SIDED MODULE.
14. DIMENSION V DEFINES OPTIONAL SINGLE-SIDED MODULE.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	4.245	4.255	107.92	108.08
B	1.245	1.255	31.62	31.88
C	—	0.360	—	9.14
D	0.040	0.042	1.02	1.07
F	0.125 BSC	—	3.18 BSC	—
G	0.050 BSC	—	1.27 BSC	—
H	—	0.010	—	0.25
J	0.047	0.053	1.19	1.35
K	0.100	—	1.19	—
L	1.750 REF	—	44.45 REF	—
M	0.075	0.085	1.90	2.16
N	0.400 BSC	—	10.16 BSC	—
P	0.125	—	3.18	—
Q	0.123	0.127	3.12	3.23
R	0.245	0.255	6.22	6.48
S	0.225	—	5.72	—
T	0.060	0.064	1.52	1.63
U	3.984 BSC	—	101.19 BSC	—
V	—	0.208	—	5.28
W	0.044	—	1.12	—
Y	0.060	0.064	1.52	1.63

72-LEAD SIMM  
CASE 866-02

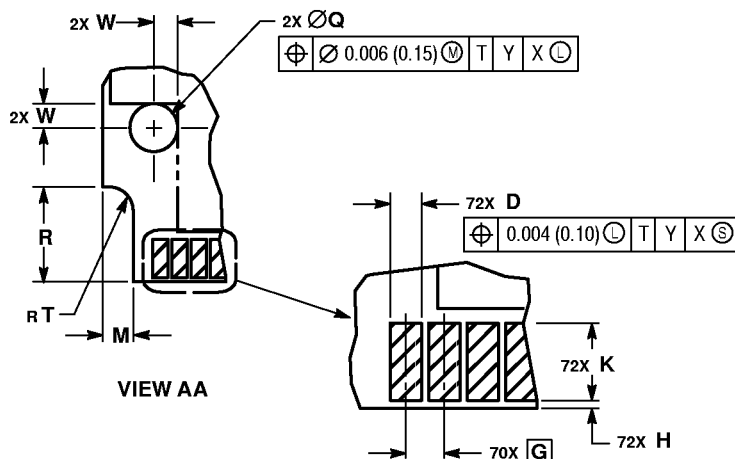
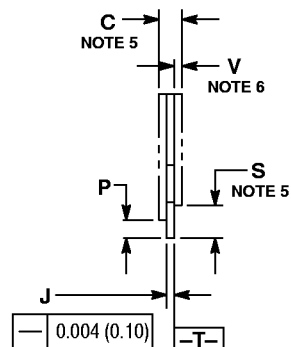
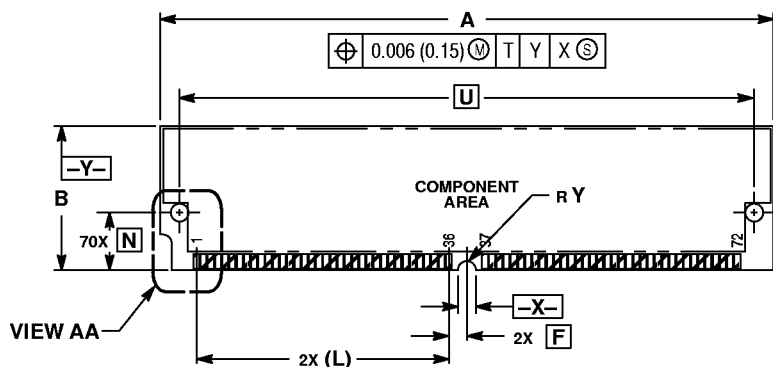


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3. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALIZATION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	107.82	108.08	4.245	4.255
B	25.27	25.53	0.995	1.005
C	—	9.14	—	0.360
D	1.02	1.07	0.040	0.042
F	3.18 BSC	—	0.125 BSC	—
G	1.27 BSC	—	0.050 BSC	—
H	—	0.25	—	0.010
J	1.19	1.37	0.047	0.054
K	0.25	—	0.100	—
L	44.45 REF	—	1.750 REF	—
M	1.90	2.16	0.075	0.085
N	10.16 BSC	—	0.400 BSC	—
P	3.18	—	0.125	—
Q	3.12	3.22	0.123	0.127
R	6.22	6.48	0.245	0.255
S	5.72	—	0.225	—
U	101.19 BSC	—	3.984 BSC	—
V	—	5.28	—	0.209
W	1.12	—	0.044	—
X	1.52	1.63	0.060	0.064

72-LEAD SIMM  
CASE 866H-01

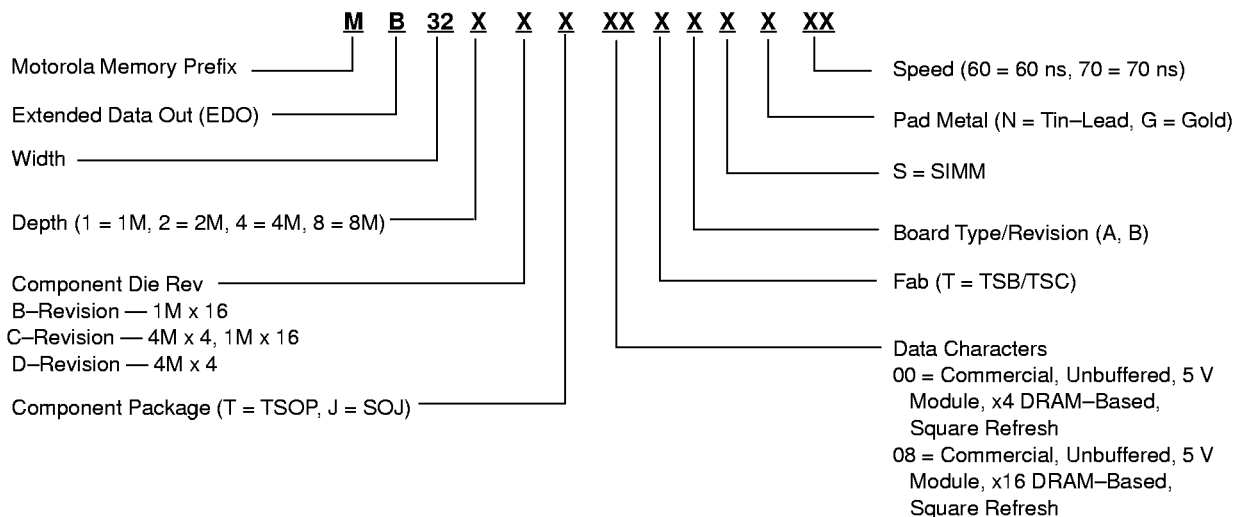


NOTES:

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2. CONTROLLING DIMENSION: INCH.
3. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALIZATION.
4. DIMENSIONS C AND S DEFINE A DOUBLE-SIDED MODULE.
5. DIMENSION V DEFINES OPTIONAL SINGLE-SIDED MODULE.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	4.245	4.255	107.82	108.08
B	0.995	1.005	25.27	25.53
C	—	0.157	—	4.00
D	0.040	0.042	1.02	1.07
F	0.125 BSC	—	3.18 BSC	—
G	0.050 BSC	—	1.27 BSC	—
H	—	0.010	—	0.25
J	0.047	0.053	1.19	1.35
K	0.100	—	2.54	—
L	1.750 REF	—	44.45 REF	—
M	0.075	0.085	1.91	2.16
N	0.400 BSC	—	10.16 BSC	—
P	0.125	—	3.18	—
Q	0.123	0.127	3.12	3.23
R	0.245	0.255	6.22	6.48
S	0.225	—	5.72	—
T	0.060	0.064	1.52	1.63
U	3.984 BSC	—	101.19 BSC	—
V	—	0.106	—	2.70
W	0.044	—	1.12	—
Y	0.060	0.064	1.52	1.63

**ORDERING INFORMATION**  
(Order by Full Part Number)



**REPLACEMENT PART NUMBERS FOR 1997**

Organization	Old Number	New 60	New 70
1M x 32	MB321BJ08TASN60 MB321BJ08TASG60 MB321BT08TASN60 MB321BT08TASG60	MB321CJ08TASN60 MB321CJ08TASG60 MB321CT08TASN60 MB321CT08TASG60	MB321CJ08TASN70 MB321CJ08TASG70 MB321CT08TASN70 MB321CT08TASG70
2M x 32	MB322BJ08TASN60 MB322BJ08TASG60 MB322BT08TASN60 MB322BT08TASG60	MB322CJ08TASN60 MB322CJ08TASG60 MB322CT08TASN60 MB322CT08TASG60	MB322CJ08TASN70 MB322CJ08TASG70 MB322CT08TASN70 MB322CT08TASG70
4M x 32	MB324CJ00TBSN60 MB324CJ00TBSG60 MB324CT00TBSN60 MB324CT00TBSG60	MB324DJ00TBSN60 MB324DJ00TBSG60 MB324DT00TBSN60 MB324DT00TBSG60	MB324DJ00TBSN70 MB324DJ00TBSG70 MB324DT00TBSN70 MB324DT00TBSG70
8M x 32	MB328CJ00TBSN60 MB328CJ00TBSG60 MB328CT00TBSN60 MB328CT00TBSG60	MB328DJ00TBSN60 MB328DJ00TBSG60 MB328DT00TBSN60 MB328DT00TBSG60	MB328DJ00TBSN70 MB328DJ00TBSG70 MB328DT00TBSN70 MB328DT00TBSG70