12×12 bit parallel and microprogrammable multiplier

018313 040783

LMU12/LMU13

general information

The LMU12/LMU13 are 12-bit parallel Multipliers with high speed and low power consumption. The LMU12 multipliers are pin and functionally compatible with TRW MPY-12HJ parts. The LMU13 multipliers are optimized for use in microprogrammed systems. Full military ambient temperature range operation is attained by the use of advanced CMOS technology.

The A and B operands and their mode controls TCA, TCB have 13-bit input registers. The mode controls specify the operands as two's complement or unsigned numbers.

At the output, a right shift control (RS) allows the user to select either a left shifted 23-bit product suitable for two's complement only, or a full 24-bit product.

Two 12-bit output registers are provided to hold the most and least significant halves of the result (MSR and LSR) as defined by RS. For asynchronous output these registers may be made transparent by taking the feed through control (FT) high. A round control (RND) allows the rounding of the MSR; this control is registered, and is entered whenever either input register is clocked.

In the LMU12 the A, B, MSR and LSR registers have independent clocks: CLKA, CLKB, CLKM, CLKL.

The LMU13 differs in that it has a single clock input (CLK) and three register enables (ENA, ENB, ENR) for the two input registers and the entire product, respectively. This facilitates the use of the part in microprogrammed systems. In both parts data is entered into the registers on the positive edge of the clock.

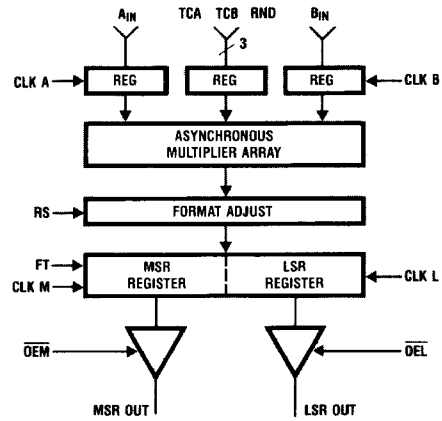
PIN CONFIGURATION LMU12 (LMU13)

PIN	FUNCTION	PIN	FUNCTION
1	A7	64	A8
2	A6	63	A9
3	A5	62	A10
4	A4	61	A11
5	A3	60	CLKA ($\overline{ENA}$)
6	A2	59	CLKB ($\overline{ENB}$)
7	A1	58	RND
8	A0	57	TCA
9	R0	56	B0
10	R1	55	B1
11	R2	54	B2
12	R3	53	B3
13	R4	52	B4
14	R5	51	B5
15	R6	50	V_{CC}
16	R7	49	V_{CC}
17	R8	48	V_{CC}
18	R9	47	B6
19	R10	46	B7
20	R11	45	B8
21	$\overline{OEL}$	44	B9
22	$\overline{OEM}$	43	B10
23	GND	42	B11
24	GND	41	TCB
25	FT	40	R23
26	RS	39	R22
27	CLKL ($\overline{CLK}$)	38	R21
28	CLKM ($\overline{ENR}$)	37	R20
29	R12	36	R19
30	R13	35	R18
31	R14	34	R17
32	R15	33	R16

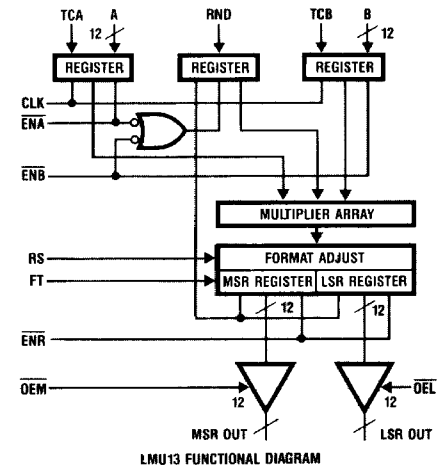
features

- **High-speed (65ns), low-power (100mW) CMOS 12 x 12 Parallel Multiplier**
- **LMU12 functionally and pin compatible with TRW MPY-12HJ**
- **TTL inputs and outputs**
- **Three-state outputs**
- **Two's complement unsigned or mixed operands**
- **High-Rel screening available**
- **Wide range of packaging available; ceramic DIP, PGA, LCC, low cost plastic LCC**

functional diagram



LMU12 FUNCTIONAL DIAGRAM



LMU13 FUNCTIONAL DIAGRAM

absolute maximum ratings

Supply Voltage	−0.5 to 7.0V
Input Voltage	0 to 5.5V
Output Voltage	0 to V_{CC}
Storage Temperature	−65°C to 150°C

recommended operating conditions

PARAMETER		min	typ	max	unit
V_{CC}	Supply Voltage Commercial	4.75	5.0	5.25	V
V_{CC}	Supply Voltage Military	4.50	5.0	5.5	V
I_{OL}	Low Level Output Current			4.0	mA
I_{OH}	High Level Output Current			−2.0	mA
T_{AMB}	Operating Temperature Commercial (Ambient)	0	25	70	°C
T_{AMB}	Operating Temperature Military (Ambient)	−55	25	125	°C

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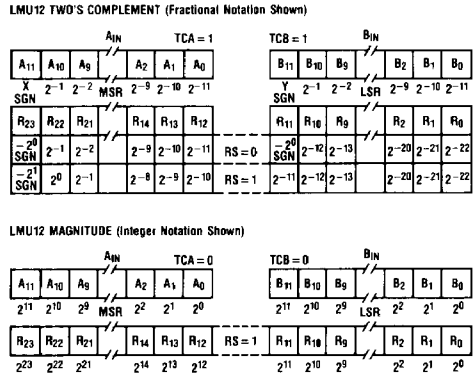
electrical characteristics

PARAMETER		TEST CONDITIONS	min	typ	max	unit
V_{IL}	Low Level Input Voltage				0.8	V
V_{IH}	High Level Input Voltage		2.0			V
V_{OL}	Low Level Output Voltage	V_{CC} = min I_{OL} = 4mA			0.5	V
V_{OH}	High Level Output Voltage	V_{CC} = min I_{OH} = −2.0mA	3.5			V
I_{IL}	Low Level Input Current	V_{CC} = max V_{IL} = 0.4V			20	μA
I_{IH}	High level Input Current	V_{CC} = max V_{IH} = 2.4V			20	μA
I_{CC}	Supply Current	Military Commercial		25[1] 28	35[2] 40[3]	mA
I_{CC}	Quiescent				0.5	mA

1) 5MHZ clock rate: TTL input levels; V_{CC} = 5V; T_A = 25°C; random input patterns.
2) 5MHZ clock: V_{IH} = 2.0; V_{IL} = 0.8; V_{CC} = 5.5V; T_A = −55°C; all outputs toggling every clock cycle.
3) As above, T_A = 0°C.

input/output formats

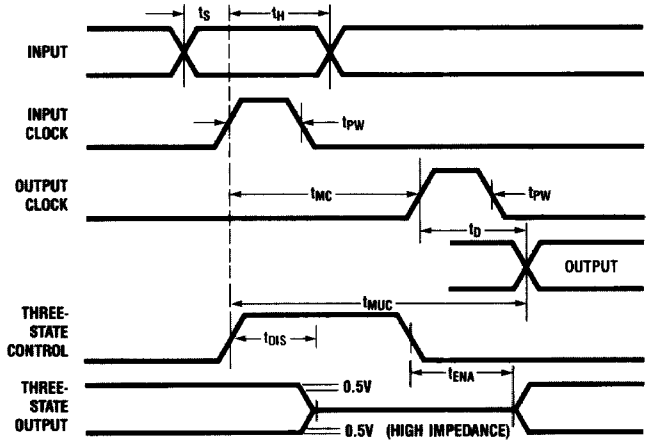


switching characteristics

		LMU12/LMU13				LMU12-1/LMU13-1				
		0°C–70°C V_{CC} = 4.75V		−55°C–125°C V_{CC} = 4.5V		0°C–70°C V_{CC} = 4.75V		−55°C–125°C V_{CC} = 4.5V		
PARAMETER		min	max	min	max	min	max	min	max	unit
t_{MC}	Multiply Time (Clocked)		80		100		65		75	ns
t_{MUC}	Unclocked Multiply Time		110		130		95		110	ns
t_D	Output Delay		30		35		26		30	ns
t_{ENA}	Three-State Enable Time		26		35		22		26	ns
t_{DIS}	Three-State Disable Time		24		35		20		24	ns
t_{PW}	Clock Pulse Width	25		25		25		25		ns
t_S	Input Register Setup Time	15		20		15		18		ns
t_H	Input Register Hold Time	5		6		0		0		ns

AC TEST CONDITIONS: Input levels: 0 to 3V Output timing reference level: 1.5V Output load: 1.0KΩ to 5V, 820Ω to GND, 60PF to GND

timing diagram

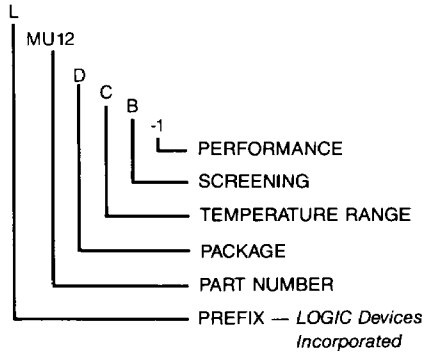


ordering information

PACKAGE*
D — Hermetic DIP
P — Molded DIP
K — Leadless Chip Carrier
X — Dice
G — Pin Grid
L — Leaded Chip Carrier
J — Plastic Chip Carrier
C — Cerdip
*Not all parts available in all packages.

TEMPERATURE RANGE
C — 0°C to +70°C
V_{CC} = 4.75 to 5.25V
M — −55°C to +125°C
V_{CC} = 4.5 to 5.5V

SCREENING
No Designator — Commercial
B — Hi Rel Process Flow
R — 48 hour Burn-In at 125°C
T — Custom



The LMU12-1/LMU13-1 meet or exceed all specifications of the LMU12/LMU13. LOGIC Devices Incorporated may, at its discretion, ship these products to fill LMU12/LMU13 orders.

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