

## 32 M-WORD BY 72-BIT SYNCHRONOUS DYNAMIC RAM MODULE

### REGISTERED TYPE

#### Description

The MC-4532DA726 is a 33,554,432 words by 72 bits synchronous dynamic RAM module on which 18 pieces of 128 M SDRAM :  $\mu$ PD45128441 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

#### Features

- 33,554,432 words by 72 bits organization (ECC type)
- Clock frequency and access time from CLK

Part number	/CAS latency	Clock frequency (MAX.)	Access time from CLK (MAX.)	Module type
MC-4532DA726EF-A80	CL = 3	125 MHz	6 ns	PC100 Registered DIMM Rev. 1.0 Compliant
	CL = 2	100 MHz	6 ns	
MC-4532DA726EF-A10	CL = 3	100 MHz	6 ns	
	CL = 2	77 MHz	7 ns	
★ MC-4532DA726EFB-A80	CL = 3	125 MHz	6 ns	PC100 Registered DIMM Rev. 1.2 Compliant
	CL = 2	100 MHz	6 ns	
★ MC-4532DA726EFB-A10	CL = 3	100 MHz	6 ns	
	CL = 2	77 MHz	7 ns	

- Fully Synchronous Dynamic RAM, with all signals referenced to a positive clock edge
- Pulsed interface
- Possible to assert random column address in every cycle
- Quad internal banks controlled by BA0 and BA1 (Bank Select)
- Programmable burst-length (1, 2, 4, 8 and Full Page)
- Programmable wrap sequence (Sequential / Interleave)
- Programmable /CAS latency (2, 3)
- Automatic precharge and controlled precharge
- CBR (Auto) refresh and self refresh
- All DQs have  $10\ \Omega \pm 10\%$  of series resistor
- Single 3.3 V  $\pm 0.3$  V power supply
- LVTTTL compatible
- 4,096 refresh cycles/64 ms
- Burst termination by Burst Stop command and Precharge command
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Registered type
- Serial PD

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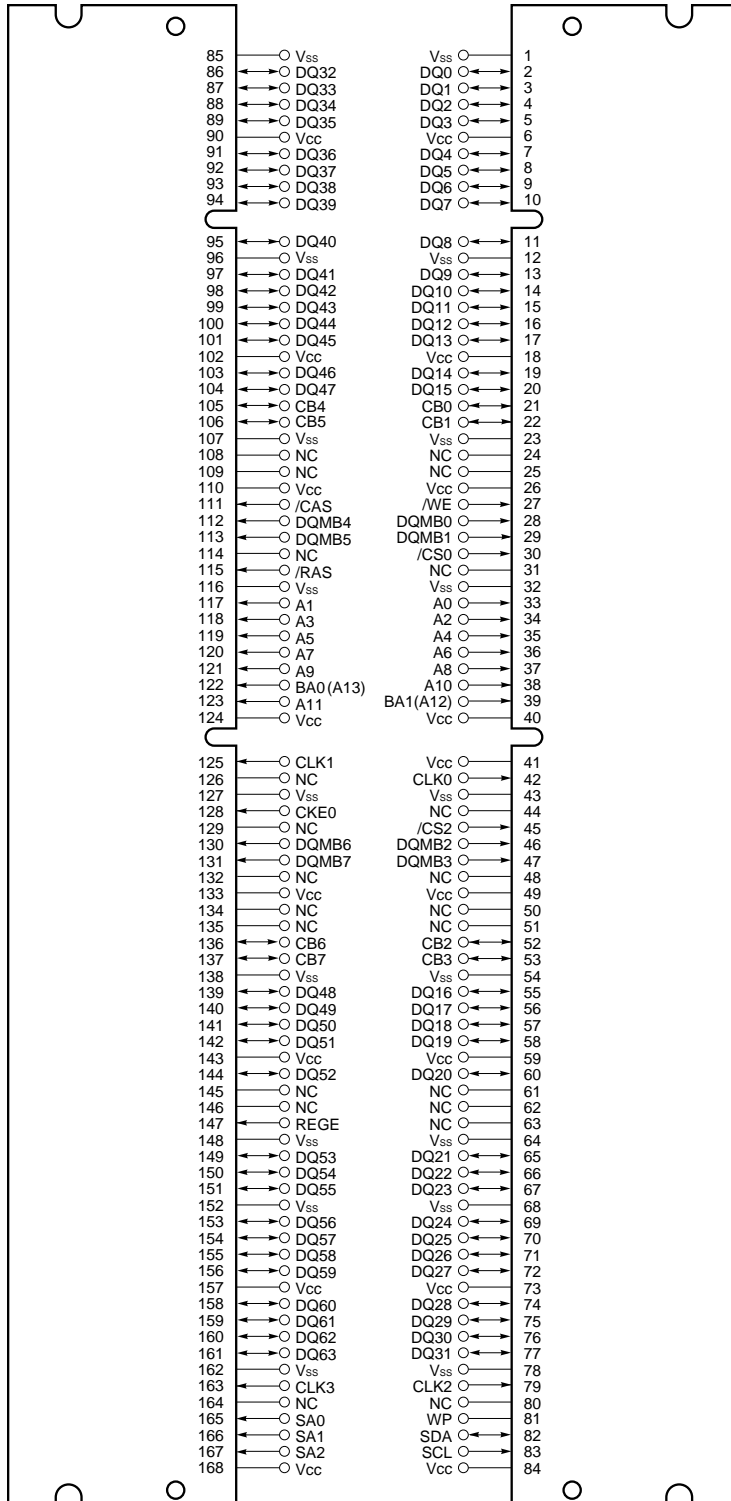
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

**Ordering Information**

Part number	Clock frequency MHz (MAX.)	Package	Mounted devices
MC-4532DA726EF-A80	125 MHz	168-pin Dual In-line Memory Module (Socket Type)	18 pieces of $\mu$ PD45128441G5 (Rev. E) (400 mil TSOP (II))
MC-4532DA726EF-A10	100 MHz		
★ MC-4532DA726EFB-A80	125 MHz	Edge connector : Gold plated	
★ MC-4532DA726EFB-A10	100 MHz	43.18 mm (1.7 inch) height	

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plated)

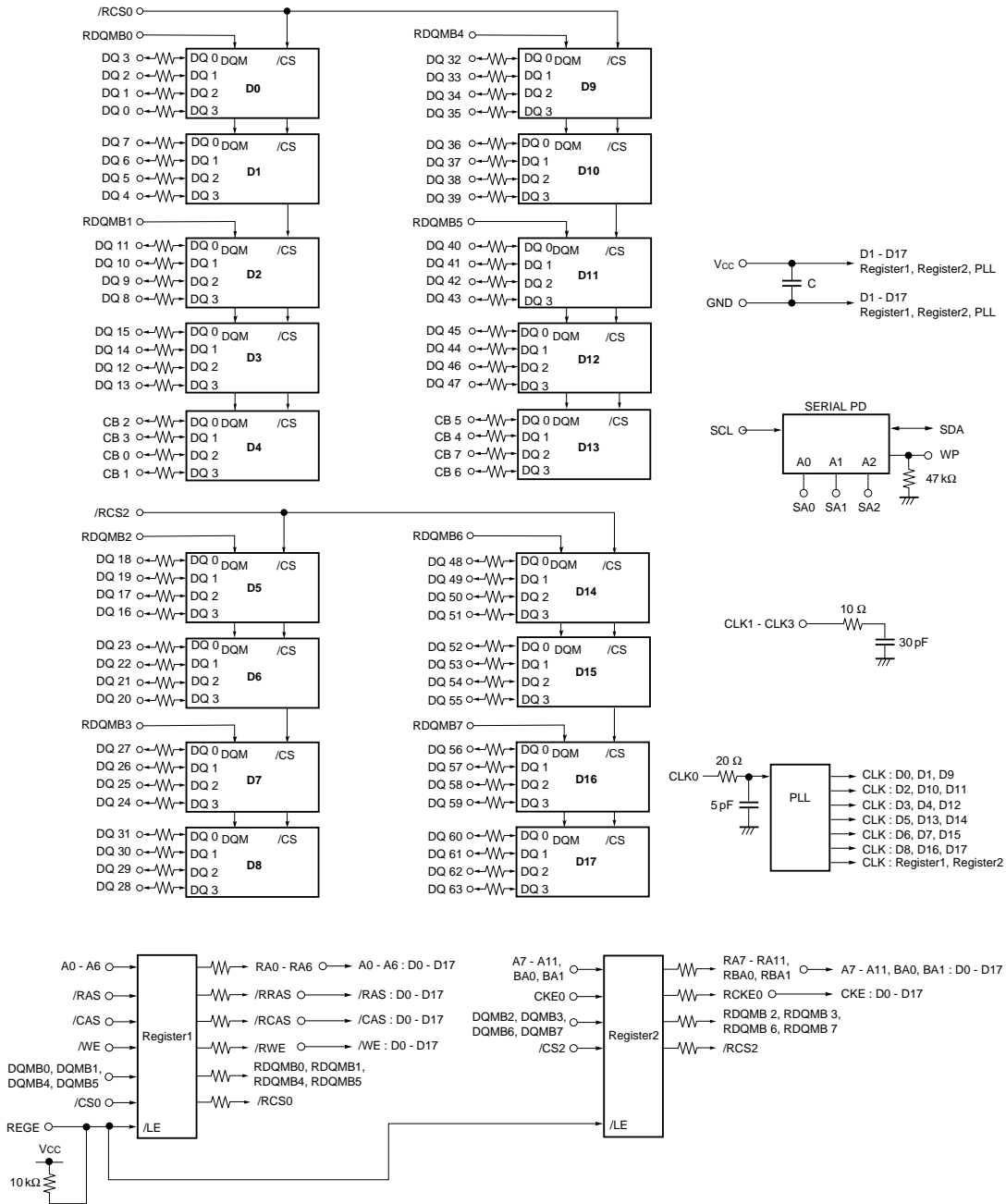


/xxx indicates active low signal.

- A0 - A11 : Address Inputs  
[Row : A0 - A11, Column : A0 - A9, A11]
- BA0 (A13), BA1 (A12) : SDRAM Bank Select
- DQ0 - DQ63, CB0 - CB7 : Data Inputs/Outputs
- CLK0 - CLK3 : Clock Input
- CKE0 : Clock Enable Input
- WP : Write Protect
- /CS0, /CS2 : Chip Select Input
- /RAS : Row Address Strobe
- /CAS : Column Address Strobe
- /WE : Write Enable
- DQMB0 - DQMB7 : DQ Mask Enable
- SA0 - SA2 : Address Input for EEPROM
- SDA : Serial Data I/O for PD
- SCL : Clock Input for PD
- Vcc : Power Supply
- Vss : Ground
- REGE : Register / Buffer Enable
- NC : No Connection

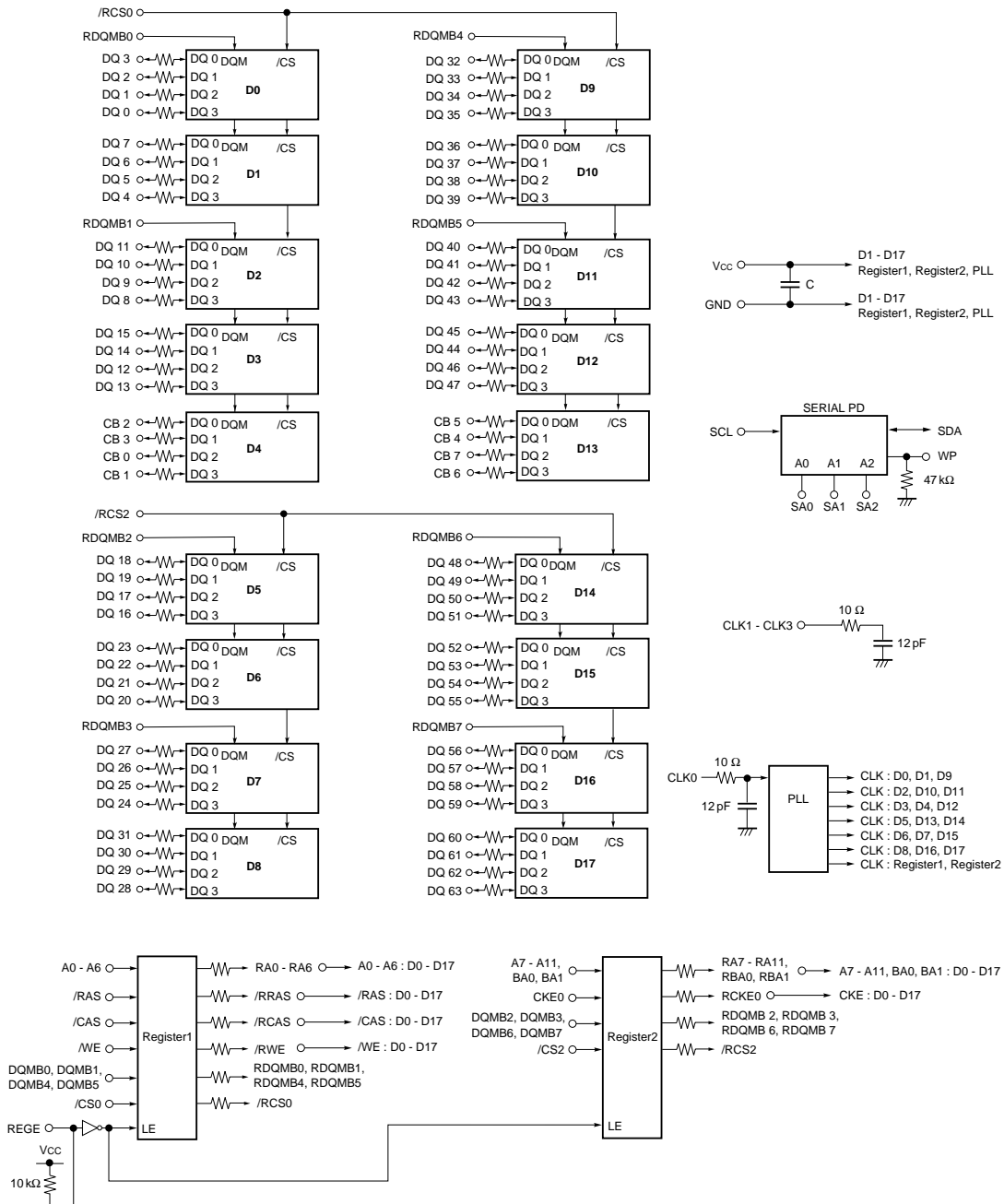
Block Diagram

[ MC-4532DA726EF ]



- Remarks**
1. The value of all resistors of DQs is 10 Ω.
  2. D0 - D17 : μPD45128441 (8 M words × 4 bits × 4 banks)
  3. REGE ≤ V<sub>IL</sub> : Buffer mode  
REGE ≥ V<sub>IH</sub> : Register mode
  4. Register : SN74ALVC16334DGG  
PLL : CDC2509APW

★ [ MC-4532DA726EFB ]



- Remarks**
1. The value of all resistors of DQs is 10 Ω.
  2. D0 - D17 : μPD45128441 (8 M words × 4 bits × 4 banks)
  3. REGE ≤ V<sub>IL</sub> : Buffer mode  
REGE ≥ V<sub>IH</sub> : Register mode
  4. Register : HD74ALVC16835  
PLL : HD74CDC2509B

**Electrical Specifications**

- All voltages are referenced to V<sub>SS</sub> (GND).
- After power up, wait more than 1 ms and then, execute power on sequence and CBR (Auto) refresh before proper device operation is achieved.

**Absolute Maximum Ratings**

Parameter	Symbol	Condition	Rating	Unit
Voltage on power supply pin relative to GND	V <sub>CC</sub>		-0.5 to +4.6	V
Voltage on input pin relative to GND	V <sub>I</sub>		-0.5 to +4.6	V
Short circuit output current	I <sub>O</sub>		50	mA
Power dissipation	P <sub>D</sub>		21	W
Operating ambient temperature	T <sub>A</sub>		0 to +70	°C
Storage temperature	T <sub>stg</sub>		-55 to +125	°C

**Caution** Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**Recommended Operating Conditions**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V <sub>CC</sub>		3.0	3.3	3.6	V
High level input voltage	V <sub>IH</sub>		2.0		V <sub>CC</sub> + 0.3	V
Low level input voltage	V <sub>IL</sub>		-0.3		+0.8	V
Operating ambient temperature	T <sub>A</sub>		0		70	°C

**Capacitance (T<sub>A</sub> = 25 °C, f = 1 MHz)**

**[ MC-4532DA726EF ]**

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C <sub>i1</sub>	A0 - A11, BA0 (A13), BA1 (A12), /RAS, /CAS, /WE	4		10	pF
	C <sub>i2</sub>	CLK0 - CLK3	15		35	
	C <sub>i3</sub>	CKE0	8		18	
	C <sub>i4</sub>	/CS0, /CS2	4		10	
	C <sub>i5</sub>	DQMB0 - DQMB7	4		10	
Data input/output capacitance	C <sub>i/o</sub>	DQ0 - DQ63, CB0 - CB7	6		13	pF

★ **[ MC-4532DA726EFB ]**

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C <sub>i1</sub>	A0 - A11, BA0 (A13), BA1 (A12), /RAS, /CAS, /WE	TBD		TBD	pF
	C <sub>i2</sub>	CLK0 - CLK3	TBD		TBD	
	C <sub>i3</sub>	CKE0	TBD		TBD	
	C <sub>i4</sub>	/CS0, /CS2	TBD		TBD	
	C <sub>i5</sub>	DQMB0 - DQMB7	TBD		TBD	
Data input/output capacitance	C <sub>i/o</sub>	DQ0 - DQ63, CB0 - CB7	TBD		TBD	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

[ MC-4532DA726EF ]

Parameter	Symbol	Test condition	Grade	MIN.	MAX.	Unit	Notes
Operating current	I <sub>CC1</sub>	Burst length = 1 t <sub>RC</sub> ≥ t <sub>RC(MIN.)</sub> , I <sub>O</sub> = 0 mA	/CAS latency = 2	-A80	2,100	mA	1
				-A10	2,100		
			/CAS latency = 3	-A80	2,100		
				-A10	2,100		
Precharge standby current in power down mode	I <sub>CC2P</sub>	CKE ≤ V <sub>IL(MAX.)</sub> , t <sub>CK</sub> = 15 ns			268	mA	
	I <sub>CC2PS</sub>	CKE ≤ V <sub>IL(MAX.)</sub> , t <sub>CK</sub> = ∞			29		
Precharge standby current in non power down mode	I <sub>CC2N</sub>	CKE ≥ V <sub>IH(MIN.)</sub> , t <sub>CK</sub> = 15 ns, /CS ≥ V <sub>IH(MIN.)</sub> , Input signals are changed one time during 30 ns.			610	mA	
	I <sub>CC2NS</sub>	CKE ≥ V <sub>IH(MIN.)</sub> , t <sub>CK</sub> = ∞ , Input signals are stable.			144		
Active standby current in power down mode	I <sub>CC3P</sub>	CKE ≤ V <sub>IL(MAX.)</sub> , t <sub>CK</sub> = 15 ns			340	mA	
	I <sub>CC3PS</sub>	CKE ≤ V <sub>IL(MAX.)</sub> , t <sub>CK</sub> = ∞			72		
Active standby current in non power down mode	I <sub>CC3N</sub>	CKE ≥ V <sub>IH(MIN.)</sub> , t <sub>CK</sub> = 15 ns, /CS ≥ V <sub>IH(MIN.)</sub> , Input signals are changed one time during 30 ns.			790	mA	
	I <sub>CC3NS</sub>	CKE ≥ V <sub>IH(MIN.)</sub> , t <sub>CK</sub> = ∞ , Input signals are stable.			360		
Operating current (Burst mode)	I <sub>CC4</sub>	t <sub>CK</sub> ≥ t <sub>CK(MIN.)</sub> , I <sub>O</sub> = 0 mA	/CAS latency = 2	-A80	2,190	mA	2
				-A10	1,830		
			/CAS latency = 3	-A80	2,640		
				-A10	2,280		
CBR (Auto) Refresh current	I <sub>CC5</sub>	t <sub>RC</sub> ≥ t <sub>RC(MIN.)</sub>	/CAS latency = 2	-A80	4,260	mA	3
				-A10	4,260		
			/CAS latency = 3	-A80	4,260		
				-A10	4,260		
Self refresh current	I <sub>CC6</sub>	CKE ≤ 0.2 V			286	mA	
Input leakage current	I <sub>I(L)</sub>	V <sub>I</sub> = 0 to 3.6 V, All other pins not under test = 0 V		-10	+10	μA	
Output leakage current	I <sub>O(L)</sub>	D <sub>OUT</sub> is disabled, V <sub>O</sub> = 0 to 3.6 V		-1.5	+1.5	μA	
High level output voltage	V <sub>OH</sub>	I <sub>O</sub> = -4.0 mA		2.4		V	
Low level output voltage	V <sub>OL</sub>	I <sub>O</sub> = +4.0 mA			0.4	V	

- Notes**
- I<sub>CC1</sub> depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I<sub>CC1</sub> is measured on condition that addresses are changed only one time during t<sub>CK(MIN.)</sub>.
  - I<sub>CC4</sub> depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I<sub>CC4</sub> is measured on condition that addresses are changed only one time during t<sub>CK(MIN.)</sub>.
  - I<sub>CC5</sub> is measured on condition that addresses are changed only one time during t<sub>CK(MIN.)</sub>.

★ [ MC-4532DA726EFB ]

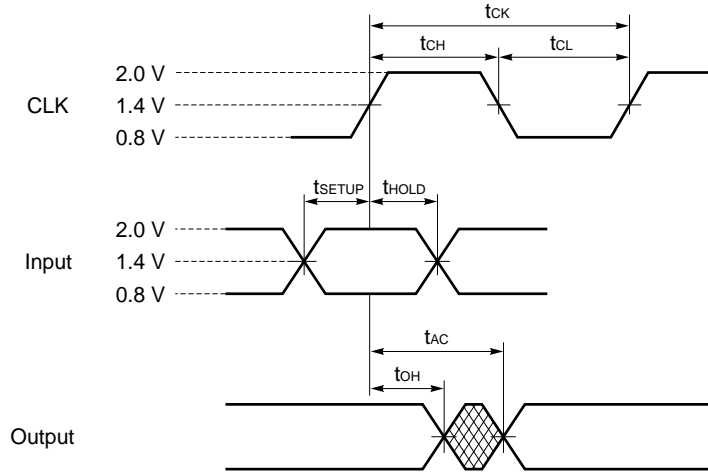
Parameter	Symbol	Test condition		Grade	MIN.	MAX.	Unit	Notes
Operating current	I <sub>CC1</sub>	Burst length = 1 t <sub>RC</sub> ≥ t <sub>RC (MIN.)</sub> , I <sub>O</sub> = 0 mA	/CAS latency = 2	-A80		2,100	mA	1
				-A10		2,100		
			/CAS latency = 3	-A80		2,100		
				-A10		2,100		
Precharge standby current in power down mode	I <sub>CC2P</sub>	CKE ≤ V <sub>IL (MAX.)</sub> , t <sub>CK</sub> = 15 ns				268	mA	
	I <sub>CC2PS</sub>	CKE ≤ V <sub>IL (MAX.)</sub> , t <sub>CK</sub> = ∞				86		
Precharge standby current in non power down mode	I <sub>CC2N</sub>	CKE ≥ V <sub>IH (MIN.)</sub> , t <sub>CK</sub> = 15 ns, /CS ≥ V <sub>IH (MIN.)</sub> , Input signals are changed one time during 30 ns.				610	mA	
	I <sub>CC2NS</sub>	CKE ≥ V <sub>IH (MIN.)</sub> , t <sub>CK</sub> = ∞ , Input signals are stable.				224		
Active standby current in power down mode	I <sub>CC3P</sub>	CKE ≤ V <sub>IL (MAX.)</sub> , t <sub>CK</sub> = 15 ns				340	mA	
	I <sub>CC3PS</sub>	CKE ≤ V <sub>IL (MAX.)</sub> , t <sub>CK</sub> = ∞				132		
Active standby current in non power down mode	I <sub>CC3N</sub>	CKE ≥ V <sub>IH (MIN.)</sub> , t <sub>CK</sub> = 15 ns, /CS ≥ V <sub>IH (MIN.)</sub> , Input signals are changed one time during 30 ns.				790	mA	
	I <sub>CC3NS</sub>	CKE ≥ V <sub>IH (MIN.)</sub> , t <sub>CK</sub> = ∞ , Input signals are stable.				440		
Operating current (Burst mode)	I <sub>CC4</sub>	t <sub>CK</sub> ≥ t <sub>CK (MIN.)</sub> , I <sub>O</sub> = 0 mA	/CAS latency = 2	-A80		2,190	mA	2
				-A10		1,830		
			/CAS latency = 3	-A80		2,640		
				-A10		2,280		
CBR (Auto) Refresh current	I <sub>CC5</sub>	t <sub>RC</sub> ≥ t <sub>RC (MIN.)</sub>	/CAS latency = 2	-A80		4,260	mA	3
				-A10		4,260		
			/CAS latency = 3	-A80		4,260		
				-A10		4,260		
Self refresh current	I <sub>CC6</sub>	CKE ≤ 0.2 V				286	mA	
Input leakage current	I <sub>I (L)</sub>	V <sub>I</sub> = 0 to 3.6 V, All other pins not under test = 0 V			-10	+10	μA	
Input leakage current (CKE0)					-20	+20		
Output leakage current	I <sub>O (L)</sub>	D <sub>OUT</sub> is disabled, V <sub>O</sub> = 0 to 3.6 V			-1.5	+1.5	μA	
High level output voltage	V <sub>OH</sub>	I <sub>O</sub> = -4.0 mA			2.4		V	
Low level output voltage	V <sub>OL</sub>	I <sub>O</sub> = +4.0 mA				0.4	V	

- Notes**
- I<sub>CC1</sub> depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I<sub>CC1</sub> is measured on condition that addresses are changed only one time during t<sub>CK (MIN.)</sub>.
  - I<sub>CC4</sub> depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I<sub>CC4</sub> is measured on condition that addresses are changed only one time during t<sub>CK (MIN.)</sub>.
  - I<sub>CC5</sub> is measured on condition that addresses are changed only one time during t<sub>CK (MIN.)</sub>.

**AC Characteristics (Recommended Operating Conditions unless otherwise noted)**

**AC Characteristics Test Conditions**

- AC measurements assume  $t_r = 1$  ns.
- Reference level for measuring timing of input signals is 1.4 V. Transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
- If  $t_r$  is longer than 1 ns, reference level for measuring timing of input signals is  $V_{IH(MIN.)}$  and  $V_{IL(MAX.)}$ .
- An access time is measured at 1.4 V.

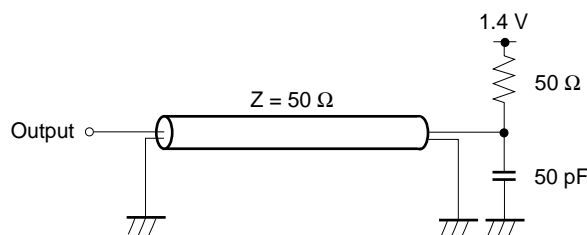


Synchronous Characteristics (Registered Mode)

[ MC-4532DA726EF ]

Parameter		Symbol	-A80		-A 10		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
Clock cycle time	/CAS latency = 3	t <sub>CK3</sub>	8	(125 MHz)	10	(100 MHz)	ns	
	/CAS latency = 2	t <sub>CK2</sub>	10	(100 MHz)	13	(77 MHz)	ns	
Access time from CLK	/CAS latency = 3	t <sub>AC3</sub>		6		6	ns	1
	/CAS latency = 2	t <sub>AC2</sub>		6		7	ns	1
★ Input CLK frequency			50	125	50	100	MHz	
Input CLK duty cycle			40	60	40	60	%	
Data-out hold time	/CAS latency = 3	t <sub>OH3</sub>	3		3		ns	1
	/CAS latency = 2	t <sub>OH2</sub>	3		3		ns	1
Data-out low-impedance time		t <sub>LZ</sub>	0		0		ns	
Data-out high-impedance time	/CAS latency = 3	t <sub>HZ3</sub>	3	6	3	6	ns	
	/CAS latency = 2	t <sub>HZ2</sub>	3	6	3	7	ns	
Data-in setup time		t <sub>DS</sub>	2		2		ns	
Data-in hold time		t <sub>DH</sub>	1		1		ns	
Address setup time		t <sub>AS</sub>	1.5		1.5		ns	
Address hold time		t <sub>AH</sub>	0.9		0.9		ns	
CKE setup time		t <sub>CKS</sub>	1.5		1.5		ns	
CKE hold time		t <sub>CKH</sub>	0.9		0.9		ns	
CKE setup time (Power down exit)		t <sub>CKSP</sub>	1.5		1.5		ns	
Command (/CS0, /CS2, /RAS, /CAS, /WE, DQMB0 - DQMB7) setup time		t <sub>CMS</sub>	1.5		1.5		ns	
Command (/CS0, /CS2, /RAS, /CAS, /WE, DQMB0 - DQMB7) hold time		t <sub>CMH</sub>	0.9		0.9		ns	

Note 1. Output load

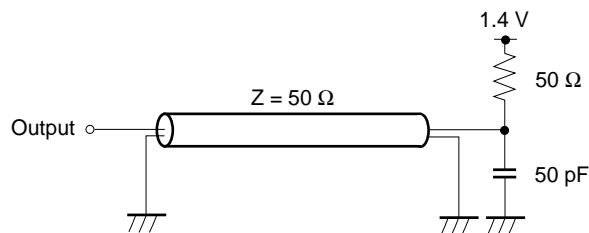


Remark These specifications are applied to the monolithic device.

★ [ MC-4532DA726EFB ]

Parameter		Symbol	-A80		-A10		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
Clock cycle time	/CAS latency = 3	t <sub>CK3</sub>	8	(125 MHz)	10	(100 MHz)	ns	
	/CAS latency = 2	t <sub>CK2</sub>	10	(100 MHz)	13	(77 MHz)	ns	
Access time from CLK	/CAS latency = 3	t <sub>AC3</sub>		6		6	ns	1
	/CAS latency = 2	t <sub>AC2</sub>		6		7	ns	1
Input CLK frequency			50	125	50	100	MHz	
Input CLK duty cycle			40	60	40	60	%	
Data-out hold time	/CAS latency = 3	t <sub>OH3</sub>	3		3		ns	1
	/CAS latency = 2	t <sub>OH2</sub>	3		3		ns	1
Data-out low-impedance time		t <sub>LZ</sub>	0		0		ns	
Data-out high-impedance time	/CAS latency = 3	t <sub>HZ3</sub>	3	6	3	6	ns	
	/CAS latency = 2	t <sub>HZ2</sub>	3	6	3	7	ns	
Data-in setup time		t <sub>DS</sub>	2		2		ns	
Data-in hold time		t <sub>DH</sub>	1		1		ns	
Address setup time		t <sub>AS</sub>	2		2		ns	
Address hold time		t <sub>AH</sub>	1		1		ns	
CKE setup time		t <sub>CKS</sub>	2		2		ns	
CKE hold time		t <sub>CKH</sub>	1		1		ns	
CKE setup time (Power down exit)		t <sub>CKSP</sub>	2		2		ns	
Command (/CS0, /CS2, /RAS, /CAS, /WE, DQMB0 - DQMB7) setup time		t <sub>CMS</sub>	2		2		ns	
Command (/CS0, /CS2, /RAS, /CAS, /WE, DQMB0 - DQMB7) hold time		t <sub>CMH</sub>	1		1		ns	

**Note 1.** Output load



**Remark** These specifications are applied to the monolithic device.

**Asynchronous Characteristics (Registered Mode)**

Parameter	Symbol	-A80		-A10		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
ACT to REF/ACT command period (Operation)	t <sub>RC</sub>	70		70		ns	
REF to REF/ACT command period (Refresh)	t <sub>RC1</sub>	70		78		ns	
ACT to PRE command period	t <sub>RAS</sub>	48	120,000	50	120,000	ns	
PRE to ACT command period	t <sub>RP</sub>	20		20		ns	
Delay time ACT to READ/WRITE command	t <sub>RCD</sub>	20		20		ns	
ACT(0) to ACT(1) command period	t <sub>RRD</sub>	16		20		ns	
Data-in to PRE command period	t <sub>DPL</sub>	-1CLK+8		-1CLK+10		ns	
Data-in to ACT(REF) command period (Auto precharge)	/CAS latency = 3	t <sub>DAL3</sub>	20	20		ns	
	/CAS latency = 2	t <sub>DAL2</sub>	20	20		ns	
Mode register set cycle time	t <sub>RSC</sub>	2		2		CLK	
Transition time	t <sub>T</sub>	0.5	30	1	30	ns	
Refresh time (4,096 refresh cycles)	t <sub>REF</sub>		64		64	ms	

Serial PD

[ MC-4532DA726EF ]

(1/2)

Byte No.	Function Described	Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes	
0	Defines the number of bytes written into serial PD memory	80H	1	0	0	0	0	0	0	0	128 bytes	
1	Total number of bytes of serial PD memory	08H	0	0	0	0	1	0	0	0	256 bytes	
2	Fundamental memory type	04H	0	0	0	0	0	1	0	0	SDRAM	
3	Number of rows	0CH	0	0	0	0	1	1	0	0	12 rows	
4	Number of columns	0BH	0	0	0	0	1	0	1	1	11 columns	
5	Number of banks	01H	0	0	0	0	0	0	0	1	1 bank	
6	Data width	48H	0	1	0	0	1	0	0	0	72 bits	
7	Data width (continued)	00H	0	0	0	0	0	0	0	0	0	
8	Voltage interface	01H	0	0	0	0	0	0	0	1	LVTTTL	
9	CL = 3 Cycle time	-A80	80H	1	0	0	0	0	0	0	0	8 ns
		-A10	A0H	1	0	1	0	0	0	0	0	10 ns
10	CL = 3 Access time	-A80	60H	0	1	1	0	0	0	0	0	6 ns
		-A10	60H	0	1	1	0	0	0	0	0	6 ns
11	DIMM configuration type	02H	0	0	0	0	0	0	1	0	ECC	
12	Refresh rate/type	80H	1	0	0	0	0	0	0	0	Normal	
13	SDRAM width	04H	0	0	0	0	0	1	0	0	×4	
14	Error checking SDRAM width	04H	0	0	0	0	0	1	0	0	×4	
15	Minimum clock delay	01H	0	0	0	0	0	0	0	1	1 clock	
16	Burst length supported	8FH	1	0	0	0	1	1	1	1	1, 2, 4, 8, F	
17	Number of banks on each SDRAM	04H	0	0	0	0	0	1	0	0	4 banks	
18	/CAS latency supported	06H	0	0	0	0	0	1	1	0	2, 3	
19	/CS latency supported	01H	0	0	0	0	0	0	0	1	0	
20	/WE latency supported	01H	0	0	0	0	0	0	0	1	0	
21	SDRAM module attributes	1FH	0	0	0	1	1	1	1	1	Registered	
22	SDRAM device attributes : General	0EH	0	0	0	0	1	1	1	0		
23	CL = 2 Cycle time	-A80	A0H	1	0	1	0	0	0	0	0	10 ns
		-A10	D0H	1	1	0	1	0	0	0	0	13 ns
24	CL = 2 Access time	-A80	60H	0	1	1	0	0	0	0	0	6 ns
		-A10	70H	0	1	1	1	0	0	0	0	7 ns
25-26		00H	0	0	0	0	0	0	0	0		
27	t <sub>RP</sub> (MIN.)	-A80	14H	0	0	0	1	0	1	0	0	20 ns
		-A10	14H	0	0	0	1	0	1	0	0	20 ns
28	t <sub>RRD</sub> (MIN.)	-A80	10H	0	0	0	1	0	0	0	0	16 ns
		-A10	14H	0	0	0	1	0	1	0	0	20 ns
29	t <sub>RCD</sub> (MIN.)	-A80	14H	0	0	0	1	0	1	0	0	20 ns
		-A10	14H	0	0	0	1	0	1	0	0	20 ns
30	t <sub>RAS</sub> (MIN.)	-A80	30H	0	0	1	1	0	0	0	0	48 ns
		-A10	32H	0	0	1	1	0	0	1	0	50 ns
31	Module bank density	40H	0	1	0	0	0	0	0	0	256M bytes	

(2/2)

Byte No.	Function Described	Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes
32	Command and address signal input setup time	15H	0	0	0	1	0	1	0	1	1.5 ns
33	Command and address signal input hold time	09H	0	0	0	0	1	0	0	1	0.9 ns
34	Data signal input setup time	20H	0	0	1	0	0	0	0	0	2 ns
35	Data signal input hold time	10H	0	0	0	1	0	0	0	0	1 ns
36-61		00H	0	0	0	0	0	0	0	0	
62	SPD revision	12H	0	0	0	1	0	0	1	0	1.2A
63	Checksum for bytes 0 - 62	-A80	08H	0	0	0	0	1	0	0	0
		-A10	6EH	0	1	1	0	1	1	1	0
64-71	Manufacture's JEDEC ID code										
72	Manufacturing location										
73-90	Manufacture's P/N										
91	Revision Code										
93-94	Manufacturing date										
95-98	Assembly serial number										
99-125	Mfg specific										
126	Intel specification frequency	64H	0	1	1	0	0	1	0	0	100 MHz
127	Intel specification /CAS latency support	-A80	87H	1	0	0	0	0	1	1	1
		-A10	85H	1	0	0	0	0	1	0	1

★ [ MC-4532DA726EFB ]

(1/2)

Byte No.	Function Described	Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes
0	Defines the number of bytes written into serial PD memory	80H	1	0	0	0	0	0	0	0	128 bytes
1	Total number of bytes of serial PD memory	08H	0	0	0	0	1	0	0	0	256 bytes
2	Fundamental memory type	04H	0	0	0	0	0	1	0	0	SDRAM
3	Number of rows	0CH	0	0	0	0	1	1	0	0	12 rows
4	Number of columns	0BH	0	0	0	0	1	0	1	1	11 columns
5	Number of banks	01H	0	0	0	0	0	0	0	1	1 bank
6	Data width	48H	0	1	0	0	1	0	0	0	72 bits
7	Data width (continued)	00H	0	0	0	0	0	0	0	0	0
8	Voltage interface	01H	0	0	0	0	0	0	0	1	LVTTTL
9	CL = 3 Cycle time	-A80	80H	1	0	0	0	0	0	0	8 ns
		-A10	A0H	1	0	1	0	0	0	0	10 ns
10	CL = 3 Access time	-A80	60H	0	1	1	0	0	0	0	6 ns
		-A10	60H	0	1	1	0	0	0	0	6 ns
11	DIMM configuration type	02H	0	0	0	0	0	0	1	0	ECC
12	Refresh rate/type	80H	1	0	0	0	0	0	0	0	Normal
13	SDRAM width	04H	0	0	0	0	0	1	0	0	×4
14	Error checking SDRAM width	04H	0	0	0	0	0	1	0	0	×4
15	Minimum clock delay	01H	0	0	0	0	0	0	0	1	1 clock
16	Burst length supported	8FH	1	0	0	0	1	1	1	1	1, 2, 4, 8, F
17	Number of banks on each SDRAM	04H	0	0	0	0	0	1	0	0	4 banks
18	/CAS latency supported	06H	0	0	0	0	0	1	1	0	2, 3
19	/CS latency supported	01H	0	0	0	0	0	0	0	1	0
20	/WE latency supported	01H	0	0	0	0	0	0	0	1	0
21	SDRAM module attributes	1FH	0	0	0	1	1	1	1	1	Registered
22	SDRAM device attributes : General	0EH	0	0	0	0	1	1	1	0	
23	CL = 2 Cycle time	-A80	A0H	1	0	1	0	0	0	0	10 ns
		-A10	D0H	1	1	0	1	0	0	0	13 ns
24	CL = 2 Access time	-A80	60H	0	1	1	0	0	0	0	6 ns
		-A10	70H	0	1	1	1	0	0	0	7 ns
25-26		00H	0	0	0	0	0	0	0	0	
27	t <sub>RP</sub> (MIN.)	-A80	14H	0	0	0	1	0	1	0	20 ns
		-A10	14H	0	0	0	1	0	1	0	20 ns
28	t <sub>RRD</sub> (MIN.)	-A80	10H	0	0	0	1	0	0	0	16 ns
		-A10	14H	0	0	0	1	0	1	0	20 ns
29	t <sub>RCD</sub> (MIN.)	-A80	14H	0	0	0	1	0	1	0	20 ns
		-A10	14H	0	0	0	1	0	1	0	20 ns
30	t <sub>RAS</sub> (MIN.)	-A80	30H	0	0	1	1	0	0	0	48 ns
		-A10	32H	0	0	1	1	0	0	1	50 ns
31	Module bank density	40H	0	1	0	0	0	0	0	0	256M bytes

(2/2)

Byte No.	Function Described	Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes	
32	Command and address signal input setup time	20H	0	0	1	0	0	0	0	0	2 ns	
33	Command and address signal input hold time	10H	0	0	0	1	0	0	0	0	1 ns	
34	Data signal input setup time	20H	0	0	1	0	0	0	0	0	2 ns	
35	Data signal input hold time	10H	0	0	0	1	0	0	0	0	1 ns	
36-61		00H	0	0	0	0	0	0	0	0		
62	SPD revision	12H	0	0	0	1	0	0	1	0	1.2A	
63	Checksum for bytes 0 - 62	-A80	3AH	0	0	1	1	1	0	1	0	
		-A10	A0H	1	0	1	0	0	0	0	0	
64-71	Manufacture's JEDEC ID code											
72	Manufacturing location											
73-90	Manufacture's P/N											
91	Revision Code											
93-94	Manufacturing date											
95-98	Assembly serial number											
99-125	Mfg specific											
126	Intel specification frequency	64H	0	1	1	0	0	1	0	0	100 MHz	
127	Intel specification /CAS latency support	-A80	87H	1	0	0	0	0	1	1	1	
		-A10	85H	1	0	0	0	0	1	0	1	

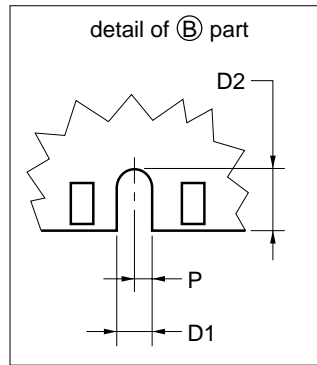
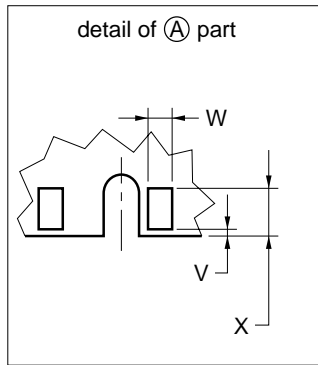
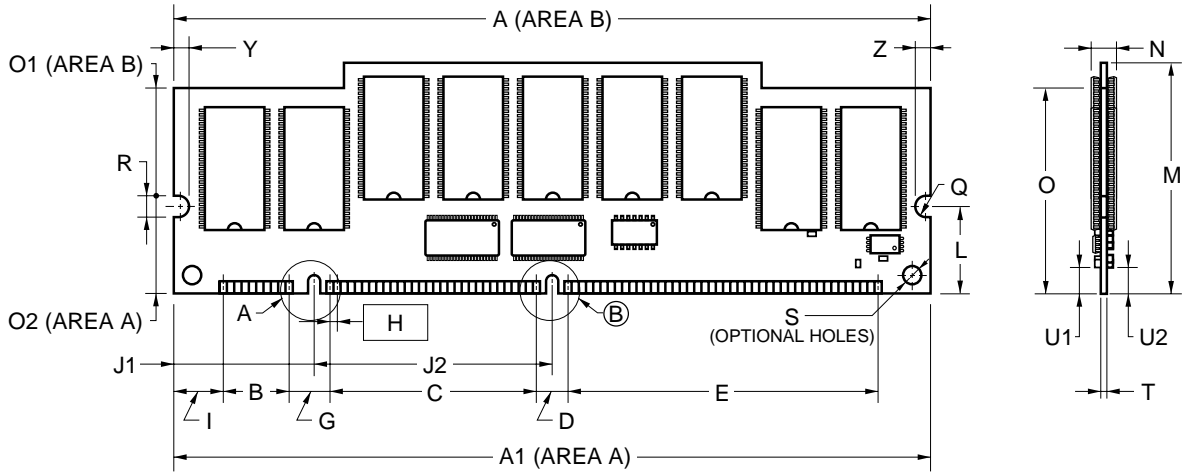
**Timing Chart**

Refer to the **SYNCHRONOUS DRAM MODULE TIMING CHART Information (M13348X)**.

Package Drawings

[ MC-4532DA726EF ]

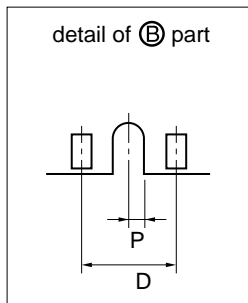
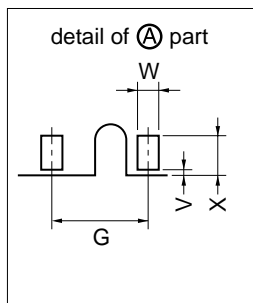
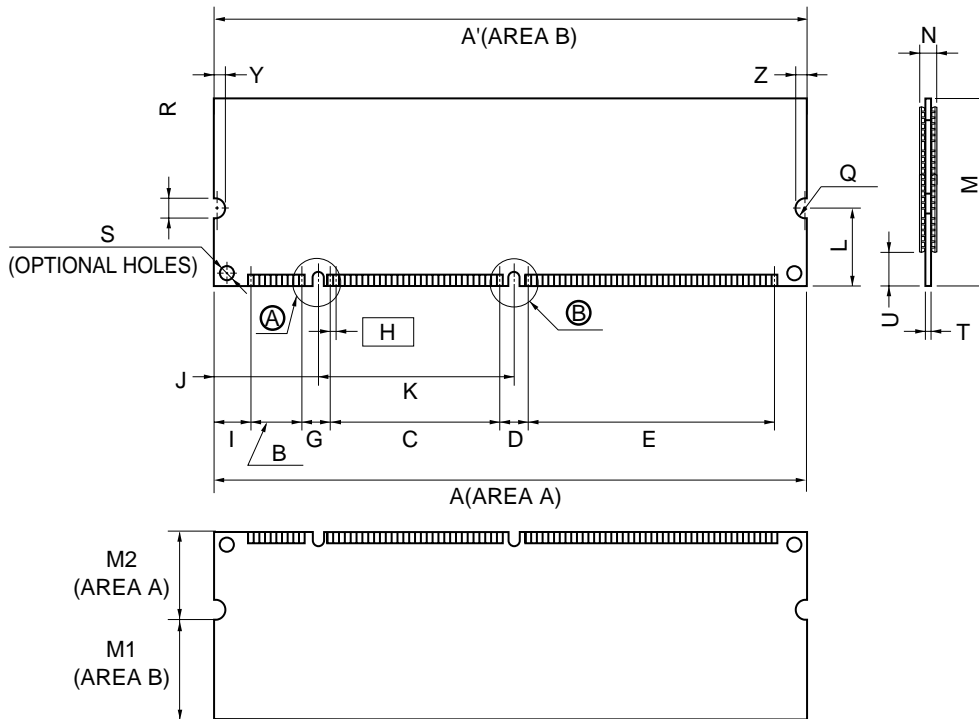
168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)



ITEM	MILLIMETERS
A	133.35
A1	133.35±0.13
B	11.43
C	36.83
D	6.35
D1	2.0
D2	3.125
E	54.61
F	5.08
G	6.35
H	1.27 (T.P.)
I	8.89
J1	24.495
J2	42.18
K1	29.97
K2	29.97
L	17.78
M	43.18±0.13
N	4.0 MAX.
O	38.1±0.13
O1	18.32
O2	19.78
P	1.0
Q	R2.0
R	4.0±0.10
S	φ 3.0
T	1.27±0.1
U1	4.0 MIN.
U2	4.0 MIN.
V	0.20±0.15
W	1.0±0.05
X	2.54±0.10
Y	3.0 MIN.
Z	3.0 MIN.

★ [ MC-4532DA726EFB ]

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)



ITEM	MILLIMETERS
A	133.35±0.13
A'	133.35
B	11.43
B'	73.406
C	36.83
C'	29.972
D	6.35
E	54.61
G	6.35
H	1.27 (T.P.)
I	8.89
J	24.495
K	42.18
L	17.78
M	43.18
M1	23.4
M2	19.78
N	4.0 MAX.
P	1.0
Q	R2.0
R	4.0±0.1
S	φ3.0
T	1.27±0.1
U	4.0 MIN.
V	0.2±0.15
W	1.0±0.05
X	2.54 MIN.
Y	3.0 MIN.
Z	3.0 MIN.

[ MEMO ]

[ MEMO ]

[ MEMO ]

**NOTES FOR CMOS DEVICES****① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

### CAUTION FOR HANDLING MEMORY MODULES

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory IC, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.

When re-packing memory modules, be sure the modules are NOT touching each other. Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

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    - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
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