PRELIMINARY

SERIAL I/O REAL TIME CLOCK

■ GENERAL DESCRIPTION

The NJU6356 series is a serial I/O Real Time Clock suitable for 4 bits microprocessor.

It contains quartz crystal oscillator, counter, shift register, voltage regulator, voltage detector and interface controller.

The NJU6356 required only 4-port of microprocessor for data transfer, and the microprocessor can receive the data at any time when the microprocessor requires.

The operating voltage is as wide as 2.0V to 5.5V, consequently, the NJU6356 can count accurate time data even if the back up period.

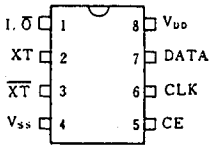
Furthermore, the long time back up is available as the current consumption during the back up period is less than 3μA.

■ PACKAGE OUTLINE

NJU6356XD

NJU6356XM

■ PIN CONFIGURATION



■ FEATURES

- Operating Voltage : 2.0 ~ 5.5V
- Low operating current : 3 μA (Typ.) at 3.0V
  4 μA (Typ.) at 5.0V
- BCD Counts of Seconds, Minutes, Hours, Date, Days of Week, Month and Year
- Required only 4-port (DATA, CLK, CE and I/O)
- Low Battery Detector (Low voltage alarm signal output)
- Automatic Leap Year Compensation
- Stabilized Oscillation.
- Package Outline --- DIP 8/DMP 8
- C-MOS Technology

■ LINE UP

VERSION	OUTPUT DATA	OSC. CAPACITOR
6356 E	Seconds, Minutes, Hours, Days of Week, Date, Month, Year	C_g/C_d on chip
F	Seconds, Minutes, Hours, Days of Week	C_g/C_d on chip
G	Seconds, Minutes, Hours, Days of Week, Date, Month, Year	C_d on chip
H	Seconds, Minutes, Hours, Days of Week	C_d on chip

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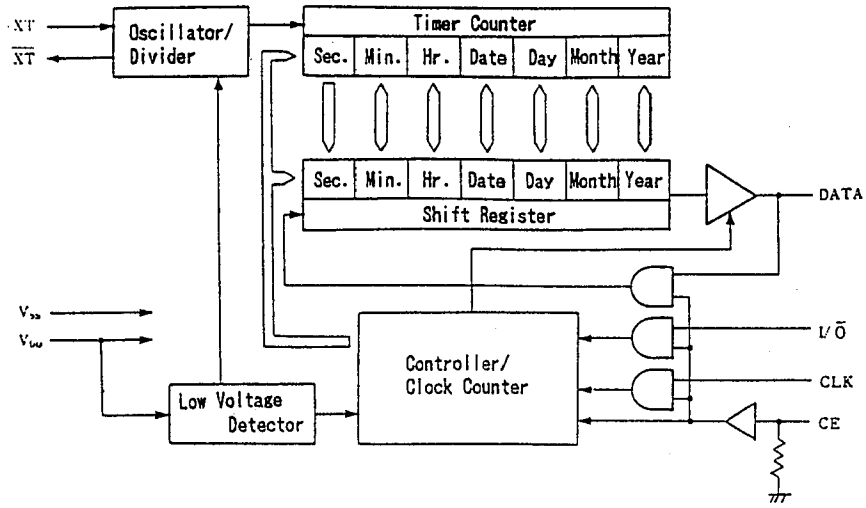
■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

NO.	SYMBOL	FUNCTION
1	I/O	Input/Output Select Terminal for DATA Terminal "H": Input, "L": Output During the CE terminal is "L", the Data terminal is high impedance.
2 3	XT $\overline{XT}$	Quartz Crystal Connecting Terminal (f=32.768kHz) Refer to the Line-Up Table for internal Cg, Cd value.
5	CE	Chip Enable Input Terminal (with pull-down resistance) "H" : Data Input/Output is available "L" : Data terminal is high impedance When the CE signal is which raising edge or falling edge, the CLK signal should be fixed to "L".
6	CLK	Clock Input Terminal The Data Input/Output is synchronized by this clock. When the CE terminal is "L" the data terminal is high impedance.
7	DATA	Serial Timer Data Input/Output
8	V_{DD}	Power Supply (+5V)
4	V_{SS}	GND

I/$\overline{O}$	CE	DATA Terminal
H	H	Input
L	H	Output
H	L	High-Impedance
L	L	High-Impedance

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■ FUNCTIONAL DESCRIPTION

1. Timer Data structure

The NJU6356 using BCD code which consisting of 4 bits per 1 digit.

The calendar function including the last date of each month and the leap year calculation is executed automatically.

The unused bit for the timer data is "0".

< Timer Data Bit Map >

	MSB							LSB	Range
Second	0	S6	S5	S4	S3	S2	S1	S0	0 - 59
Minute	0	m6	m5	m4	m3	m2	m1	m0	0 - 59
Hour	0	0	H5	H4	H3	H2	H1	H0	0 - 23
Days of Week					0	W2	W1	W0	1 - 7
Date	0	0	D5	D4	D3	D2	D1	D0	1 - 31
Month	0	0	0	M4	M3	M2	M1	M0	1 - 12
Year	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	0 - 99

2. Timer Data Reading

When the I/$\overline{O}$ terminal is "L" and the CE terminal is "H", timer data can read out. The output is LSB first and the output data strings (depending on the version) is shown below.

The timer data is transferred from timer counter to shift register at rising edge of the chip enable on the CE terminal, and output the LSB of the timer data from the Data terminal.

Afterward the timer data in the shift register shift by synchronized at the falling edge of clock signal on CLK terminal and output from the DATA terminal.

If the timer data is updated in the data output, there are one second difference between timer data and output data.

< E & G Version >

Year	Month	Date	Day	Hour	Minute	Second

The data is read out from LSB of Year, and first 52-bit is effective.

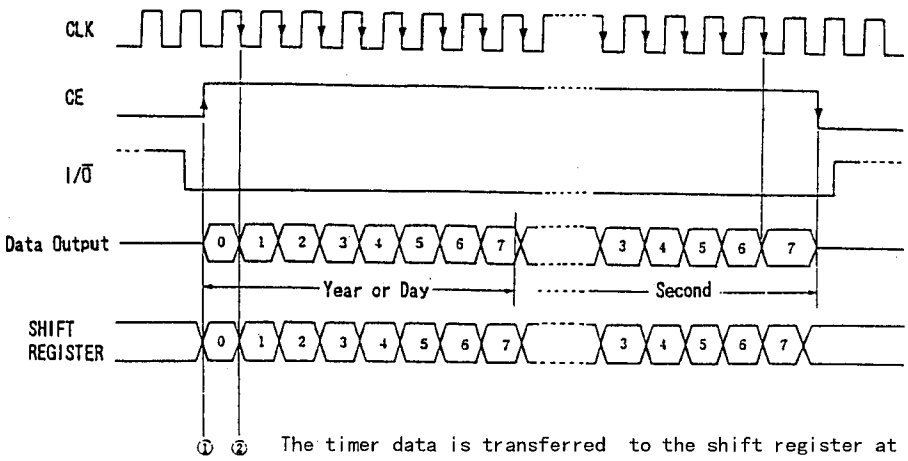
< F & H Version >

Day	Hour	Minute	Second

The data is read out from LSB of Days of Week, and first 28-bit is effective.

If the low voltage detector detect the low battery, $(EE)_H$ is written into each digit of timer data and read out. The code of $(EE)_H$ is a warning for the data broken.

< Read-Out Timing >



The timer data is transferred to the shift register at rising edge of the CE(①) and LSB of the timer data is output to the Data terminal. Afterward the timer data in the shift register shift by synchronized at falling edge of the CLK(②) then output to the Data terminal time-to-time.

note) When the CE signal is which raising edge or falling edge, the CLK signal should be fixed to "L". And so, before the CE signal is raised, the I/$\overline{O}$ signal should be fixed to "L".

3. Timer Data Writing

When both of I/$\overline{O}$ terminal and CE terminal are "H", update is stopped, Oscillator divider is cleared, and the timer data can be written to the NJU6356. The timer data is written into the shift register from the Data terminal by synchronized with rising edge of the clock signal input from the CLK terminal, and the data is transferred from the shift register to the timer counter by synchronized with falling edge of the CE signal. In this time the second-counter is cleared to "0", and the oscillator divider start the operation. The input data strings are LSB first of each digit as shown below (the data format is depend on the version):

< E & G Version >

Year	Month	Date	Day	Hour	Minute

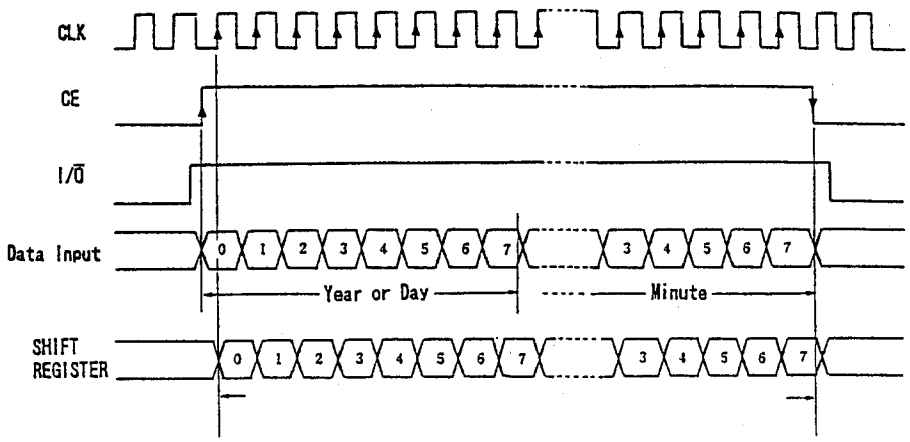
The data is written from LSB of Year and last 44-bit is effective.

< F & H Version >

Day	Hour	Minute

The data is written from LSB of Days of Week and last 20-bit is effective.

< Write-Down Timing >



The data is input into the shift register at rising edge of the CLK.

The data in the shift register is transferred to the timer counter at this falling edge of the CE, then the oscillator divider start the operation.

note) When the CE signal is which raising edge or falling edge, the CLK signal should be fixed to "L". And so, before the CE signal is raised, the I/$\overline{O}$ signal should be fixed to "H".

4. Low Voltage Detector

The NJU6356 series incorporate the low battery detector. If the supply voltage reduce to the detection level, $(EE)_H$ is written into each digit of the shift register as warning code for the CPU.

5. Data Access

The NJU6356 series can operate from 2.0V to 5.5V. However, it is not allow the data access out of the range of 5V±10%. It may be broken the data unless 5V±10%.

Thus, when the data access, CE terminal should be "H" after the power supply rise to 5V±10%, then start the operation.

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	- 0.3 ~ + 6.0	V
Input Voltage	V_{IN}	V_{SS}-0.3 ~ V_{DD}+0.3	V
Power Dissipation	P_D	250 (DIP) 200 (DMP)	mW
Operating Temperature	T_{opr}	- 30 ~ + 80	°C
Storage Temperature	T_{stg}	- 55 ~ +150	°C

■ ELECTRICAL CHARACTERISTICS

DC Characteristics (V_{DD}=2.0V, Ta=25°C)

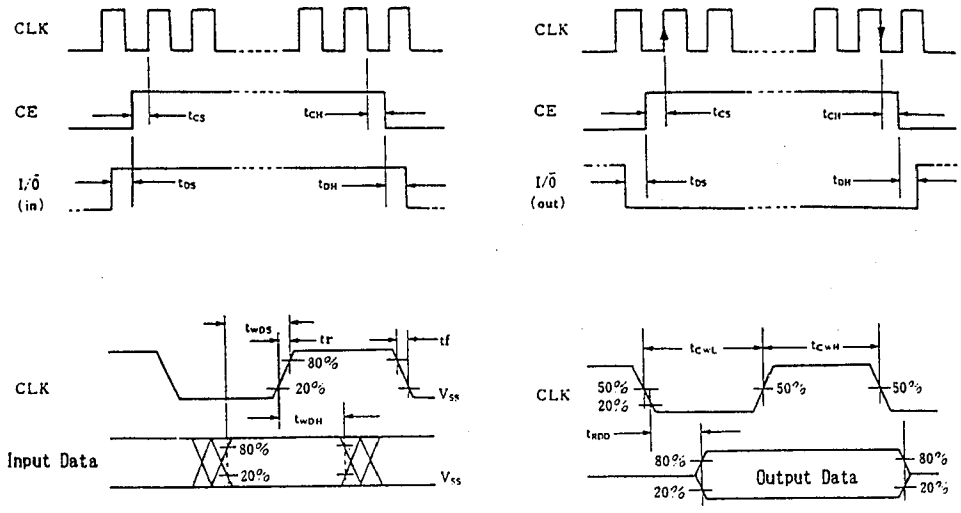
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Current	I_{DD}	XT=32.768kHz, CE=0V		3.0	4.0	μA
LowBattery Detect Voltage	V_{DET}		1.1		1.7	V

DC Characteristics (V_{DD}=5.0V±10%, Ta=25°C)

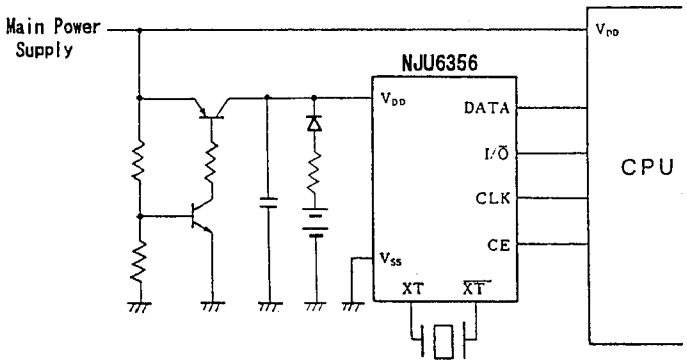
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage	V_{DD}		4.5		5.5	V
Operating Current	I_{DD}	XT=32.768kHz, CE=0V		4.0	15	μA
3-st Leakage Current	I_{TSL}	DATA Terminal (CE=0V)	-2.0		2.0	μA
Input Leakage Current	I_{IL}	I/$\overline{O}$, CLK Terminals	-1.0		1.0	μA
Input Current	I_{CE}	CE Terminal (CE=V_{DD})			20	μA
Input Voltage	V_{IH}	I/$\overline{O}$, CE, CLK, DATA Terminals	V_{DD}x0.8		V_{DD}	V
	V_{IL}	I/$\overline{O}$, CE, CLK, DATA Terminals	V_{SS}		V_{DD}x0.2	
Output Voltage	V_{OH}	DATA Terminal (I_{OH}=-0.4mA)	4.1			V
	V_{OL}	DATA Terminal (I_{OL}=1.0mA)			0.4	

AC CHARACTERISTICS (V_{DD}=5.0V±10%, Ta=25°C, C_L=50pF)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
CLK Pulse "H" Period	t_{CWH}		0.47		5000	μs
CLK Pulse "L" Period	t_{CWL}		0.47		5000	μs
CE Set-up Time Before CLK Rising	t_{CS}		470			ns
CE Hold Time After CLK Falling	t_{CH}		20			ns
I/$\overline{O}$ Set-up Time Before CLK Rising	t_{DS}		60			ns
I/$\overline{O}$ Hold Time After CLK Falling	t_{DH}		20			ns
Write-Down Data Set-Up Time	t_{WDS}		100			ns
Write-Down Data Hold Time	t_{WDH}		20			ns
Data Delay Time After CLK Falling	t_{RDD}				200	ns
Rise/Fall Time	t_{RF}				50	ns



■ APPLICATION CIRCUIT



MEMO