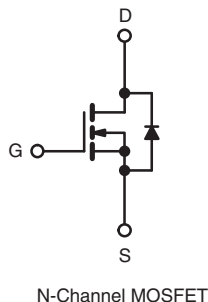
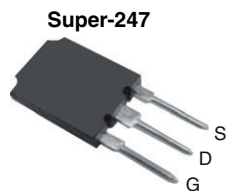


D Series Power MOSFET



FEATURES

- Optimal design
 - Low area specific on-resistance
 - Low input capacitance (C_{iss})
 - Reduced capacitive switching losses
 - High body diode ruggedness
 - Avalanche energy rated (U_{IS})
- Optimal efficiency and operation
 - Low cost
 - Simple gate drive circuitry
 - Low figure-of-merit (FOM): $R_{on} \times Q_g$
 - Fast switching
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

PRODUCT SUMMARY

V_{DS} (V) at T_J max.	550	
$R_{DS(on)}$ max. at 25 °C (Ω)	$V_{GS} = 10$ V	0.130
Q_g max. (nC)	125	
Q_{gs} (nC)	23	
Q_{gd} (nC)	37	
Configuration	Single	

APPLICATIONS

- Consumer electronics
 - Displays (LCD or Plasma TV)
- Server and telecom power supplies
 - SMPS
- Industrial
 - Welding, induction heating, motor drives
- Battery chargers

ORDERING INFORMATION

Package	Super-247
Lead (Pb)-free and halogen-free	SiHS36N50D-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	500	V
Gate-source voltage	V_{GS}	± 30	
Gate-source voltage AC ($f > 1$ Hz)		30	
Continuous drain current ($T_J = 150$ °C)	V_{GS} at 10 V	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed drain current ^a	I_{DM}	112	
Linear derating factor		3.6	W/°C
Single pulse avalanche energy ^b	E_{AS}	332	mJ
Maximum power dissipation	P_D	446	W
Operating junction and storage temperature range	T_J, T_{stg}	- 55 to + 150	°C
Drain-source voltage slope	dV/dt	24	V/ns
Reverse diode dV/dt ^d		0.1	
Soldering recommendations (peak temperature)	for 10 s	300 °C	°C

Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 50$ V, starting $T_J = 25$ °C, $L = 2.3$ mH, $R_g = 25$ Ω , $I_{AS} = 17$ A
- 1.6 mm from case
- $I_{SD} \leq I_D$, starting $T_J = 25$ °C

**THERMAL RESISTANCE RATINGS**

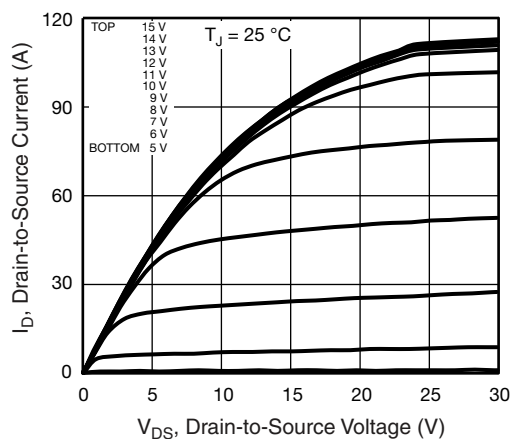
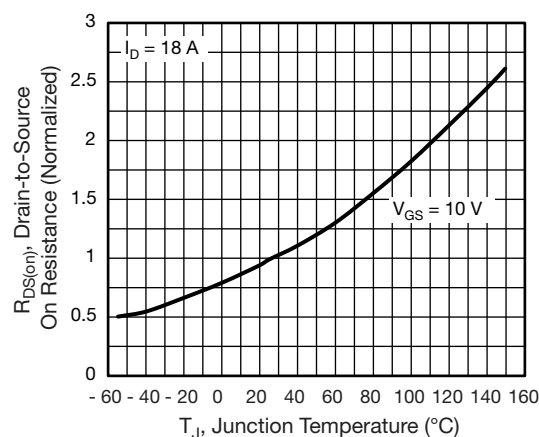
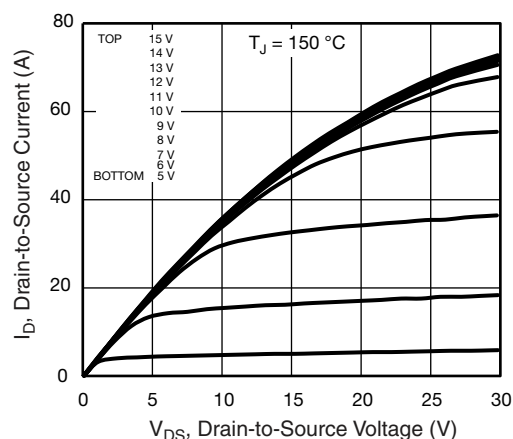
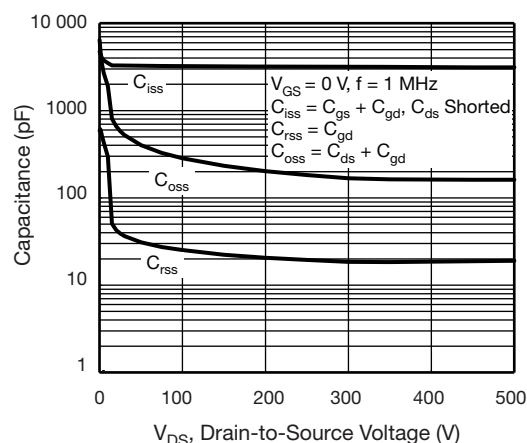
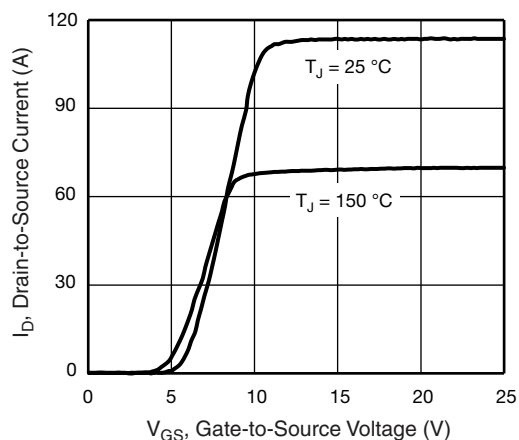
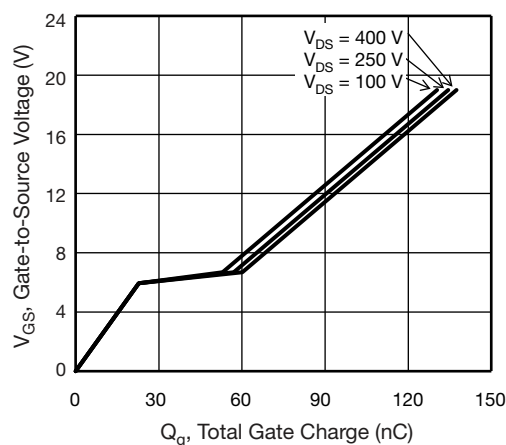
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	40	°C/W
Maximum junction-to-case (drain)	R_{thJC}	-	0.28	

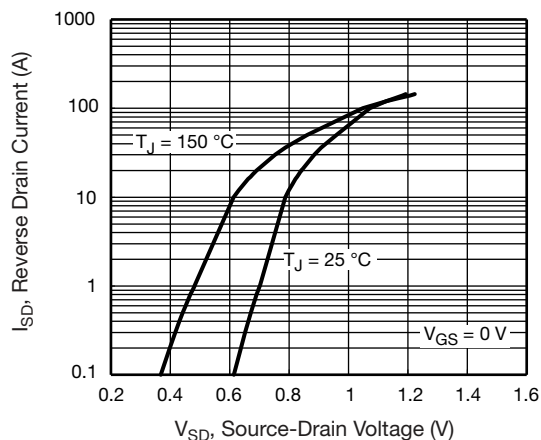
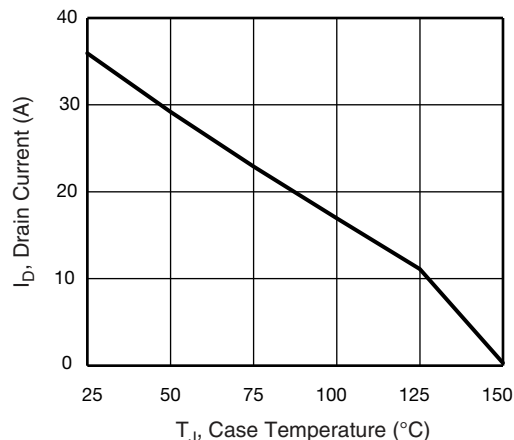
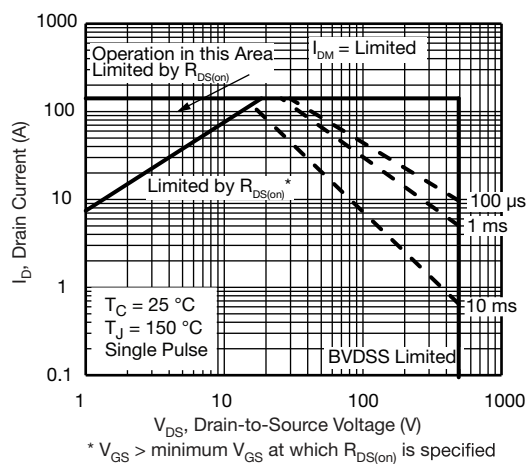
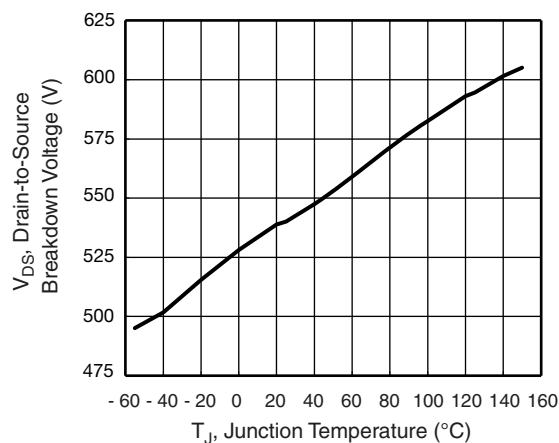
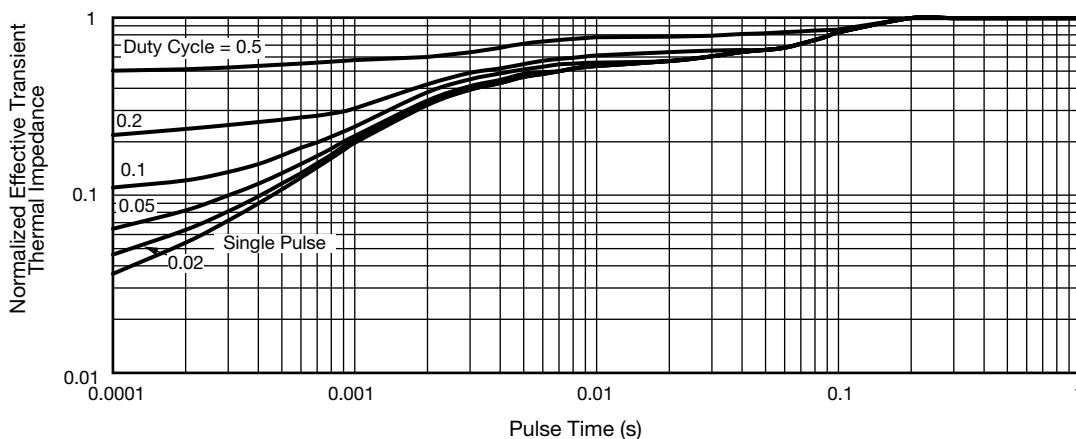
SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

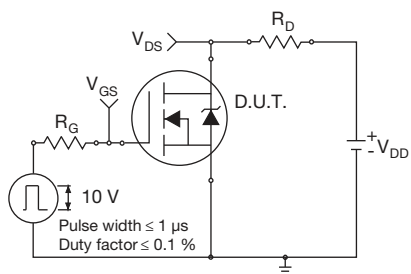
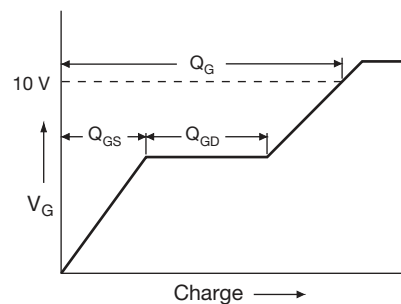
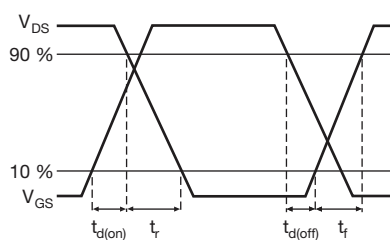
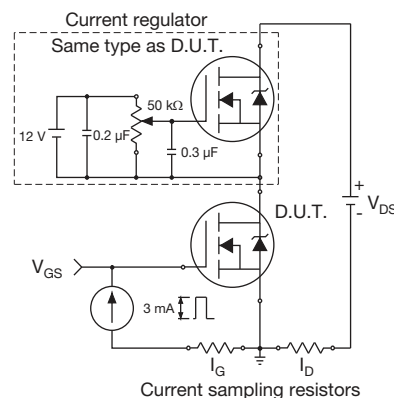
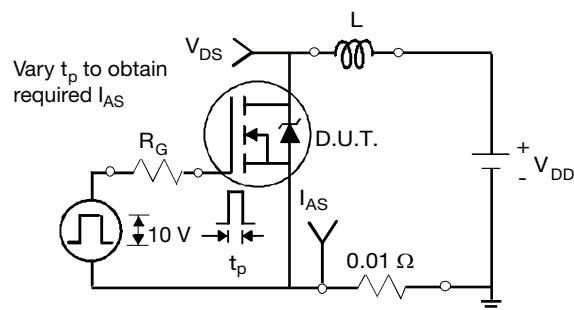
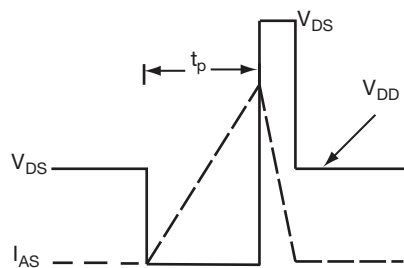
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		500	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 250 μA		-	0.52	-	V/°C
Gate threshold voltage (N)	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		3.0	-	5.0	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 30 V		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 500 V, V _{GS} = 0 V		-	-	1	μA
		V _{DS} = 400 V, V _{GS} = 0 V, T _J = 125 °C		-	-	10	
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 18 A	-	0.105	0.130	Ω
Forward transconductance ^a	g _{fs}	V _{DS} = 50 V, I _D = 18 A		-	12.8	-	S
Dynamic							
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 100 V, f = 1 MHz		-	3233	-	pF
Output capacitance	C _{oss}			-	285	-	
Reverse transfer capacitance	C _{rss}			-	25	-	
Effective output capacitance, energy related ^a	C _{o(er)}	V _{GS} = 0 V, V _{DS} = 0 V to 400 V		-	240	-	
Effective output capacitance, time related ^b	C _{o(tr)}			-	352	-	
Total gate charge	Q _g	V _{GS} = 10 V	I _D = 18 A, V _{DS} = 400 V	-	83	125	nC
Gate-source charge	Q _{gs}			-	23	-	
Gate-drain charge	Q _{gd}			-	37	-	
Turn-on delay time	t _{d(on)}	V _{DD} = 400 V, I _D = 18 A, V _{GS} = 10 V, R _g = 9.1 Ω		-	33	66	ns
Rise time	t _r			-	89	134	
Turn-off delay time	t _{d(off)}			-	79	119	
Fall time	t _f			-	68	102	
Gate input resistance	R _g	f = 1 MHz, open drain		-	1.8	-	Ω
Drain-source body diode characteristics							
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	36	A
Pulsed diode forward current	I _{SM}			-	-	144	
Diode forward voltage	V _{SD}	T _J = 25 °C, I _S = 18 A, V _{GS} = 0 V		-	-	1.2	V
Reverse recovery time	t _{rr}	T _J = 25 °C, I _F = I _S = 18 A, dI/dt = 100 A/μs, V _R = 20 V		-	490	-	ns
Reverse recovery charge	Q _{rr}			-	8.2	-	μC
Reverse recovery current	I _{RRM}			-	31	-	A

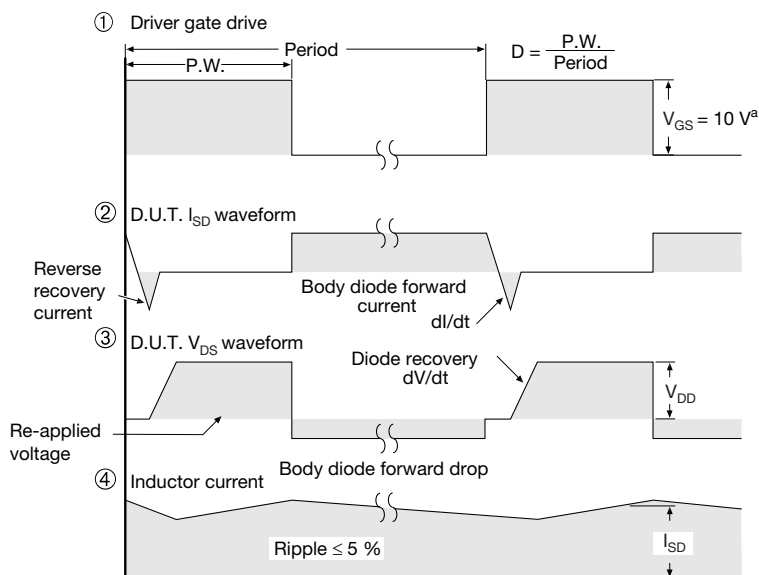
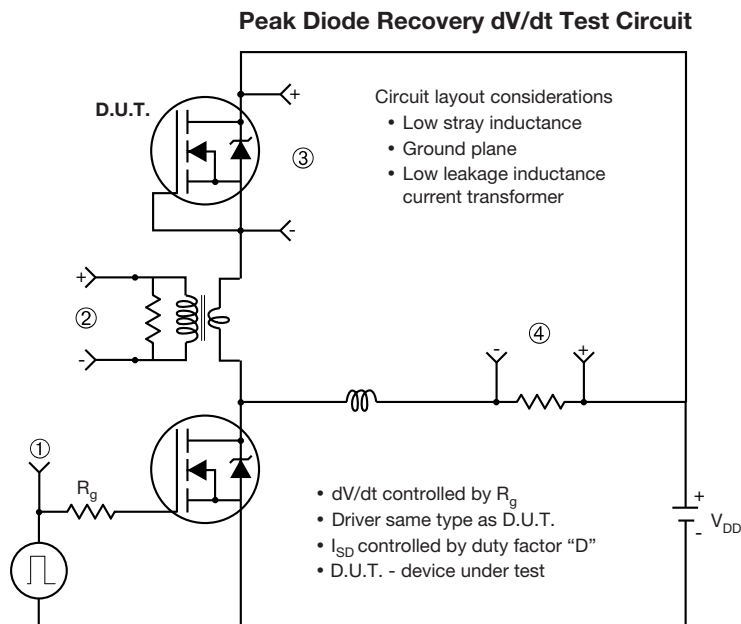
Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}
b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 4 - Normalized On-Resistance vs. Temperature

Fig. 2 - Typical Output Characteristics

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 3 - Typical Transfer Characteristics

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage


Fig. 7 - Typical Source-Drain Diode Forward Voltage

Fig. 9 - Maximum Drain Current vs. Case Temperature

Fig. 8 - Maximum Safe Operating Area

Fig. 10 - Temperature vs. Drain-to-Source Voltage

Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case


Fig. 12 - Switching Time Test Circuit

Fig. 16 - Basic Gate Charge Waveform

Fig. 13 - Switching Time Waveforms

Fig. 17 - Gate Charge Test Circuit

Fig. 14 - Unclamped Inductive Test Circuit

Fig. 15 - Unclamped Inductive Waveforms


Note

a. $V_{GS} = 5 V$ for logic level devices

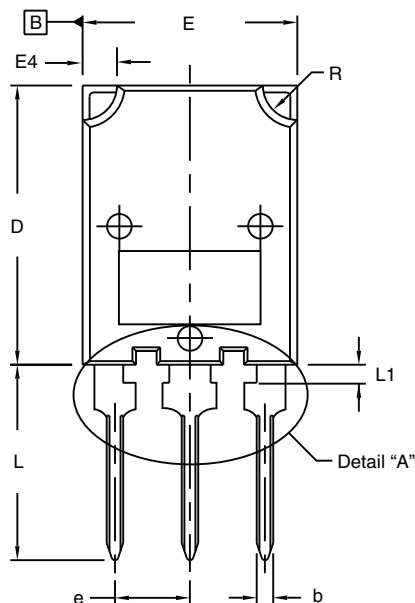
Fig. 18 - For N-Channel

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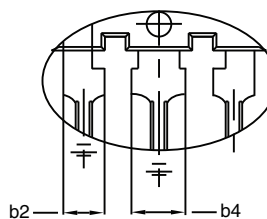
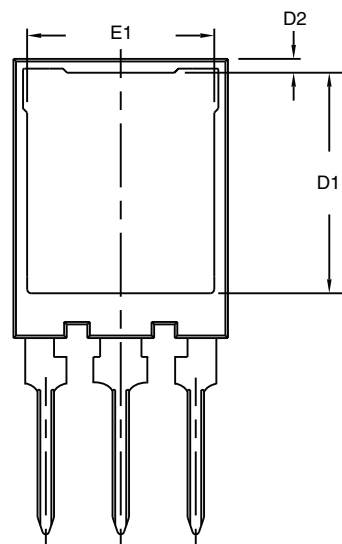
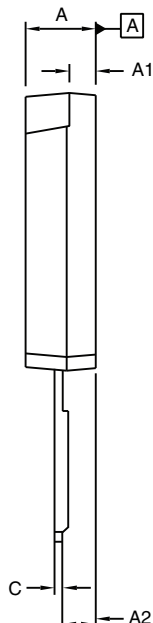
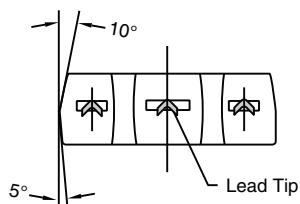


TO-274AA (High Voltage)

VERSION 1: FACILITY CODE = Y



⌀ 0.10 (0.25) Ⓜ B A Ⓜ



Detail "A"
Scale: 2:1

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.70	5.30	0.185	0.209
A1	1.50	2.50	0.059	0.098
A2	2.25	2.65	0.089	0.104
b	1.30	1.60	0.051	0.063
b2	1.80	2.20	0.071	0.087
b4	3.00	3.25	0.118	0.128
c ⁽¹⁾	0.38	0.89	0.015	0.035
D	19.80	20.80	0.780	0.819

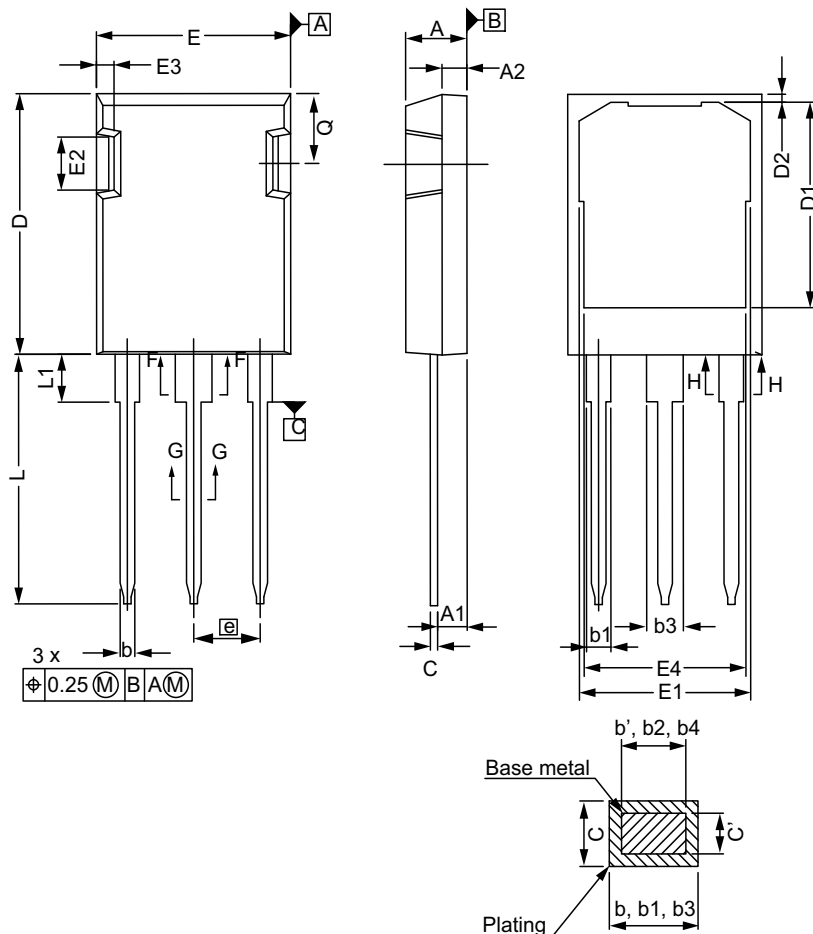
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	15.50	16.10	0.610	0.634
D2	0.70	1.30	0.028	0.051
E	15.10	16.10	0.594	0.634
E1	13.30	13.90	0.524	0.547
e	5.45 BSC		0.215 BSC	
L	13.70	14.70	0.539	0.579
L1	1.00	1.60	0.039	0.063
R	2.00	3.00	0.079	0.118

Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994
- Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outer extremes of the plastic body
- Outline conforms to JEDEC® outline to TO-274AA
- ⁽¹⁾ Dimension measured at tip of lead



VERSION 2: FACILITY CODE = N



SECTION "F-F", "G-G" AND "H-H"
SCALE: NONE

	MILLIMETERS	
DIM.	MIN.	MAX.
A	4.83	5.21
A1	2.29	2.54
A2	1.91	2.16
b'	1.07	1.28
b	1.07	1.33
b1	1.91	2.41
b2	1.91	2.16
b3	2.87	3.38
b4	2.87	3.13
c'	0.55	0.65
c	0.55	0.68
D	20.80	21.10

	MILLIMETERS	
DIM.	MIN.	MAX.
D1	16.25	17.65
D2	0.50	0.80
E	15.75	16.13
E1	13.10	14.15
E2	3.68	5.10
E3	1.00	1.90
E4	12.38	13.43
e	5.44 BSC	
N	3	
L	19.81	20.32
L1	3.70	4.00
Q	5.49	6.00

ECN: E20-0538-Rev. C, 19-Oct-2020
DWG: 5975

Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994
- Outline conforms to JEDEC® outline to TO-274AD
- Dimensions are measured in mm, angles are in degree
- Metal surfaces are tin plated, except area of cut



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