# MH51208ATN-70L,-85L,-10L,-12L/ MH51208ATN-70H,-85H,-10H,-12H

## 4194304-BIT(524288-WORD BY 8-BIT)CMOS STATIC RAM

### DESCRIPTION

The MH51208ATN is a 4194304-bits CMOS static RAM module organized as 524288-words by 8-bits. It consists of four industry standard 1M × 8 static RAMs.

The stand-by current is low enough for a battery backup application. It is mounted a flat package on a 64-pin single in line package.

### FEATURES

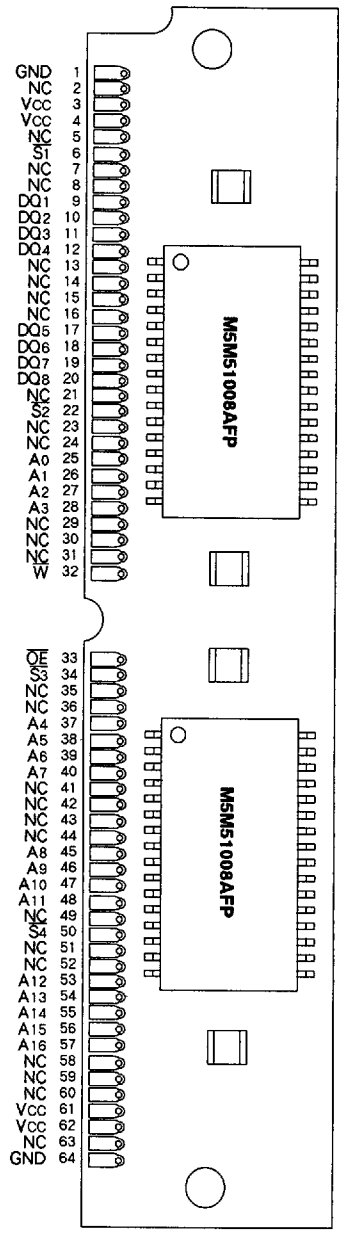
| Type name | Access time (max) | Power supply current | |
|---|---|---|---|
| | | Active (max) | Stand-by (max) |
| MH51208ATN-70L<br>MH51208ATN-85L<br>MH51208ATN-10L<br>MH51208ATN-12L | 70ns<br>85ns<br>100ns<br>120ns | 79mA | 200 μA<br>Vcc = 3.0V |
| MH51208ATN-70H<br>MH51208ATN-85H<br>MH51208ATN-10H<br>MH51208ATN-12H | 70ns<br>85ns<br>100ns<br>120ns | | 40 μA<br>Vcc = 3.0V |

- 64pins single in-line package
- Single +5V power supply
- No clocks, No refresh
- Data-hold on +2V power supply
- Directly TTL compatible : all inputs and outputs
- Thress-state outputs : OR-tie capability
- Simple memory expansion by $\overline{S}$
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O
- Gold plating contact

### APPLICATION

Small capacity memory units

### PIN CONFIGURATION(TOP VIEW) (Both side)




Outline 64N9G

NC : NO CONNECTION





MITSUBISHI ELECTRIC

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### FUNCTION

The operation mode of the MH51208ATN is determinde by a combination of the device control inputs $\overline{S}$, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low levlel $\overline{S}$. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S}$, whichever occurs first, requiring the set-up and hold time ralative to these edge to be maintained. The output enable $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bau contention problem in the write cycle is eliminated.

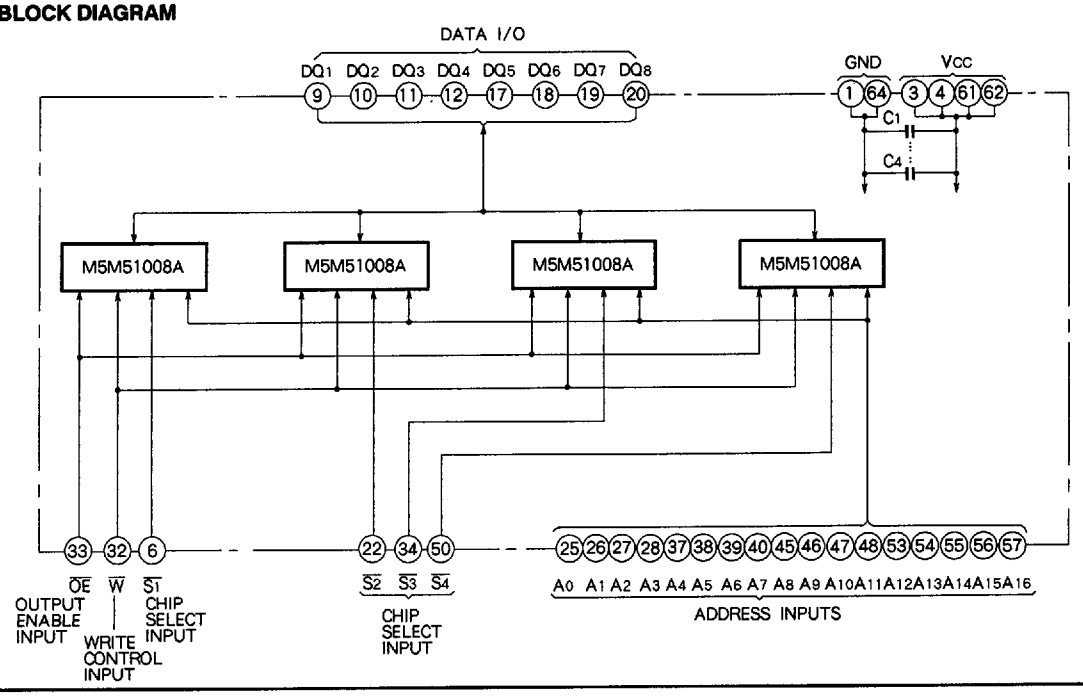
A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}$ are in an active state.

When setting $\overline{S}$ at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S}$. The power supply current is reduced as low as the stand-by current which is specified as $I_{CC3}$ or $I_{CC4}$, and the memory data can be held + 2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

### FUNCTION TABLE

| $\overline{S}$ | $\overline{W}$ | $\overline{OE}$ | Mode | DQ | Icc |
|---|---|---|---|---|---|
| H | X | X | Non selection | High-impedance | Stand-by |
| L | L | X | Write | $D_{IN}$ | Active |
| L | H | L | Read | $D_{OUT}$ | Active |
| L | H | H | | High-impedance | Active |

### BLOCK DIAGRAM



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## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Ratings | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | Wtith respect to GND | −0.3~7 | V |
| $V_I$ | Input voltage | | −0.3*~$V_{CC}$+0.3 | V |
| $V_O$ | Output voltage | | 0~$V_{CC}$ | V |
| $P_d$ | Power dissipation | Ta = 25℃ | 700 | mW |
| $T_{opr}$ | Operating temperature | | 0~70 | ℃ |
| $T_{stg}$ | Storage temperature | | −40~125 | ℃ |

* −3.0V incase of AC (Pulse width ≦ 50ns)

## DC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, $V_{CC}$ = 5V ± 10%, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits Min | Limits Typ | Limits Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High input voltage | | | 2.2 | | $V_{CC}$+0.3 | V |
| $V_{IL}$ | Low input voltage | | | −0.3* | | 0.8 | V |
| $V_{OH}$ | High output voltage | $I_{OH}$ = −1mA | | 2.4 | | | V |
| $V_{OL}$ | Low output voltage | $I_{OL}$ = 2mA | | | | 0.4 | V |
| $I_I$ | Input current | $V_I$ = 0~$V_{CC}$ | | | | ±4 | μA |
| $I_O$ | Output current | $\overline{S}$ = $V_{IH}$ or $\overline{OE}$ = $V_{IH}$, $V_{I/O}$ = 0~$V_{CC}$ | | | | ±4 | μA |
| $I_{CC1}$ | Active supply current (AC. MOS level) | $\overline{S}$ ≦ 0.2V, output open other input ≦ 0.2Vor ≧ $V_{CC}$ − 0.2V Min, cycle | | | 47 | 79 | mA |
| $I_{CC2}$ | Active supply current (AC. TTL level) | $\overline{S}$ = $V_{IL}$, output open other input = $V_{IL}$ or $V_{IH}$ Min, cycle | | | 49 | 79 | mA |
| $I_{CC3}$ | Stand-by supply current | $\overline{S}$ ≧ $V_{CC}$ − 0.2V, Other inputs = 0~$V_{CC}$ | -L | | | 400 | μA |
| | | | -H | | 4.0 | 80 | |
| $I_{CC4}$ | Stand-by supply current | $\overline{S}$ = $V_{IH}$, Other inputs = 0~$V_{CC}$ | | | | 12 | mA |
| $C_{I(A)}$ | Input capacitance, Address input | f = 1MHz $V_I$ = GND $V_i$ = 25mVrms $V_O$ = GND $V_o$ = 25mVrms | | | | 45 | pF |
| $C_{I(W)}$ | Input capacitance, Write control input | | | | | 45 | pF |
| $C_{I(OE)}$ | Input capacitance, $\overline{OE}$ input | | | | | 45 | pF |
| $C_{I(S)}$ | Input capacitance, Chip select input | | | | | 20 | pF |
| $C_{(DQ)}$ | Input output capacitance, DQ | | | | | 55 | pF |

Note 1 : Direction for current flowing into an IC is positive (no mark)
2 : Typical value is $V_{CC}$ = 5V, Ta = 25℃

## AC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, $V_{CC}$ = 5V ± 10%, unless otherwise noted)

### (1) MEASUREMENT CONDITIONS

Input pulse level ····· $V_{IH}$ = 2.4V, $V_{IL}$ = 0.6V
Input rise and fall time ····· 5ns
Reference level ····· $V_{OH}$ = $V_{OL}$ = 1.5V
Transition is measured ±500mV from steady state voltage.(for $t_{en}$, $t_{dis}$)
Output loads ····· Fig.1, $C_L$ = 100pF (-85L, -10L, -12L, -85H, -10H, -12H)
$C_L$ = 30pF (-70L, -70H)
$C_L$ = 5pF (for $t_{en}$, $t_{dis}$)

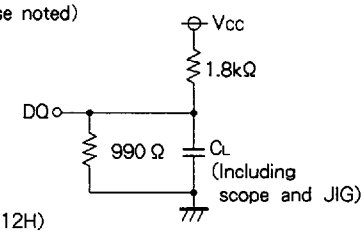


Fig. 1 Output load

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## (2) READ CYCLE

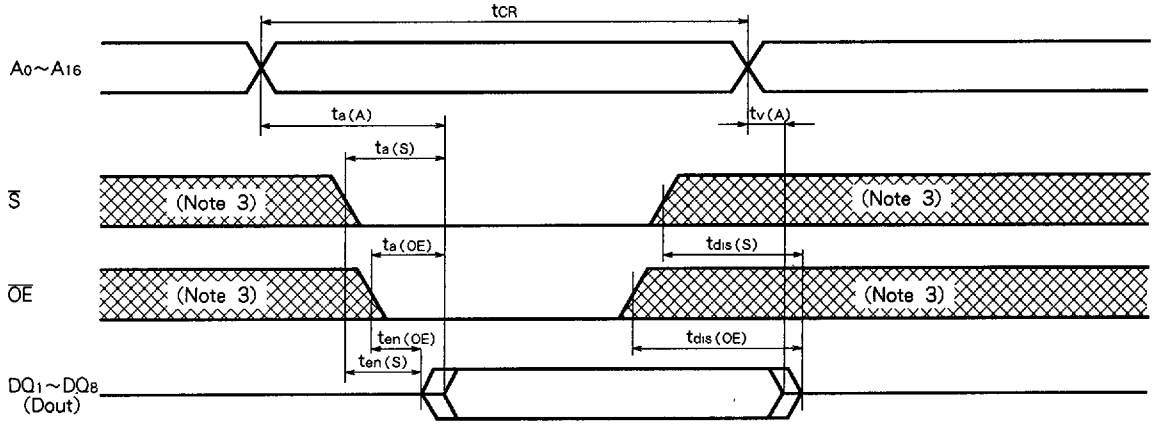
| Symbol | Parameter | Limits | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | MH51208ATN-70 | | MH51208ATN-85 | | MH51208ATN-10 | | MH51208ATN-12 | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| tCR | Read cycle time | 70 | | 85 | | 100 | | 120 | | ns |
| ta(A) | Address access time | | 70 | | 85 | | 100 | | 120 | ns |
| ta(S) | Chip select access time | | 70 | | 85 | | 100 | | 120 | ns |
| ta(OE) | Output enable access time | | 35 | | 45 | | 50 | | 60 | ns |
| tdis(S) | Output disable time after $\overline{S}$ high | | 25 | | 30 | | 35 | | 40 | ns |
| tdis(OE) | Output disable time after $\overline{OE}$ high | | 25 | | 30 | | 35 | | 40 | ns |
| ten(S) | Output enable time after $\overline{S}$ low | 10 | | 10 | | 10 | | 10 | | ns |
| ten(OE) | Output enable time after $\overline{OE}$ low | 5 | | 5 | | 5 | | 5 | | ns |
| tV(A) | Data valid time after address change | 10 | | 10 | | 10 | | 10 | | ns |

## (3) WRITE CYCLE

| Symbol | Parameter | Limits | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | MH51208ATN-70 | | MH51208ATN-85 | | MH51208ATN-10 | | MH51208ATN-12 | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| tCW | Write cycle time | 70 | | 85 | | 100 | | 120 | | ns |
| tW(W) | Wtire pulse width | 55 | | 65 | | 75 | | 85 | | ns |
| tsu(A) | Address set up time | 0 | | 0 | | 0 | | 0 | | ns |
| tsu(A-WH) | Address set up time with respect to $\overline{W}$ high | 65 | | 75 | | 85 | | 100 | | ns |
| tsu(S) | Chip select set up time | 65 | | 75 | | 85 | | 100 | | ns |
| tsu(D) | Data set up time | 30 | | 35 | | 40 | | 45 | | ns |
| th(D) | Data hold time | 0 | | 0 | | 0 | | 0 | | ns |
| trec(W) | Wtite recovery time | 0 | | 0 | | 0 | | 0 | | ns |
| tdis(W) | Output disable time after $\overline{W}$ low | | 25 | | 30 | | 35 | | 40 | ns |
| tdis(OE) | Output disable time after $\overline{OE}$ high | | 25 | | 30 | | 35 | | 40 | ns |
| ten(W) | Output enable time after $\overline{W}$ high | 5 | | 5 | | 5 | | 5 | | ns |
| ten(OE) | Output enable time after $\overline{OE}$ low | 5 | | 5 | | 5 | | 5 | | ns |

## (4) TIMING DIAGRAM

**Read cycle**




$\overline{W}$ = "H"level

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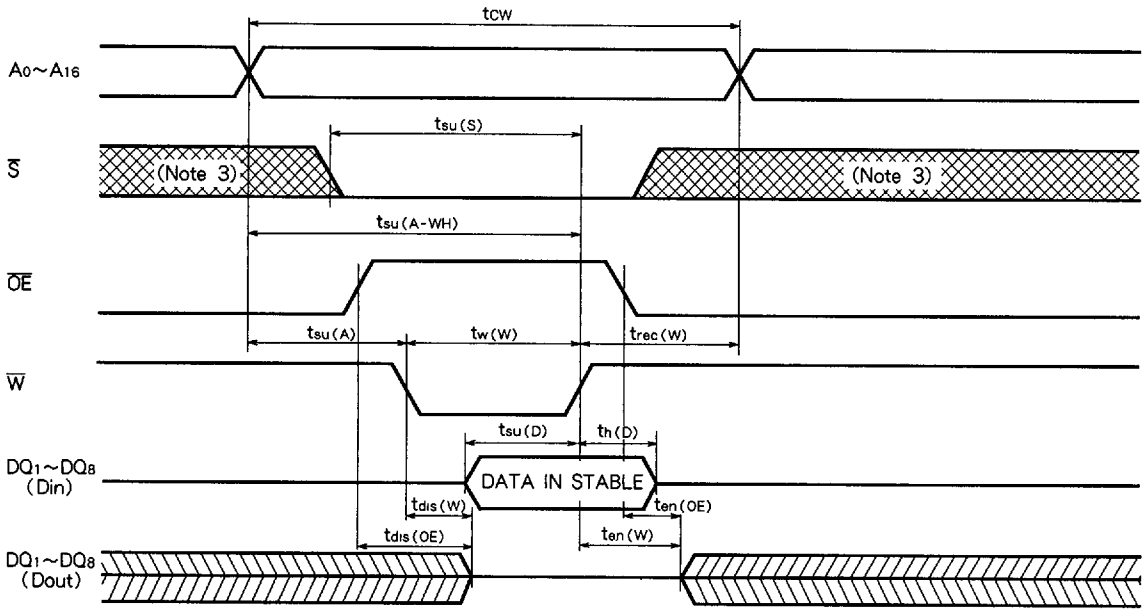
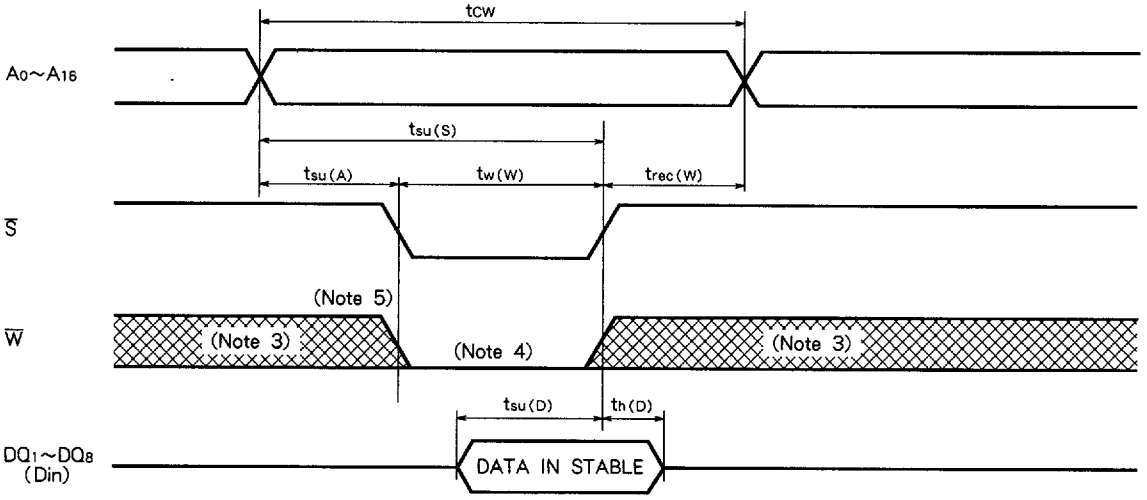
**Write cycle ($\overline{W}$ control)**




**Write cycle ($\overline{S}$ control)**




Note 3 : Hatching indicates the stage is don't care.
4 : Writing is executed in overlap of $\overline{S}$ and $\overline{W}$ low.
5 : If $\overline{W}$ goes low simultaneously with or prior to $\overline{S}$, the output remains in the high, impedance state.
6 : Don't active inverted phase signal externally when DQ pin is in output mode.

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**POWER DOWN CHARACTERISTICS** (Ta = 0~70℃, unless otherwise noted)

**ELECTRICAL CHARACTERISTICS**

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{CC(PD)}$ | Power down supply voltage | | | 2 | | | V |
| $V_{I(S)}$ | Chip select input $\overline{S}$ | 2.2V ≦ $V_{CC(PD)}$ | | 2.2 | | | V |
| | | 2V ≦ $V_{CC(PD)}$ ≦ 2.2V | | | $V_{CC(PD)}$ | | |
| $I_{CC(PD)}$ | Power down supply current | $V_{CC}$ = 3V, $\overline{S}$ ≧ $V_{CC}$ − 0.2V, Other inputs = 0~3V | -L | | | 200 | μA |
| | | | -H | | | 40 (Note 7) | |

* When $\overline{S}$ is at 2.2V ($V_{IH}$ min) and supply voltage is at any level between 4.5V and 2.4V, supply current is defined as $I_{CC4}$.
Note 7 : $I_{CC(PD)}$ = 4 μA in case of Ta = 25℃

**TIMING REQUIREMENTS** (Ta = 0~70℃, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $t_{su(PD)}$ | Power down setup time | | 0 | | | ns |
| $t_{rec(PD)}$ | Power down recovery time | | 5 | | | ms |

**POWER DOWN CHARACTERISTICS**

**$\overline{S}$ control**