S1201

Congo Device Specification

Revision NC

August 2, 2000

CONGO

DEVICE SPECIFICATION

STS-12C/STS-3C POS/ATM SONET MAPPER

Features

- Processes SONET/SDH STS-12c/(STM-4/AU-4-4c) or STS-3c/STM-1 data streams with full duplex mapping of ATM cells or packets (PPP) into SONET/SDH payloads.
- Terminates & generates SONET/SDH section, line, & path layers, with transport/section E1, E2, F1 and DCC overhead interfaces in both transmit and receive directions.
- Provides an 8-bit parallel line-side interface operating at 19.44/77.76 MHz, and a 16-bit Utopia Level 2 or POS-PHY™ system-side interface at 25/50 MHz.
- Generic 8-bit microprocessor interface for configuration, control, and status monitoring.
- Scrambling/descrambling ($1+X^6+X^7$) of SONET/SDH frame. Selectable self-synchronous scrambler implementing ($X^{43}+1$) polynomial for ATM/HDLC.
- Supports multiple devices sharing the same Utopia interface when used in a multi-PHY configuration.
- Provides an 8-bit General Purpose I/O (GPIO) register.
- HDLC/PPP processing compliant with RFC 1619 & 1662.
- Compliant with SONET/ SDH specifications ANSI T1.105, Bellcore GR-253-CORE and ITU G.707.
- Supports IEEE 1149.1 JTAG testing.
- Provides internal loopback paths for diagnostics.
- Packaged in a 208 pin PQFP.
- Implemented in 0.35 micron CMOS with 3.3v core and 5V tolerant I/O.

General Description

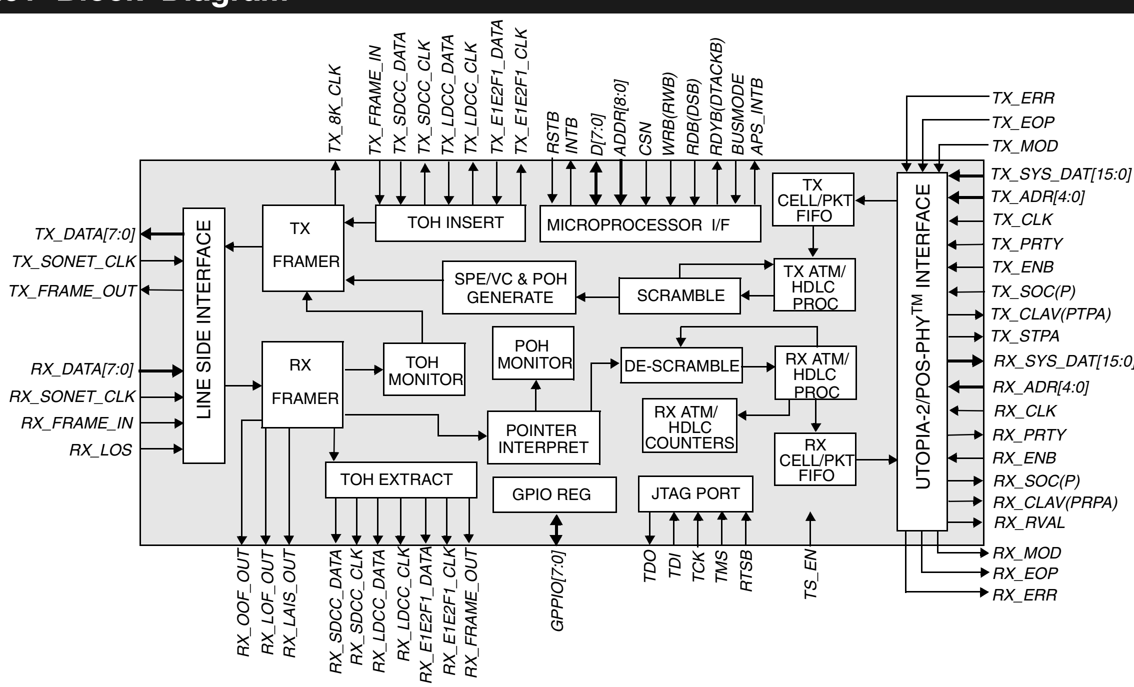
The S1201 is a highly-integrated VLSI device that provides full-duplex mapping of PPP encapsulated packets or ATM cells into STS-12c/AU-4-4c or STS-3c/AU-4 payloads. The S1201 supports full-duplex processing of SONET/SDH data streams with full section, line, and path overhead processing. The device supports framing pattern, scrambling/descrambling, alarm signal insertion/detection, and bit interleaved parity (B1/B2/B3) processing. Serial interfaces for SONET/SDH TOH overhead bytes are also provided.

The S1201 provides a line-side interface that can operate at 622.08 Mb/s (8-bit bus at 77.76 MHz) or 155.52 Mb/s (8-bit bus at 19.44 MHz). For ATM applications, a UTOPIA Level 2 system interface, operating at either 25 or 50 MHz is provided. For Packet-over-SONET applications, a POS-PHY™ interface is provided.

ATM support includes insertion and extraction of ATM cells into and out of the SONET/SDH SPE, scrambling/descrambling, header error control (HEC) detection and correction, idle cell generation and filtering, and generation of performance monitoring counts for TX, RX, ERR, dropped and idle cells.

HDLC support includes framing, transparency processing, optional 16/32 FCS processing, and self synchronous scrambling/descrambling ($X^{43}+1$). It also supports a direct flow-thru mode where the system data is passed directly to or from the SPE.

S1201 Block Diagram



Device Speicification Information - The information contained in this document is about a product in its fully tested and characterized phase. All features described herein are supported. Contact AMCC for updates to this document and the latest product status.

Overview and Applications

SONET Processing

The S1201 performs standard STS-3c/STM-1 or STS-12c/(STM-4/AU-4-4c) processing for both the transmit and receive directions. ATM cells or PPP packets are mapped into the SONET/SDH SPE/VC, the POH, TOH/SOH are inserted, and the resulting STS frame is transmitted in byte wide format to the line-side interface. The reverse process occurs when receiving data from the line-side. A TOH interface provides direct add/drop capability for E1, E2, F1, & both Section and Line DCC channels. The S1201 also includes a clear channel mode that enables the direct transmission of system payload from the system interface to the line-side interface.

ATM Processing

When configured for ATM cell processing, the S1201's transmit ATM processor will perform all necessary cell encapsulation including HEC generation, cell level scrambling (X^{43}+1), and idle cell insertion to adapt the cell rate to the SPE. When receiving data from the line side, it performs cell delineation, Rx header control, descrambling, and receive cell rate adaptation. The S1201 also provides a full suite of status and control registers accessible via the microprocessor.

PPP/HDLC Processing

When configured for POS mode, the S1201's transmit HDLC processor provides the insertion of HDLC framed packets into the STS SPE. It will perform PPP packet framing, inter-frame fill and Tx FIFO error recovery. In addition, it optionally performs payload scrambling (X^{43}+1), performs transparency processing as required by RFC 1662 and will optionally generate a 16/32 bit CRC.

The receive HDLC processor provides for the extraction of HDLC frames, transparency removal, de-scrambling (if enabled), FCS error checking and optionally deletes the HDLC control and address fields. The S1201 also provides a robust set of counters and status/control registers for performance monitoring via the microprocessor.

Line-side Interface

On the line-side, the S1201 supports an 8-bit parallel interface which operates at 77.76/19.44 MHz when the device is configured for STS-12/STS-3. The device is typically connected to a parallel-to-serial converter, which is in turn connected to an electrical-to-optical converter for interfacing to the fiber optic interface. (See figure below.)

System Interface

The S1201 interface to the system link-layer device is via a Utopia Level-2 compliant interface when operating in ATM mode, and a POS-PHY™ compatible interface when operating in Packet-Over-SONET mode. The interface operates at 25/50 MHz, as either 8 or 16 bits, in either Utopia or POS-PHY™ mode.

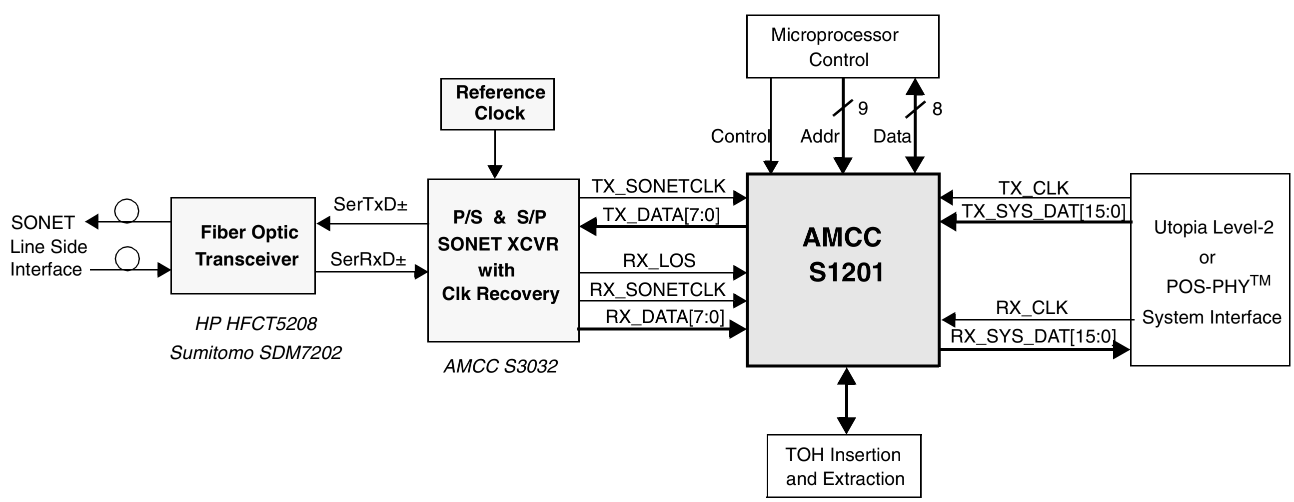
Microprocessor Interface

An 8-bit microprocessor interface is provided for device control and monitoring. The interface supports both Intel and Motorola type microprocessors, and is capable of operating in either an interrupt driven or polled-mode configurations.

Applications

ATM switches, Routers, IP switches, Virtual Networks.

Typical Application: S1201 in 622 Mb/s ATM or POS System



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1.0 Applicable Documents

1. ATM Forum, “Utopia Specification Level 1”, Version 2.01, af-phy-0017.001, March 1994
2. ATM Forum, “Utopia Specification Level 2”, Version 1.0, af-phy-0039.000, June 1995
3. ATM Forum “ATM User-Network Interface Specification”, V3., 1af-uni-0010.002, 1994
4. William Simpson, “PPP Over SONET/SDH”, IETF RFC 1619, May 1994
5. William Simpson, “PPP in HDLC-Like Framing”, IETF RFC 1662, July 1994
6. William Simpson, “The Point-to-Point Protocol”, IETF RFC 1661, July 1994
7. ISO/IEC 3309:1991(E), “Information Technology - Telecommunications & information exchange between systems - High Level Data Link Control (HDLC) procedures - Frame structure”, International Organization for Standardization, Fourth Edition 1991-06-01.
8. ISO/IEC 3309:1991/Amd.2:1992(E), “Information Technology - Telecommunications & information exchange between systems - High Level Data Link Control (HDLC) procedures - Frame structure - Amendment 2”: Extended transparency options for start/stop transmission”, International Organization for Standardization, 1992-01-15.
9. ANSI, “Digital Hierarchy-Optical Interface Rates and Format Specification”. ANSI-T1.105-1991
10. Bellcore Specification “SONET Transport Systems: Common Generic Criteria”, GR-253-CORE, Issue 2, Rev. 1, December 1997.
11. ITU-T Recommendation G.707, “Network Node Interface for the Synchronous Digital Hierarchy”, March 1996.
12. ITU-T I.432.1, “Series 1: Integrated Services Digital Network: B-ISDN user-network interface - Physical layer specification: General characteristics”, August 1996.
13. ITU-T I.432.2, “Series 1:Integrated Services Digital Network: B-ISDN user-network interface - Physical layer specification: 155 520 kbit/s and 622 080 kbit/s operation”, August 1996.

2.0 Pin Assignments and Descriptions

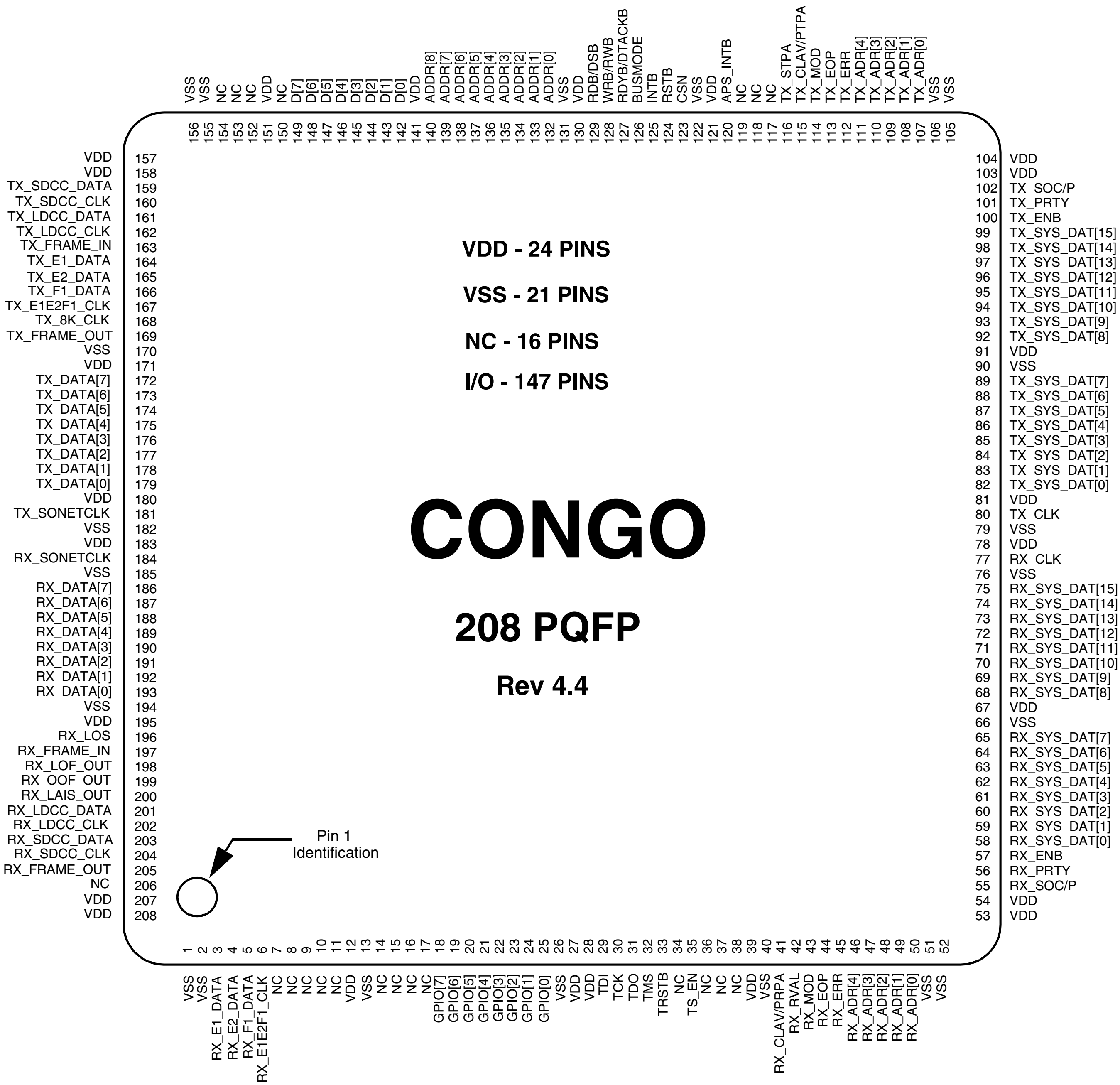


Figure 1: S1201 Pin Assignments

Table 1. Line Side Interface Pin Descriptions

Signal Name	Pin #	Type (I/O)	Signal Description
RX_DATA[0] RX_DATA[1] RX_DATA[2] RX_DATA[3] RX_DATA[4] RX_DATA[5] RX_DATA[6] RX_DATA[7]	193 192 191 190 189 188 187 186	I	**RECEIVE DATA:** Byte-wide STS-3c/12c data input stream. RX_DATA[7] is the MSB, RX_DATA[0] is the LSB. Data is sampled on the rising edge of RX_SONETCLK.
RX_FRAME_IN	197	I	**RECEIVE FRAME INDICATOR:** Frame position indication signal is active high and indicates the SONET frame position on the RX_DATA[7:0] bus. Sampled on the rising edge of RX_SONETCLK.
RX_LAIS_OUT	200	O	**RECEIVE LINE ALARM INDICATION SIGNAL OUTPUT:** Receive line alarm indication signal will be set high if a binary “111” pattern is received for the number of consecutive frames programmed into the K2_CONSEC register. RX_LAIS_OUT will be cleared if a binary “111” pattern is not received for the number of consecutive frames programmed into the K2_CONSEC register.
RX_LOF_OUT	198	O	**RECEIVE LOSS OF FRAME OUTPUT:** RX_LOF_OUT is set high when there is a loss of frame indication. If RX_OOF is active continuously for 24 consecutive frames (3 ms), the RX_LOF bit is set high. Once RX_LOF is set, it remains high until RX_OOF is inactive continuously for 3 ms.
RX_LOS	196	I	**RECEIVE LOS OF SIGNAL:** RX_LOS should be used to indicate to the framer that there is no signal present from the optical receiver. The signal’s default is active high, but can be set to active low by programming RX_LOS_LEVEL = 1.
RX_OOF_OUT	199	O	**RECEIVE OUT OF FRAME OUTPUT:** RX_OOF_OUT is set high when there is an out of frame indication. An out of frame condition occurs when four consecutive errored framing patterns specified in the A1 or A2 bytes have been received.
RX_SONETCLK	184	I	**RECEIVE SONET CLOCK:** RX_SONETCLK is the receive input clock from the line side, and provides timing for the receive data bus and frame position indication inputs. When run in STS-3c mode, RX_SONETCLK should be 19.44 MHz. When run in STS-12c mode, RX_SONETCLK should be 77.76 MHz.
TX_DATA[0] TX_DATA[1] TX_DATA[2] TX_DATA[3] TX_DATA[4] TX_DATA[5] TX_DATA[6] TX_DATA[7]	179 178 177 176 175 174 173 172	O	**TRANSMIT DATA:** Byte-wide STS-3c/12c data output stream. TX_DATA[7] is the MSB, TX_DATA[0] is the LSB. Data is updated on the rising edge of TX_SONETCLK.

Table 1. Line Side Interface Pin Descriptions

Signal Name	Pin #	Type (I/O)	Signal Description
TX_FRAME_OUT	169	O	**TRANSMIT FRAME POSITION OUTPUT INDICATOR:** Frame position indication signal is active high and indicates the SONET frame position on the TX_DATA[7:0] bus. Updated on the rising edge of TX_SONETCLK.
TX_SONETCLK	181	I	**TRANSMIT SONET CLOCK:** TX_SONETCLK is the transmit output clock to the line side, and provides timing for the transmit data bus and frame position indication outputs. When run in STS-3c mode, TX_SONETCLK will be nominally 19.44 MHz. When run in STS-12c mode, TX_SONETCLK should be nominally 77.76 MHz.

Table 2. Utopia and POS-PHY™ Pin Descriptions

Signal Name	Pin #	Type (I/O)	Signal Description
RX_ADR[0] RX_ADR[1] RX_ADR[2] RX_ADR[3] RX_ADR[4]	50 49 48 47 46	I	**RECEIVE SYSTEM ADDRESS** ***All Modes:*** Five bit wide true data driven from the ATM or Link Layer device to the framer to poll and select the appropriate device. RX_ADR[4] is the MSB. For polled mode applications, RX_ADR[4:0] is also used to determine the device whose cell/packet available signal is polled on the RX_CLAV/PRPA output. The S1201's address value is programmed using the register PHYADDR[4:0]. Address 0x1F is the null-PHY address, and is not responded to by any S1201 device.
RX_CLAV/PRPA	41	O,Z	**RECEIVE CELL AVAILABLE/PACKET AVAILABLE** ***All Modes:*** When the S1201 is configured for polled access cell/packet-level transfer, the RX_CLAV/PRPA signal is asserted high when there is data available in the polled-device's receive FIFO. RX_CLAV/PRPA is tri-stated when an address not matching the value programmed in the S1201's PHYADDR register is present, or when the null-PHY address (0x1F) is present. When the S1201 is configured for direct access byte-level transfer mode, RX_CLAV/PRPA is a direct status indication that there is data available in the device's receive FIFO. ***POS-PHY™ and Direct Map Modes:*** The user can control the assertion and de-assertion of RX_CLAV/PRPA by programming the high and low watermarks in the **RX_FIFOFULL_RPA** and **RX_FIFOEMPTY_RPA** registers. ***UTOPIA Mode:*** When operating in UTOPIA mode, RX_CLAV/PRPA is asserted high when a cell is available in the receive FIFO. RX_CLAV/PRPA is de-asserted one cycle after or four cycles before the transfer of the final byte/word, if there is not another complete cell available for transfer.

Table 2. Utopia and POS-PHY™ Pin Descriptions

Signal Name	Pin #	Type (I/O)	Signal Description
RX_CLK	77	I	**RECEIVE CLOCK** ***All Modes:*** Used to synchronize data transfers between the link layer device and the S1201. RX_CLK nominally operates at 25 MHz when the S1201 is operating in 155Mb/s mode, and 50 MHz when operating in 622Mb/s.
RX_ENB	57	I	**RECEIVE ENABLE** ***All Modes:*** Active low signal asserted by the ATM or Link layer device to indicate that RX_SYS_DAT and RX_SOC/P will be sampled at the end of the next cycle. Note, to support multi-PHY configurations, RX_ENB is used to tri-state RX_SYS_DAT and RX_SOC/P outputs. RX_SYS_DAT and RX_SOC/P are enabled only in cycles following those with RX_ENB asserted. When the S1201 is configured for polled access cell/packet-level transfer mode, data transfer operations occur with device selection on RX_ADR[4:0] when RX_ENB is deasserted, and subsequent data transfer on RX_SYS_DAT[15:0] while RX_ENB is asserted. When RX_ENB is asserted, RX_ADR[4:0] is used for polling RX_CLAV/PRPA signals. When the S1201 is configured for direct access byte-level transfer mode, RX_ENB is asserted when data is transferred from the S1201 selected by RX_ADR[4:0] to the ATM or link layer device.
RX_EOP	44	O,Z	**RECEIVE END OF PACKET** ***POS-PHY™ Mode:*** RX_EOP marks the end of a packet on the RX_SYS_DAT[15:0] bus. The S1201 tri-states RX_EOP when RX_ENB is high. RX_EOP is also tri-stated when an address not matching the value programmed in the S1201's PHYADDR register is present, or when the null-PHY address (0x1F) is present. ***UTOPIA and Direct Map Modes:*** Not used.
RX_ERR	45	O,Z	**RECEIVE ERROR** ***POS-PHY™ Mode:*** Used to indicate that the current packet is aborted and should be discarded. The S1201 tri-states RX_ERR when RX_ENB is high. RX_ERR is also tri-stated when an address not matching the value programmed in the S1201's PHYADDR register is present, or when the null-PHY address (0x1F) is present. ***UTOPIA and Direct Map Modes:*** Not used.
RX_MOD	43	O,Z	**RECEIVE MODULO** ***POS-PHY™ Mode:*** Used to indicate the modulo of the last word of a packet transfer. RX_MOD is set high to indicate the last word of the transfer contains 1 byte, is set low to indicate a 2-byte word. The S1201 tri-states RX_MOD when RX_ENB is high. RX_MOD is also tri-stated when an address not matching the value programmed in the S1201's PHYADDR register is present, or when the null-PHY address (0x1F) is present. ***UTOPIA and Direct Map Modes:*** Not used.

Table 2. Utopia and POS-PHY^{TM} Pin Descriptions

Signal Name	Pin #	Type (I/O)	Signal Description
RX_PRTY	56	O,Z	**RECEIVE PARITY** ***All Modes:*** Indicates the parity on the data being driven onto RX_SYS_DAT[15:0] when the system interface is configured for word mode, and RX_SYS_DAT[7:0] when configured for byte mode. Parity mode is programmed in the **RX_PRTY_MODE** register for odd or even parity. The S1201 tri-states RX_PRTY when RX_ENB is high. RX_PRTY is also tri-stated when an address not matching the value programmed in the S1201's PHYADDR register is present, or when the null-PHY address (0x1F) is present.
RX_RVAL	42	O,Z	**RECEIVE DATA VALID** ***POS-PHY^{TM} and Direct Map Mode:*** RX_RVAL indicates the validity of the receive data signals. When RX_RVAL is high, the receive signals RX_SYS_DAT, RX_SOC/P, RX_EOP, RX_MOD, RX_PRTY and RX_ERR are valid. When RX_RVAL is low, all receive signals are invalid and should be disregarded. RX_RVAL allows the link layer device to monitor the selected S1201 during a data transfer, while polling other S1201's using RX_CLAV/PRPA. The S1201 tri-states RX_RVAL when RX_ENB is high. RX_RVAL is also tri-stated when an address not matching the value programmed in the S1201's PHYADDR register is present, or when the null-PHY address (0x1F) is present. ***UTOPIA Mode:*** Not used.
RX_SOC/P	55	O,Z	**RECEIVE START OF CELL/PACKET** ***POS-PHY^{TM} and Utopia Modes:*** RX_SOC/P is asserted high on the first word of a packet transmitted from the S1201 to the ATM or Link layer. The S1201 tri-states RX_SOC/P when RX_ENB is high. RX_SOC/P is also tri-stated when an address not matching the value programmed in the S1201's PHYADDR register is present, or when the null-PHY address (0x1F) is present. ***DIrect Map Mode:*** Not used.
RX_SYS_DAT[0] RX_SYS_DAT[1] RX_SYS_DAT[2] RX_SYS_DAT[3] RX_SYS_DAT[4] RX_SYS_DAT[5] RX_SYS_DAT[6] RX_SYS_DAT[7] RX_SYS_DAT[8] RX_SYS_DAT[9] RX_SYS_DAT[10] RX_SYS_DAT[11] RX_SYS_DAT[12] RX_SYS_DAT[13] RX_SYS_DAT[14] RX_SYS_DAT[15]	58 59 60 61 62 63 64 65 68 69 70 71 72 73 74 75	O,Z	**RECEIVE SYSTEM DATA** ***All Modes:*** RX_SYS_DAT[15:0] transfers the data packet from the S1201 to the link layer device. Eight bit operation across RX_SYS_DAT[7:0] is possible by setting the register RX_SYSINT_8BIT=1. RX_SYS_DAT is considered valid only when RX_ENB is simultaneously asserted and a valid S1201 device has been selected via RX_ADR[4:0]. Data is updated on the rising edge of RX_CLK. The S1201 tri-states RX_SYS_DAT bus when RX_ENB is high. RX_SYS_DAT bus is also tri-stated when an address not matching the value programmed in the S1201's PHYADDR register is present, or when the null-PHY address (0x1F) is present.

Table 2. Utopia and POS-PHY™ Pin Descriptions

Signal Name	Pin #	Type (I/O)	Signal Description
TX_ADR[0] TX_ADR[1] TX_ADR[2] TX_ADR[3] TX_ADR[4]	107 108 109 110 111	I	**TRANSMIT SYSTEM ADDRESS** ***All Modes:*** Used to select the device that is being written to using the TX_ENB signal. TX_ADR[4] is the MSB. For polled modes, TX_ADR[4:0] is also used to determine the device whose cell/packet/data available signal is polled on the TX_CLAV/TPTA output. The S1201's address value is programmed using the register PHYADDR[4:0]. Address 0x1F is the null-PHY address, and is not responded to by any S1201 device.
TX_CLAV/PTPA	115	O,Z	**TRANSMIT CELL AVAILABLE/POLLED PACKET AVAILABLE** ***All Modes:*** When the S1201 is configured for polled access transfer mode, the TX_CLAV/PTPA signal is asserted high when the transmit FIFO can accept cell/packet data, otherwise is deasserts the signal. TX_CLAV/PTPA is tri-stated when an address not matching the value programmed in the S1201's PHYADDR register is present, or when the null-PHY address (0x1F) is present. ***POS-PHY™ Mode:*** The user can control the assertion and de-assertion of TX_CLAV/PTPA by programming the high and low watermarks in the **TX_FIFOFULL_TPA** and **TX_FIFOEMPTY_TPA** registers. ***UTOPIA Mode:*** When operating in UTOPIA mode, TX_CLAV/PTPA is asserted high to indicate it can accept the transfer of a complete cell, otherwise it deasserts the signal. TX_CLAV/PTPA is de-asserted one cycle after or four cycles before the transfer of the final byte/word, if there is not another complete cell available for transfer.
TX_CLK	80	I	**TRANSMIT CLOCK** ***All Modes*:** Used to synchronize data transfers between the link layer device and the S1201. TX_CLK nominally operates at 25 MHz when the S1201 is operating in 155Mb/s mode, and 50 MHz when operating in 622Mb/s.
TX_ENB	100	I	**TRANSMIT ENABLE** ***All Modes:*** Active low signal asserted by the ATM or Link layer device to indicate that TX_SYS_DAT and TX_SOC/P will be sampled at the end of the next cycle. When the S1201 is configured for polled access transfer mode, data transfer operations occur with device selection on TX_ADR[4:0], while TX_ENB is deasserted (high), and subsequent data transfer on TX_SYS_DAT[15:0], while TX_ENB is asserted (low). When TX_ENB is asserted, TX_ADR[4:0] is used for polling TX_CLAV/PTPA signals. When the S1201 is configured for direct access transfer mode, TX_ENB is asserted when data is transferred from the ATM or link layer device to the S1201 selected by TX_ADR[4:0].
TX_EOP	113	I	**TRANSMIT END OF PACKET** ***POS-PHY™ Mode:*** TX_EOP marks the end of a packet on the TX_SYS_DAT[15:0] bus. When *TX_EOP* is high, the last word of the packet is present on the *TX_SYS_DAT* bus. ***UTOPIA and Direct Map Modes:*** Not used.

Table 2. Utopia and POS-PHY^{TM} Pin Descriptions

Signal Name	Pin #	Type (I/O)	Signal Description
TX_ERR	112	I	**TRANSMIT ERROR** ***POS-PHY^{TM} Mode:*** Used to indicate that the current packet is aborted and should be discarded. TX_ERR is only asserted during the last word transfer of a packet. ***UTOPIA and Direct Map Mode:*** Not used.
TX_MOD	114	I	**TRANSMIT MODULO** ***POS-PHY^{TM} Mode:*** Used to indicate the modulo of the last word of a packet transfer. TX_MOD is set high to indicate the last word of the transfer contains 1 byte, is set low to indicate a 2-byte word. ***UTOPIA and Direct Map Modes:*** Not used.
TX_PRTY	101	I	**TRANSMIT PARITY** ***All Modes:*** Indicates the parity on the data being driven onto TX_SYS_DAT[15:0] when the system interface is configured for word mode, and TX_SYS_DAT[7:0] when configured for byte mode.Parity mode is programmed in the **TX_PRTY_MODE** register for odd or even parity.
TX_SOC/P	102	I	**TRANSMIT START OF CELL/PACKET** ***POS-PHY^{TM} and Utopia Modes:*** TX_SOC/P is asserted high on the first word of every cell/packet transmitted to the S1201. TX_SOC/P is required to be present at the beginning of every cell/packet and is considered valid only when TX_ENB is asserted. ***Direct Map Mode:*** Not used.
TX_STPA	116	O	**TRANSMIT SELECTED PHY PACKET AVAILABLE** ***POS-PHY^{TM} and Direct Map Modes:*** TX_STPA is only available in polled transfer mode. It provides a continuous status indication for the CD12001 that currently has data being written into it, in order to avoid FIFO overflows while polling is performed. TX_STPA is tristated when TX_ENB is deasserted, when the null address is on TX_ADR, or when an address not matching PHYADDR has been selected for data transfer. When actively driving, TX_STPA transitions according to the same algorithm used for TX_CLAV/PTPA. ***UTOPIA Mode:*** Not used.

Table 2. Utopia and POS-PHY™ Pin Descriptions

Signal Name	Pin #	Type (I/O)	Signal Description
TX_SYS_DAT[0] TX_SYS_DAT[1] TX_SYS_DAT[2] TX_SYS_DAT[3] TX_SYS_DAT[4] TX_SYS_DAT[5] TX_SYS_DAT[6] TX_SYS_DAT[7] TX_SYS_DAT[8] TX_SYS_DAT[9] TX_SYS_DAT[10] TX_SYS_DAT[11] TX_SYS_DAT[12] TX_SYS_DAT[13] TX_SYS_DAT[14] TX_SYS_DAT[15]	82 83 84 85 86 87 88 89 92 93 94 95 96 97 98 99	I	**TRANSMIT SYSTEM DATA** ***All Modes:*** TX_SYS_DAT[15:0] transfers the cell/packet/data from the ATM or link layer device to the S1201. TX_SYS_DAT[15] is the MSB. Eight bit operation across TX_SYS_DAT[7:0] is possible by setting the register TX_SYSINT_8BIT=1. TX_SYS_DAT is considered valid only when TX_ENB is simultaneously asserted and a valid S1201 device has been selected via TX_ADR[4:0]. Data is updated on the rising edge of TX_CLK.

Table 3. Transport Overhead Pin Descriptions

Signal Name	Pin #	Type (I/O)	Signal Description
RX_E1_DATA	3	O	**RECEIVED E1 DATA:** Local orderwire channel data byte (E1) received from the line side.
RX_E2_DATA	4	O	**RECEIVED E2 DATA:** Express orderwire channel data byte (E2) received from the line side.
RX_F1_DATA	5	O	**RECEIVED F1 DATA:** Maintenance channel data byte (F1) received from the line side.
RX_E1E2F1_CLK	6	O	**RECEIVED E1/E2/F1 DATA REFERENCE CLOCK:** A 64 kHz clock reference output for E1/E2/F1 data. The MSB of the E1/E2/F1 bytes appears in the first 64 kHz clock cycle after a rising edge of RX_FRAME_OUT.
RX_FRAME_OUT	205	O	**RECEIVE FRAMER START-OF-FRAME INDICATION:** This signal is nominally 8 kHz and is high during the first row of overhead of the received frame. The RX_FRAME_OUT signal is also used for byte alignment of the received E1/E2/F1 data outputs.
RX_LDCC_DATA	201	O	**RECEIVED LINE DCC DATA:** Drop output for received Line Data Communications Channel (DCC).
RX_LDCC_CLK	202	O	**RECEIVED LINE DCC REFERENCE CLOCK:** A gapped 576 kHz clock reference for Line DCC data. The RX_LDCC_DATA outputs are updated on the falling edge of RX_LDCC_CLK.
RX_SDCC_DATA	203	O	**RECEIVED SECTION DCC DATA:** Drop output for received Section Data Communications Channel (DCC).
RX_SDCC_CLK	204	O	**RECEIVED SECTION DCC REFERENCE CLOCK:** A gapped 192 kHz clock reference for Section DCC data. The RX_SDCC_DATA outputs are updated on the falling edge of RX_SDCC_CLK.
TX_E1_DATA	164	I	**TRANSMIT E1 DATA:** Local orderwire channel data byte (E1) to be inserted by the S1201 into the outgoing SONET data stream.

Table 3. Transport Overhead Pin Descriptions

Signal Name	Pin #	Type (I/O)	Signal Description
TX_E2_DATA	165	I	**TRANSMIT E2 DATA:** Express orderwire channel data byte (E2) to be inserted by the S1201 into the outgoing SONET data stream.
TX_F1_DATA	166	I	**TRANSMIT F1 DATA:** Maintenance channel data byte (F1) to be inserted by the S1201 into the outgoing SONET data stream.
TX_E1E2F1_CLK	167	O	**TRANSMIT E1/E2/F1 DATA REFERENCE CLOCK:** A 64 kHz clock reference output for E1/E2/F1 data to be inserted by the S1201 into the outgoing SONET data stream.
TX_FRAME_IN	163	I	**TRANSMIT FRAMER START-OF-FRAME INDICATION:** This signal is nominally 8 kHz and is used for byte alignment of the transmitted E1/E2/F1 data outputs. The MSB of the E1/E2/F1 bytes should be aligned with the frame start pulse on TX_FRAME_IN.
TX_LDCC_DATA	161	I	**TRANSMIT LINE DCC DATA:** Input for the Line Data Communications Channel (DCC) to be inserted by the S1201 into the outgoing SONET data stream.
TX_LDCC_CLK	162	O	**TRANSMIT LINE DCC REFERENCE CLOCK:** A 576 kHz clock reference for Line DCC data to be inserted by the S1201 into the outgoing SONET data stream. The TX_LDCC_DATA inputs are sampled on the falling edge of TX_LDCC_CLK.
TX_SDCC_DATA	159	I	**TRANSMIT SECTION DCC DATA:** Input for the Section Data Communications Channel (DCC) to be inserted into the outgoing SONET data stream from the S1201.
TX_SDCC_CLK	160	O	**TRANSMIT SECTION DCC REFERENCE CLOCK:** A 192 kHz clock reference for Section DCC data to be inserted by the S1201 into the outgoing SONET data stream. The TX_SDCC_DATA inputs are sampled on the falling edge of TX_LDCC_CLK.
TX_8K_CLK	168	O	**8kHz TRANSMIT CLOCK:** A general purpose 8kHz buffered clock derived from TX_SONETCLK which may be used for external clock reference purposes.

Table 4. Microprocessor Interface Pin Descriptions

Signal Name	Pin #	Type (I/O)	Signal Description
ADDR[0] ADDR[1] ADDR[2] ADDR[3] ADDR[4] ADDR[5] ADDR[6] ADDR[7] ADDR[8]	132 133 134 135 136 137 138 139 140	I	**ADDRESS BUS:** Allows host microprocessor to perform register selection within the S1201.
APS_INTB	120	O	**APS INTERRUPT**: Active-low output from the S1201 triggered by an APS event. APS_INTB is an open-drain output which is tri-stated when the interrupt is acknowledged by accessing the interrupt.

Table 4. Microprocessor Interface Pin Descriptions

Signal Name	Pin #	Type (I/O)	Signal Description
BUSMODE	126	I	**BUS INTERFACE MODE:** This signal allows the data transfer operations to be compatible with most microprocessor interfaces. When Busmode=1 data transfer occurs in “Intel mode” (RDB,WRB,RDYB), when Busmode=0 data transfer occurs in “Motorola mode” (DSB, RWB, DTACKB).
CSN	123	I	**CHIP SELECT**: Active-low chip select to the S1201 used to validate the address bus for read and write transfers.
D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7]	142 143 144 145 146 147 148 149	I/O	**DATA BUS:** Allows transfer of data between host microprocessor and the S1201.
INTB	125	O	**INTERRUPT**: Active-low output from the S1201 triggered by an event which caused the internal interrupt to become activated. INTB is an open-drain output which is tri-stated when the interrupt is acknowledged by accessing the interrupt.
RDB/DSB	129	I	**READ DATA BUS/DATA STROBE:** If BUSMODE=1, the RDB/DSB input is low to enable data to be read from the addressed location on the data bus. If BUSMODE=0 the RDB/DSB input is low to enable data to be read from, or to strobe write data into the S1201.
RDYB/DTACKB	127	O,Z	**READY/DATA ACKNOWLEDGE:** RDYB/DTACKB goes low to acknowledge the end of data transfers over the data bus. The RDYB/DTACKB signal is a tri-stated output and operates the same for both BUSMODE settings.
RSTB	124	I	**RESET:** Active low input to reset the S1201.
WRB/RWB	128	I	**WRITE/READ-WRITE DATA BUS:** If BUSMODE=1, the WRB/RWB input is low to enable data to be WRITTEN TO the addressed location on the data bus. If BUSMODE=0 the RDB/DSB input is low during write operations, and high during read operations.

Table 5. JTAG Interface Pin Description

Signal Name	Pin #	Type (I/O)	Signal Description
TCK	30	I	**TEST CLOCK:** JTAG input clock used to sample data on the TDI and TDO pins. Should be left high when JTAG interface is not in use.
TDI	29	I	**TEST DATA IN:** Input pin for serial data stream to be sent to the S1201. TDI is sampled on the rising edge of TCK.
TDO	31	O	**TEST DATA OUT:** Output pin for serial data stream sent from the S1201. TDO is sampled on the falling edge of TCK.

Table 5. JTAG Interface Pin Description

Signal Name	Pin #	Type (I/O)	Signal Description
TMS	32	I	**TEST MODE SELECT:** Controls the operating mode of the JTAG interface. TMS is sampled on the rising edge of TCK.
TRSTB	33	I	**TEST PORT RESET:** Active low input used to reset the JTAG interface.

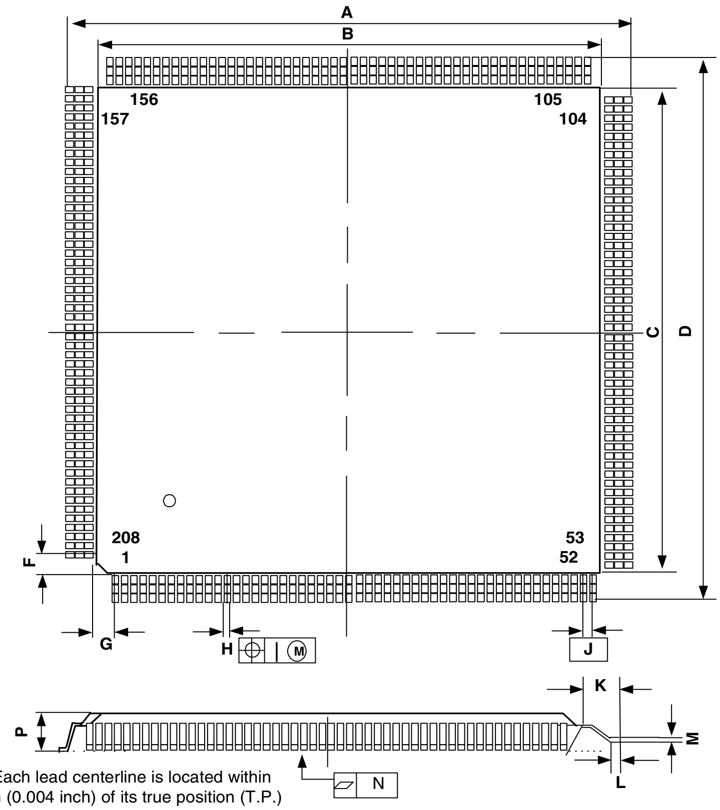
Table 6. Miscellaneous Pin Descriptions

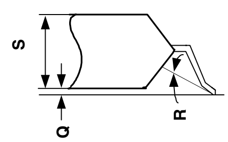
Signal Name	Pin #	Type (I/O)	Signal Description
GPIO[0] GPIO[1] GPIO[2] GPIO[3] GPIO[4] GPIO[5] GPIO[6] GPIO[7]	25 24 23 22 21 20 19 18	I/O	**GENERAL PURPOSE I/O:** The GPIO register allows the user to define each grouping (GPIO[0,1], GPIO[2,3], GPIO[4,5], GPIO[6,7]) as either input or output bits. These bits can be used for functions such as LED control or user-defined input control.
TS_EN	35	I	**TRI-STATE ENABLE:** When TS_EN is brought high, all output and input/output pins on the S1201 are tri-stated.
NC	7,8,9,10,11 14,15,16, 17, 34 36, 37, 38 117, 118 119 150, 152 153, 154 206	-	**NO CONNECT:** These pins are not used by the S1201 and should be left disconnected.
VDD	12, 27,28 39, 53,54 67,78,81 91, 103 104, 121 130, 141 151, 157 158, 171 180, 183 195, 207, 208	-	**POWER:** These pins should be connected to the 3.3v power supply.
VSS	1,2,13,26 40,51,52 66, 76, 79 90, 105 106, 122 131, 155 156, 170 182, 185 194	-	**GROUND:** These pins should be connected to the ground plane.

Note:

1. I = Input, O = Output, and Z = High Impedance.

3.0 Mechanical Packaging Information





NOTE: Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	30.6±0.2	1.205±0.008
B	28.0±0.2	1.102+0.009 -0.008
C	28.0±0.2	1.102+0.009 -0.008
D	30.6±0.2	1.205±0.008
F	1.25	0.049
G	1.25	0.049
H	0.22+0.05 -0.04	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.3±0.2	0.051±0.008
L	0.5±0.2	0.020+0.008 -0.009
M	0.17+0.03 -0.07	0.007+0.001 -0.003
N	0.10	0.004
P	3.2	0.126
Q	0.4±0.1	0.016+0.004 -0.005
R	5j±5j	5j±5j
S	3.8 MAX.	0.150 MAX.
		P208GD-50-LML, MML-2

4.0 Functional Descriptions

4.1 Conventions

Note: Bytes within the SONET or SDH signal are transmitted MSB first. By convention, the MSBs of SONET/SDH bytes are referred to as bit 1 and the LSBs as bit 8. However, the register words that provision and monitor SONET/SDH bytes are defined with bit 7 as the MSB and bit 0 as the LSB.

The S1201 fully supports SONET and SDH modes. For brevity, SONET terminology will be used as the main protocol for discussion.

The interface where data flows from the ATM or Link Layer device to the S1201 device is labeled the Transmit System Interface. The interface where data flows from the S1201 to the ATM or Link Layer device is labeled the Receive System Interface.

All bytes are transmitted in big endian order (MSB first) unless otherwise specified.

4.2 Monitors and Control Interface

For performance monitoring purposes, the CONGO contains a number of “delta” bits, “event” bits, “second event” bits, and error counters.

Delta bits are set (to logic “1”) by the CONGO when a monitored parameter changes state. The delta bit then stays high until the controller clears (to logic “0”) the bit by writing a 1 to the bit. If a write to 1 occurs simultaneously with a parameter state change, the delta bit is set. Delta bits are indicated by a **_D** suffix.

Event bits are similar to delta bits, but they do not have a corresponding status bit. Event bits are set (to logic “1”) by the CONGO when the associated event occurs (such as FIFO overflow). The event bit then stays high, regardless of whether or not the event reoccurs, until the controller clears (to logic “0”) the bit by writing a 1 to the bit. If a write to 1 occurs simultaneously with the event occurrence, the event bit is set. Event bits are indicated by a **_E** suffix.

There are several “events” that are monitored for occurrence each second. This allows the controller to accumulate the number of seconds that contain a particular event. (For example, the number of seconds that at least 1 error was detected in a received signal by monitoring the B1 bytes.) For this purpose, the CONGO creates a 1 Hz signal, SEC_EVENT. Alternatively, the timing for “second events” can be controlled by the **LATCH_CNT** register.

When the CONGO detects a rising edge of SEC_EVENT (and **CNT_SEC_EN** = 1) or when **LATCH_CNT** in register 0x001 is written from a 0 to a 1 (and **CNT_SEC_EN** = 0), it produces a pulse on an internal signal, LATCH_EVENT. When a pulse occurs on LATCH_EVENT, the ***_SECE** register bits are set if their corresponding internal current second event monitoring bits are active. Like delta and event bits, the ***_SECE** bits are not cleared until they are written to 1 by the controller. The microprocessor is notified via **LATCH_E** when a pulse occurs on LATCH_EVENT.

All the internal performance monitoring counter blocks are comprised of a running error counter and a holding register that presents stable results to the controller. The counts in all of the running counters are latched into the hold registers and the running counters cleared when a pulse occurs on LATCH_EVENT. To prevent missing a count that occurs when latching occurs, a counter is set to 1, rather than 0, if the clear signal is simultaneous with an increment.

After being latched, the results are held to be read by the microprocessor. All the internal counters have the ability to store more than the maximum possible count in a one second interval for a bit error rate of 10^{-3}. As long as the count values are latched (and the results read) every second, no counts will be lost. In case this doesn’t happen, all the running counters will hold their maximum value rather than roll over to zero.

Summary delta/event/second event bits provide a consolidated view of the various individual delta/event/second event bits, grouped either by function or tributary. Summary delta/event/second events are therefore a function of the other delta/event/second events bits in the register maps. These summary bits do not behave as their individual counterparts do, in that the summary bits are NOT cleared when written to a 1 by the uP. The summary bits are read only, and should only clear when all delta/event/second event bits that contribute to them are cleared.

The summary bits, as well as some delta, event and second event bits, are “NOR’ed” to form the CONGO interrupt outputs, *INTB* and *APS_INTB*. The contribution of any of these bits to the summary interrupts can be deleted by setting the corresponding “mask” bit.

4.3 Configuration

The **TX/RX_SIG_MODE** bit determines the format and rate of the SONET/SDH output signal. The value of this bit and the input signal formats that correspond to each are defined in Table 7.

Table 7. TX/RX_SIG_MODE Values

TX/RX_SIG_MODE	Output Signal
0	STS-3c/STM-4, byte wide output at 19.44 MHz
1	STS-12c/STM-4, byte wide output at 77.76 MHz

4.4 SONET/SDH Processing

The S1201 performs standard STS-12c/STM-4c or STS-3c/STM-1 processing for both the transmit and receive directions. In the transmit direction, the ATM cells or PPP packets are encapsulated into the SONET/SDH SPE/VC. The POH and TOH/SOH are inserted, and the resulting STS signal is transmitted in byte wide format to a parallel/serial converter and then to a Fiber Optic transceiver.

In the receive direction the process is reversed. The byte wide STS signal is received, the S1201 locates the frame and TOH/SOH, interprets the pointer, terminates the TOH/SOH and POH, extracts the SPE/VC, and then extracts the ATM cells or PPP packets from the SPE/VC payload. The PPP packets or ATM cells are then passed on to an appropriate Link Layer device via the Utopia Level 2 or POS-PHY™ system interface.

The SONET/SDH processor consists of a Receive SONET/SDH Processor and a Transmit SONET/SDH processor.

4.4.1 Receive SONET/SDH Processing

The Receive SONET/SDH Processor provides for the framing of the STS signal, descrambling, TOH/SOH monitoring including B1 and B2 monitoring, AIS detection, pointer processing, and POH monitoring.

The Receive SONET/SDH Processor performs the following functions:

- SONET/SDH framing, [A1 A1 A2 A2] bytes are detected and used for framing. Provides OOF and LOF indicators (single event and second event).
- Descrambling of payload using SONET/SDH frame synchronous scrambler, polynomial ($X^7 + X^6 + 1$).
- Monitors incoming B1 bytes and compares them to recalculated BIP-8 values. Provides error event information, including counts of individual bit errors, errored frames, and errored seconds.
- Monitors incoming B2 bytes and compares them to recalculated BIP-96/24 values. Provides error event information, including counts of individual bit errors, errored frames, and errored seconds.
- Monitors K1 and K2 bytes, which are used for sending Line/MS AIS or RDI, and for APS signaling.
- Monitors the 4 LSBs of received S1 bytes for consistent values in consecutive frames.
- Monitors the M1 byte for determining the number of B2 errors that are detected by the remote terminal in its received signal.
- For the purpose of determining whether or not the bit error rate of the received signal is above or below two different provisionable thresholds, the S1201 provides two B2 error rate threshold blocks. The Signal Fail (SF) and the Signal Degrade (SD) conditions are reported when thresholds are exceeded via interrupts.
- The TOH/SOH drop block outputs the received E1, F1, and E2 bytes and 2 serial DCC channels, SDCC

(D1-D3) and LDCC (D4-D12).

- Pointer state determination involves examining the H1-H2 bytes to establish the state of the received pointer (Normal, LOP, AIS). If the pointer state is normal, the first H1H2 bytes are read to determine the start of the SPE/VC.
- The POH monitoring block consists of J1, B3, C2, and G1 monitoring. These POH bytes are monitored for errors or changes in states.
- Monitors/Captures J1 bytes. In SONET applications, captures 64 consecutive J1 bytes and in SDH applications the CD12001 looks for repeating 16 consecutive J1 byte patterns.
- Monitors C2 bytes for verification of correct tributary types. The tributary is checked for 5 consecutive frames with identical C2 byte values.
- Monitors G1 for REI-P and RDI-P.
- Monitors incoming B3 bytes and compares them to recalculated BIP-8 values. Provides error event information, including counts of individual bit errors, errored frames, and errored seconds.

4.4.2 Transmit SONET/SDH Processing

The Transmit SONET/SDH Processor provides for the encapsulation of the ATM cells or POS packets into the SPE/VC. It then inserts the appropriate POH and TOH/SOH and outputs the final STS signal to a parallel to serial converter followed by a Fiber Optic transceiver.

- The Synchronous Payload Envelope/Virtual Container (SPE/VC) Generation block multiplexes ATM cells or PPP packets from the system interface with Path Overhead (POH) bytes that it generates to create the SPE for SONET or VC for SDH.
- Supports the following POH bytes: Path Trace (J1), Path BIP-8 (B3), Signal Label (C2), Path Status (G1). Other POH bytes are transmitted as fixed all-zeros.
- Performs AIS and Unequipped signal insertion.
- TOH/SOH generation, including:

  Frame bytes A1A2 - Fixed F628 or forced errors through Microprocessor Interface for test purposes

  Section Trace (J0) - Programmable through Microprocessor Interface

  Section Growth (Z0) - Fixed pattern 2-12

  Section BIP-8 (B1) - Calculated or forced errors through Microprocessor Interface for test purposes

  Orderwire (E1E2) - External Serial Interface

  Section User Channel (F1) - External Serial Interface

  Data Communications Channel (D1-D12) - External Serial Interface

  Pointer Bytes (H1H2H3) - Fixed 522, NDF disabled, SS programmable

  Line BIP-96/24 (B2) - Calculated or forced errors through Microprocessor Interface for test purposes

  APS/MS AIS (K1K2) - Programmable through Microprocessor Interface

  Synchronization Status (S1) - Programmable through Microprocessor Interface

  Line/MS REI (M1) - Calculated or forced errors through Microprocessor Interface for test purposes

- Undefined TOH/SOH transmitted as fixed all-zeros.

Scrambling of payload using SONET/SDH frame synchronous scrambler, polynomial ($X^7 + X^6 + 1$).

4.5 HDLC/ATM Processing

The S1201 extracts packets or cells from the SONET Payload Envelope (SPE). Packets are extracted via an HDLC processor and cells are extracted via an ATM cell delineation processor. The S1201 also supports a flow-thru mode that allows the SPE to pass directly to the System Interface.

The HDLC processor performs HDLC like framing for PPP and other packet based data. The HDLC processor is a single channel engine that is used to encapsulate packets into an HDLC frame as per RFC1619/1662. The HDLC processor operates on byte aligned data only (e.g. the message is an integer number of bytes in length). In POS mode, the HDLC processor is broken up into a Receive HDLC Processor and a Transmit HDLC Processor.

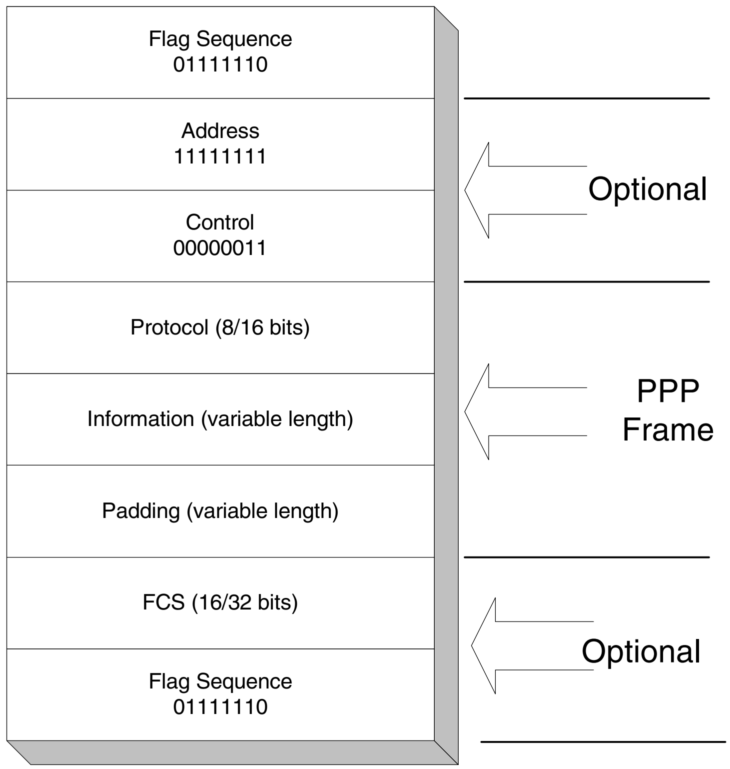
The ATM processor performs Cell insertion and delineation, per ITU-T 432.2. The ATM processor is broken up into a Receive ATM Processor and a Transmit ATM Processor.

4.5.1 Receive HDLC Processor

The Receive HDLC Processor provides for the extraction of HDLC frames, transparency removal, FCS error checking, de-scrambling of the SPC/VC payload, optional deletion of the control and address fields, and performance monitoring. Additionally, it includes a clear channel mode that enables the direct transfer of STS SPE data to the System Interface.

After the start/end of field flags and byte stuffing are removed the remaining payload includes the data and the FCS field. See figure below for details. Note, only one flag byte is required between two packets. All flags between packets are discarded.

Figure 2: HDLC Frame Structure



The Receive HDLC Processor performs the following functions:

- Optionally self synchronous de-scrambles (X^{43}+1 polynomial) received payload.
- Detects and terminates the HDLC frame, e.g. frame delimiting flag detection.
- Removes Control Escape stuffing
- Calculates optional FCS code (16 or 32 bit) and compares it against the received FCS value. Errors are accumulated in Performance Monitor Registers. Outgoing data is marked as errored if FCS error is detected.
- Detects abort sequence in (0x7D, 0x7E) in byte stream.
- Optionally deletes Address and Control fields.
- Provides optional minimum and maximum packet length detection (SW configurable) and asserts RX_ERR signal with data to mark errored condition.
- Generates Performance Monitoring for octets: FCS Errors, Aborted packets, Short Packets, Long Packets, Packets discarded due to RXFIFO error.
- Optionally deletes packet stuffing used to handle far end FIFO underflow conditions.
- Generates interrupt on error conditions.
- Automatically deletes inter-packet gap of flags.

4.5.2 Receive ATM Processor

When the S1201 is configured for ATM cell extraction, the Receive ATM Processor performs cell delineation, RX Header Control, descrambling, and receive cell rate adaptation. It also provides performance monitoring counts.

Specifically, the Receive ATM Processor performs the following functions:

- ATM Cell Delineation per ITU-T 432.2
- Receive Header Error Control
- Receive Cell Payload De-scrambling (X^{43} + 1) (Optional)
- Idle Cell Filtering - user programmable Idle Cell definition
- Receive Performance Monitoring for ATM. Counts include:
  - HEC Errored Cells - cells dropped due to error
  - Valid Cells
  - Cells with Headers that were corrected
  - Cells that were discarded due to FIFO overflow

4.5.3 Transmit HDLC Processor

The Transmit HDLC Processor provides the insertion of packet-based information into the STS SPE. It provides packet encapsulation, FCS field generation, inter-packet fill, TXFIFO error recovery and scrambling. Additionally it includes a clear channel mode that enables the direct transfer of System Interface Payload data to the STS SPE.

The Transmit HDLC Processor performs the following functions:

- Encapsulates packets within an HDLC frame. Each packet is encapsulated with a start flag (0x7E), an optional FCS field, optional Address and Control fields, and an optional end of field flag (0x7E).
- Optional self synchronous transmit payload scrambler (X^{43}+1 polynomial).
- Transparency processing as required by RFC 1662 (octet stuffing for Flags & Control Escape). Byte stuffing occurs between start and end of field flags. Stuffing replaces any byte that matches the flag or the control escape bytes with a two byte sequence consisting of the Control Escape followed by the original byte exclusive-ored with (0x20) HEX.
- Generates start and end of field flags (0x7E). Note a single flag can be shared between two packets.
- Optionally generates 16 or 32-bit CRC for Frame Check Sequence (FCS) field.
- Provides the ability to insert FCS errors for testing under SW control.
- TX_PRTY errors generate an interrupt.
- Provides for a selectable treatment of FIFO underflow. A FIFO underflow condition occurs when a TXFIFO empty occurs prior to the end of a packet. When this occurs an interrupt is generated. The packet can either be ended via generation of an FCS error, or an abort sequence, or “fill” bytes can be inserted during the gap via a SW configurable escape code.
- Generates Performance Monitor counts that include: Number of FIFO error events, aborted packets, and number of packets that violate minimum and maximum packet length parameters (SW configurable).
- Supports a clear channel mode that enables the direct transfer of System Interface Payload data to the STS SPE.

4.5.4 Transmit ATM Processor

When the S1201 is configured for ATM operation, the Transmit Processor performs HEC generation, cell level scrambling, and idle cell insertion to adapt the cell rate to the SPE. It also provides performance monitoring information from the Utopia System Interface.

Specifically the Transmit ATM Processor performs the following functions:

- System Interface Data Integrity checking (HEC and Parity)
- ATM HEC Sequence generation (optional), polynomial ($X^8 + X^2 + X + 1$).
- Transmit Cell Payload scrambling ($X^{43} + 1$) (Optional)
- Idle Cell Insertion - User defined Idle Cells
- Transmit System Interface Performance Monitoring for ATM.
    - FIFO over/underflow events
    - Parity error events
    - Cells received with HEC error
    - Valid Cells

4.6 FCS Polynomials

The S1201 supports CRC-16 (CCITT) and CRC-32 Frame Check Sequence (FCS) generation and checking. The Frame Check Sequence field defaults to 16 bits (two octets). The FCS is transmitted least significant octet first, which contains the coefficient of the highest term. The S1201 can be provisioned to calculate the FCS either using little endian bit order as per HDLC or big endian bit order.

The following polynomials are used for the generation and checking of the FCS values

CRC-16 (CCITT): $X^{16} + X^{12} + X^5 + 1$

CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$

The FCS field is calculated over all bits of the Address, Control, Protocol, Information & Padding fields, not including any octets inserted for transparency. This does not include the Flag Sequences nor the FCS field itself.

With both FCS methods, the CRC generators and checkers are initialized to all Logic “ones”. Upon completion of the FCS calculation the FCS value is ones-complemented. It is this new value that is inserted in the FCS field.

5.0 Processing of Data in the Transmit Direction

In the Transmit Direction, the CONGO device provides for the insertion of either packet based data or ATM cells into the STS/STM SPE. The operating mode of the device is provisionable through the management interface. The register value **TX_POS = 1** places the device in POS mode. The register value **TX_POS** = 0 places the device in ATM mode.

Optionally, the CONGO device can accept data from the system interface and directly map it into the SONET/SDH SPE. This mode of operation is selected by setting **TX_DIRECT_MAP** = 1. The value of **TX_POS** is ignored when **TX_DIRECT_MAP** = 1. The default values of **TX_DIRECT_MAP** and **TX_POS** are 0.

5.1 Transmit FIFO Interface

In ATM mode of operation, the Transmit System Interface operates as an Utopia Level 2 compliant interface. In POS mode, the Transmit System Interface operates as a POS-PHY™ compliant interface. In the direct mapping mode of operation, the Transmit System Interface operates as a variant of the POS-PHY™ interface, with the *TX_SOC/P*, *TX_EOP, TX_MOD* and *TX_ERR* signals disabled.

5.1.1 Transmit Data Parity Check

In all three modes, the CONGO calculates the parity of each 1 or 2 octet word received over the Transmit System Interface *TX_SYS_DAT* and compares it to the received parity, *TX_PRTY*. Parity errors are reported to the management interface by setting the **TX_PRTY_ERR_E** register to 1. **TX_PRTY_MODE** = 0 (the default) indicates that odd parity is used for this calculation. **TX_PRTY_MODE** = 1 indicates that even parity is used.

The CONGO does not treat a cell/packet received with parity errors as an errored cell/packet. It does not alter the cell/packet, but simply notifies the management interface of the parity error.

5.1.2 Transmit FIFO

The Transmit System Interface is controlled by the Link Layer device that precedes the CONGO in the transmit direction of the transmission path. The Link Layer device provides an interface clock to the CONGO for synchronizing all interface transfers. This convention requires the CONGO to incorporate a rate-matching buffer (i.e. a FIFO). The size of the FIFO is 256 octets.

The CONGO also transfers the packet/cell status (start/end of packet/cell, whether the last word in the packet consists of one or two octets, packet error) through the FIFO.

5.1.2.1 Transmit FIFO Error

In POS and ATM modes, the state of the FIFO is monitored by the CONGO device. A FIFO error condition is declared whenever 1) a *TX_SOC/P* is received prior to the end of a cell (53/54 octets later) or end of a packet (*TX_EOP* indication) or 2) the *TX_ENB* is active beyond the “transmit window” following the deassertion of the *TX_CLAV* signal. FIFO error events are reported to the management interface by setting **TX_FIFOERR_E = 1**.

The CONGO contains an 8-bit FIFO error counter that counts every cell/packet affected by a FIFO error event. When the performance monitoring counters are latched, the value of this counter is latched to the **TX_FIFOERR_CNT[7:0]** register, and the FIFO error counter is cleared. (See section 4.2).

If there has been at least one FIFO error event since the last rising edge of LATCH_EVENT, then the FIFO error event bit, **TX_FIFOERR_SECE**, is set.

In POS mode (**TX_POS = 1)**, the CONGO aborts the errored packets, see section 5.1.3.

In ATM mode (**TX_POS = 0**), any ATM cells corrupted by FIFO error events are deleted.

5.1.3 POS Errored Packet Handling

In POS mode of operation, (**TX_POS = 1),** the following errored packet handling procedures are provided:

5.1.3.1 *TX_ERR* Link Layer Indication

The Transmit System Interface provides a method by which the Link Layer device can indicate to the CONGO when a particular packet contains errors and should be aborted or discarded (see definition of *TX_ERR* in section 7.0)

The CONGO contains an 8-bit link layer error counter that counts every packet received from the Link Layer that is marked as errored (see *TX_ERR, section 7.0*). When the performance monitoring counters are latched (LATCH_EVENT transitions high), the value of this counter is latched to the **TX_POS_LLPKT_ERRCNT[7:0]** register, and the link layer packet error counter is cleared. (See section 4.2).

If there has been at least one link layer packet error since the last rising edge of LATCH_EVENT*,* then the link layer packet error event bit, **TX_POS_LLPKT_ERR_SECE**, is set.

5.1.3.2 Minimum/Maximum Packet Sizes

The CONGO also, as an option, views a packet as being errored and does not transmit it or aborts if it violates minimum or maximum packet sizes.The packet sizes refer to the size of the PPP packet only, and do not include the bytes inserted by the CONGO (flag sequence, address, control, FIFO underflow, transparency or the FCS bytes). These minimum and maximum sizes are programmable via the management interface. Register **TX_POS_PMIN[3:0]** contains the minimum packet size. The default value of this register is be **0**.

Register **TX_POS_PMAX[15:0]** contains the maximum packet size. The default value of this register is **0x05E0** (RFC 1661, pg 4).

The CONGO disables/enables minimum and maximum size packet checking when instructed to through the management interface. If **TX_POS_PMIN_ENB** or **TX_POS_PMAX_ENB = 1**, packet abort due to a violation of the packet size restriction is enabled. If = 0 (the default), packet size violations are ignored.

The CONGO contains two 8-bit error counters that count every violation of the maximum and minimum packet size limits. When the performance monitoring counters are latched, the value of these counters are latched to the **TX_POS_PMIN_ERRCNT[7:0]** and **TX_POS_PMAX_ERRCNT[7:0]** registers, and the packet size violation counters are cleared. (See section 4.2).

If there has been at least one packet size violation error since the last rising edge of LATCH_EVENT*,* then the appropriate packet size violation second event bit, **TX_POS_PMIN_ERR_SECE** or **TX_POS_PMAX_ERR_SECE**, is set.

5.1.3.3 Errored Packet Abort

The CONGO cannot delete packets if the error condition is received or detected after transmission of the packet has begun. These packets are therefore aborted. The CONGO supports two options for aborting an errored packet. The default option is to abort a packet by inserting the abort sequence, 0x7d7e. Reception of this code at the far end will cause the receiver to discard this packet.

As an alternative, the CONGO can also abort an errored packet by simply inverting the FCS bytes. The abort mode is controlled via the management interface. **TX_POS_FCSABRT_ENB = 1** enables the FCS inversion method, **TX_POS_FCSABRT_ENB = 0** (the default) disables it.

5.1.4 Line Side Cell/Packet Loopback

For testing purposes, the CONGO also provides the capability for the user to loopback the cells/packets it extracts from the SONET/SDH signal into the transmit direction FIFO, where it replaces the data received from the System Interface. This data will then undergo the transmit side ATM/HDLC processing, and be sent back out the SONET/SDH line. When **SYS_R_TO_T_LOOP** is set to 1, the loopback is activated. When **SYS_R_TO_T_LOOP** is 0, the loopback is inhibited and normal processing proceeds.

This loopback is provided primarily for device testing purposes. In actual operation, if the receive clock is faster than the transmit clock and the SONET/SDH payload is filled with packets or non-idle ATM cells, there could be periodic errors due to the inability of the transmit side to accommodate the full data rate of the receive side.

5.2 Transmit HDLC Processing

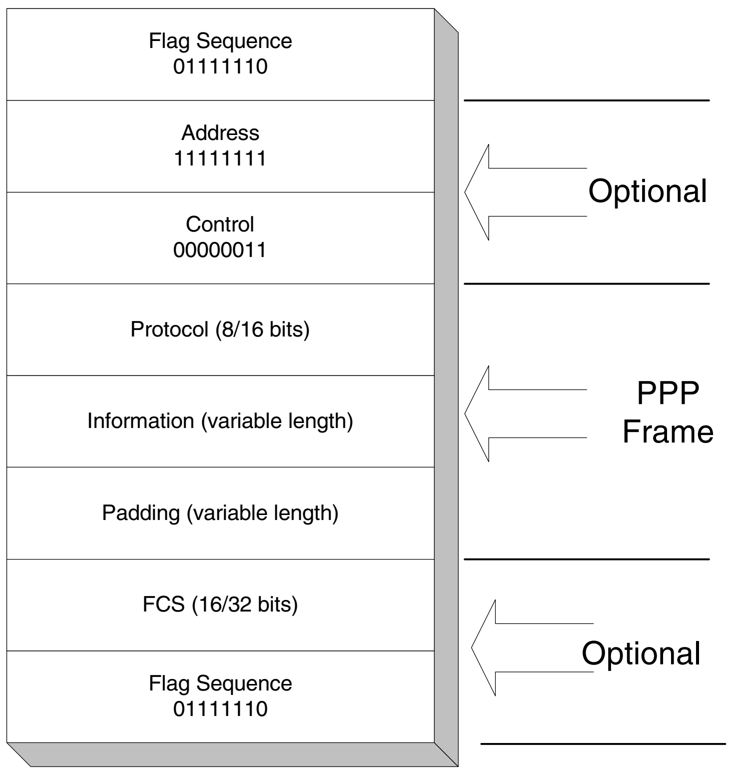
Following the Transmit System Interface, the CONGO device performs the following processing when in POS mode (**TX_POS = 1)**.

The CONGO performs a subset of this processing when in direct mapping mode (**TX_DIRECT_MAP** = 1). Specifically, in direct mapping mode the CONGO optionally performs the transparency processing, in order to support the insertion of the FIFO underflow stuff byte into the data stream.

5.2.1 Encapsulation of Packets in HDLC Frame

The HDLC frame defined for POS applications is illustrated in Figure 3. In POS mode (**TX_POS** = 1), each PPP packet received from the Link Layer is delineated using the Flag Sequence defined in RFC 1662, which is used to indicate both the beginning and end of an HDLC frame. The value of this Flag Sequence is 01111110 (hexadecimal 0x7e).

Figure 3. HDLC Frame for POS



As an option, the CONGO may insert a single flag to indicate both the end of one frame and the start of the following frame. This is controlled via the management interface; if **TX_POS_EOP_FLAG** = 1, the CONGO inserts separate flags to indicate the start and end of frame. If **TX_POS_EOP_FLAG** = 0 (the default), only a single Flag Sequence may be inserted.

In the special case when generation of the FCS field is inhibited (see section 5.2.3), **TX_POS_EOP_FLAG** is ignored by the CONGO, and start and end of frame Flag Sequences are always inserted. This is non-standard operation, as the FCS field is mandatory according to RFC 1662. This feature is required to insure proper operation at the receive side during testing periods in which the FCS is inhibited and single byte packets are possible.

5.2.2 Address and Control Fields

The HDLC POS standards specify two fields immediately following the start of frame Flag Sequence: an Address byte, always set to all 1's, and a Control byte, which is defined to be 00000011. In POS mode (**TX_POS** = 1), the CONGO will optionally insert these fields, if **TX_POS_ADRCTL_INS** = 1. It will not insert these fields if **TX_POS_ADRCTL_INS** = 0 (the default).

5.2.3 Frame Check Sequence (FCS) Field

In POS mode (**TX_POS** = 1), as an option, an FCS field is then calculated and inserted at the end of each frame. This option is controlled by register **TX_POS_FCS_INH**. A value of **TX_POS_FCS_INH = 0** (the default) enables the FCS. A value of **TX_POS_FCS_INH = 1** disables it. Two types of FCS fields have been defined in RFC 1662, a 16 bit check sequence (FCS-16) and a 32 bit check sequence (FCS-32). The device supports both types. **TX_POS_FCS_MODE = 0** places the device in FCS-32 mode, and is the default. **TX_POS_FCS_MODE = 1** places the device in FCS-16 mode.

The CONGO provides FCS-16 functionality, using the following generator polynomial:

$$1 + X^5 + X^{12} + X^{16}$$

The CONGO provides FCS-32 functionality, using the following generator polynomial:

$$1 + X + X^2 + X^4 + X^5 + X^7 + X^8 + X^{10} + X^{11} + X^{12} + X^{16} + X^{22} + X^{23} + X^{26} + X^{32}$$

The FCS field is calculated over all bits of the original packet, as well as the Address and Control fields. It does not include the Flag Sequence, nor the FCS field itself.

If **TX_POS_FCS_BIT_ORDR** = 0 (the default), the packet data is read into the shift register in big endian bit order (MSB first). If **TX_POS_FCS_BIT_ORDR** = 1, the packet data is read into the shift register in little endian bit order (LSB first). In either case, the packet data is restored to big endian order for processing after the FCS calculation.

The FCS is inverted and then transmitted least significant octet first, which contains the coefficient of the highest term. If **TX_POS_FCS_BIT_ORDR** = 0 (the default), the FCS is transmitted in big endian order. If **TX_POS_FCS_BIT_ORDR** = 1, the FCS is transmitted in little endian order.

5.2.4 Transparency

5.2.4.1 POS Mode

In the POS mode (**TX_POS** = 1, **TX_DIRECT_MAP** = 0), an octet stuffing procedure is performed at this point, which is referred to as Transparency Processing. A specific octet, Control Escape (01111101 or hexadecimal 0x7d) is used as a marker to indicate bytes that will require specific processing at the receive side. Control Escape is used to mark any occurrence of specific codes (see the following table) in the frame data.

After FCS computation, the CONGO examines the entire frame between any two Flag Sequences. Each occurrence of any code identified in Table 8 is replaced by a two octet sequence consisting of the Control Escape octet followed by the original octet exclusive-or’d with hexadecimal 0x20.

The CONGO performs transparency processing on the following byte sequences, with the single exception of the Flag Sequences that are inserted by the CONGO to delineate the frames. Occurrences of 0x7e in the payload (between Flag Sequences) are processed as described.

Table 8. Octet Values Handled by Transparency Processing

Octet Value (Hex) or Register	Name
0x7e	Flag Sequence
0x7d	Control Escape
TX_POS_FIFOUNDR_BYTE[7:0]	FIFO Underflow

As an example:

0x7e is encoded as 0x7d, 0x5e

0x7d is encoded as 0x7d, 0x5d

The transparency byte stuffing for the FIFO underflow byte code is controlled by the **TX_POS_FIFOUNDR_MODE** register, see section 5.2.5.3. If **TX_POS_FIFOUNDR_MODE =** 1, the FIFO byte code **TX_POS_FIFOUNDR_BYTE[7:0]** is inserted during periods of FIFO underflow, and the transparency byte stuffing for the FIFO byte code is enabled. If **TX_POS_FIFOUNDR_MODE** = 0, the FIFO byte code is not inserted, and the byte stuffing of the FIFO byte code is not performed.

5.2.4.2 Direct Map Mode

In the direct mapping mode (**TX_DIRECT_MAP** = 1), transparency byte stuffing on the Flag Sequence (0x7e) is not performed. If **TX_POS_FIFOUNDR_MODE** = 1, transparency byte stuffing is performed on the Control Escape (0x7d) and FIFO underflow code (**TX_POS_FIFOUNDR_BYTE[7:0]**). If **TX_POS_FIFOUNDR_MODE** = 0, all transparency processing is disabled.

5.2.5 SPE Creation

5.2.5.1 POS Operation (TX_POS = 1)

The POS stream is then mapped into the payload of the SONET/SDH Synchronous Payload Envelope (SPE). The POS octet boundaries are aligned with the SPE octet boundaries. As POS frames are variable in length, they are allowed to cross SPE boundaries.

When, during operation, there are no HDLC frames available for immediate insertion into the SPE, the Flag Sequence is transmitted to fill the time between HDLC frames. This is only done between complete frames. See section 5.2.5.3 for the case where a FIFO underflow occurs prior to the end of a packet.

The available information rate for PPP over SONET/SDH for STS-3c/STM-1 is 149.760 Mbps, which is the SPE rate with section, line and path overhead removed. This is the same super-rate mapping that is used for ATM and FDDI. For STS-12c/STM-4 (622.080 Mb/s) applications, the available bandwidth is 599.040 Mbps, the SPE rate with section, line and path overhead removed.

5.2.5.2 Direct Data Mapping (TX_DIRECT_MAP = 1)

The direct data is then mapped into the payload of the SONET/SDH Synchronous Payload Envelope (SPE). The data octet boundaries are aligned with the SPE octet boundaries.

In direct data mapping applications, the Link Layer device is responsible for insuring there is enough data in the CONGO to fill the SONET/SDH SPE. See section 5.2.5.3 for the case where a FIFO underflow occurs prior to the end of a packet.

5.2.5.3 FIFO Underflow

In POS mode (**TX_POS = 1)**, the transmit FIFO will become empty as a matter of course between packets, but should not become empty during a packet transmission, i.e. after a *TX_SOC/P* indication has been received, but before a *TX_EOP* indication has been received. If it does, the CONGO provides two options for handling FIFO underflow: the packet can be aborted, using the abort methods described in section 5.1.2.1; or a special code can be transmitted, **TX_POS_FIFOUNDR_BYTE[7:0],** filling the SPE until valid data is once again in the FIFO. Register **TX_POS_FIFOUNDR_MODE** controls the response; **TX_POS_FIFOUNDR_MODE = 0** indicates that the packet will be aborted. This is the default value. **TX_POS_FIFOUNDR_MODE = 1** indicates that the special FIFO underflow code, **TX_POS_FIFOUNDR_BYTE[7:0]** will be transmitted while the underflow condition exists. **TX_POS_FIFOUNDR_BYTE[7:0]** defaults to 0x50.

In direct mapping mode, (**TX_DIRECT_MAP = 1)**, the **TX_POS_FIFOUNDR_MODE** and **TX_POS_FIFOUNDR_BYTE[7:0]** can be enabled as well. If **TX_POS_FIFOUNDR_MODE = 0**, the CONGO does nothing except report FIFO underflow events; it is the responsibility of the user to insure that the correct amount of data is delivered to the CONGO in a timely manner. If **TX_POS_FIFOUNDR_MODE = 1**, the CONGO will insert the **TX_POS_FIFOUNDR_BYTE[7:0]** into the SONET/SDH SPE until valid data is once again present in the FIFO.

If a FIFO underflow event occurs, it is reported to the management interface by setting **TX_POS_FIFOUNDR_E = 1**. The CONGO contains an 8-bit FIFO underflow counter that counts every packet affected by a FIFO underflow event (in the direct mapping case, each new FIFO underflow event is counted). When the performance monitoring counters are latched, the value of this counter is latched to the **TX_POS_FIFOUNDR_ERRCNT[7:0]** register, and the FIFO underflow error counter is cleared. (See section 4.2).

If there has been at least one FIFO underflow event since the last rising edge of LATCH_EVENT, then the FIFO underflow error event bit, **TX_POS_FIFOUNDR_ERR_SECE**, is set.

5.3 Transmit ATM Processing

5.3.1 Transmit Data HEC Check

In ATM mode (**TX_POS = 0)**, the CONGO calculates the HEC value across the ATM cell header (the first four octets) of the transmit data. The HEC calculation follows the procedure used in section 5.3.4, including the use of the **TX_ATM_HEC_ENH** register. HEC errors are reported to the management interface by setting the **TX_ATM_HEC_ERR_E** event bit to 1. This HEC check can be inhibited by setting **TX_ATM_UTP_HEC_INH** = 1.

Register **TX_ATM_HEC_UDF** defines the location of the ATM HEC within the two User Defined bytes in the Utopia ATM data structure (see section 7.9.2). If **TX_ATM_HEC_UDF** = 0, the HEC is located in UDF1. If = 1, the HEC is located in UDF2.

5.3.2 Transmit Valid Cell Count

In ATM mode (**TX_POS** = 0), the CONGO contains an ATM cell counter that counts every ATM cell (including idle cells) received from the ATM Layer that appear at the Utopia interface. When the performance monitoring counters are latched (LATCH_EVENT transitions high), the value of this counter is latched to the **TX_ATM_CELL_CNT[20:0]** register, and the ATM cell counter is cleared. (See section 4.2).

5.3.3 SPE Payload Creation

5.3.3.1 ATM Cells into STS-3c/AU-4

The bit rate available for the ATM cells (user information cells, signalling cells, OAM cells, unassigned cells and cells used for cell rate decoupling) excluding SONET overhead packets is 149.760 Mb/s.

For STS-3c/AU-4 applications, the CONGO device maps the ATM cell stream into a C-4 container (VC-4 without the POH column). The ATM cell boundaries are aligned with the STS-3c/STM-1 octet boundaries. Since the C-4 capacity (2340 octets) is not an integer multiple of the cell length (53 octets), a cell may cross a C-4 boundary.

5.3.3.2 ATM Cells into STS-12c/AU-4-4c

The bit rate available for the ATM cells (user information cells, signalling cells, OAM cells, unassigned cells and cells used for cell rate decoupling) excluding SONET overhead packets is 599.040 Mb/s.

For STS-12c/AU-4-4c applications, the CONGO device maps the ATM cell stream into a C-4-4c container (VC-4-4c without the POH and fixed stuff columns). The ATM cell boundaries are aligned with the STS-12c/STM-4 octet boundaries. Since the C-4-4c capacity (9360 octets) is not an integer multiple of the cell length (53 octets), a cell may cross a C-4-4c boundary.

5.3.3.3 Idle Cell Stuffing

ATM idle cell stuffing is used when necessary to match the rate of ATM cell stream with the C-4 or C-4-4c.

An ATM idle cell is defined as follows:

Table 9. Pattern for Default Idle Cell

	Octet 1	Octet 2	Octet 3	Octet 4	Octet 5
Header pattern	00000000	00000000	00000000	00000001	HEC = valid code 01010010
Note 1 - The default content of the information field is “01101010” repeated 48 times. Note 2 - There is no significance to any of these individual header fields from the point of view of the ATM layer, as idle cells are not passed to the ATM layer.					

The CONGO provides user programmable fields within the idle cell. The format of an ATM cell header across the UNI is illustrated in the following table:

Table 10. ATM Cell Header Format

ATM Cell Header							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GFC (Generic Flow Control)				VPI (Virtual Path Identifier)			
VPI				VCI(Virtual Channel Identifier)			
VCI							
VCI				PTI (Payload Type Indicator)			CLP (Cell Loss Priority)
HEC (Header Error Control)							

The CONGO allows the user to provision the GFC, PTI and CLP fields of the idle cells, via registers **TX_ATM_IDLE_GFC[3:0]**, **TX_ATM_IDLE_PTI[2:0]** and **TX_ATM_IDLE_CLP**. The default values for these fields is all 0’s for GFC and PTI, and 1 for CLP (see Table 9). All other fields within the first four bytes of the header are set to 0. A valid HEC field is calculated for the idle cell, according to section 5.3.4.

The CONGO also allows the user to provision the contents of the 48 information octets of the idle cell, via register **TX_ATM_IDLE_DATA[7:0]**. The default value of this register is 01101010.

5.3.4 Header Error Control (HEC) Sequence Generation

The CONGO now optionally calculates the HEC value across the entire ATM cell header (the first four octets) and inserts the result in the appropriate header field. This option is controlled by register **TX_ATM_HEC_INH**. A value of **TX_ATM_HEC_INH = 0** enables the HEC. A value of **TX_ATM_HEC_INH = 1** disables it. When disabled, the CONGO passes through the HEC byte received from the ATM Layer.

A CRC-8 calculation is used to produce the HEC octet, using the following generator polynomial:

$$X^8 + X^2 + X + 1$$

As another configurable option to improve the cell delineation process, the CONGO supports the addition (modulo 2) of the bit pattern 01010101 to the 8 bit HEC before being inserted into the last octet of the header.This option is controlled by register **TX_ATM_HEC_ENH**. A value of **TX_ATM_HEC_ENH = 1** enables the modulo 2 addition of the alternating bit pattern (0x55) to the HEC. A value of **0** disables it. The default is 1.

5.4 Scrambling

After HDLC or ATM processing, the data is scrambled using a self-synchronizing $X^{43} + 1$ scrambler. In all modes, register **TX_SCR_INH** controls the operation of the scrambler. When **TX_SCR_INH = 0** (the default), the scrambler is enabled. When **TX_SCR_INH = 1**, operation of the scrambler is inhibited.

The CONGO provides a self-synchronizing scrambler based on the following generator polynomial:

$$X^{43} + 1$$

5.4.1 ATM Scrambler Operation

In ATM mode (**TX_POS** = 0), the operation of the scrambler adheres to the following requirements:

- the scrambler randomizes the bits of the information fields only
- during the five octet header the scrambler operation is suspended and the scrambler state retained

5.4.2 HDLC Scrambler Operation

In POS mode (**TX_POS** = 1), the scrambler scrambles the whole SPE payload, including the FCS and the flags.

5.4.3 Direct SPE Mapping Scrambler Operation

In direct data mode (**TX_DIRECT_MAP** = 1), the scrambler randomizes the entire SPE payload.

5.5 SPE/VC Generation

At this point in the transmission flow, POS packets, ATM cells or direct data have been encapsulated into a SONET/SDH SPE/VC. From this point on, the three modes operate identically.

The Synchronous Payload Envelope/Virtual Container (SPE/VC) Generation block multiplexes bytes from the system interface with Path Overhead (POH) bytes that it generates to create the SPE for SONET or VC for SDH.

5.5.1 SPE/VC Structure

The first column of the SPE/VC is the POH. The ordering of these 9 bytes is shown below for SONET and SDH.

SONET POH:	SDH POH:
J1	J1
B3	B3
C2	C2
G1	G1
F2	F2
H4	H4
Z3	F3
Z4	K3
Z5	N1

The structure of the STS-12c SPE or VC-4-4c is shown in Figure 4.

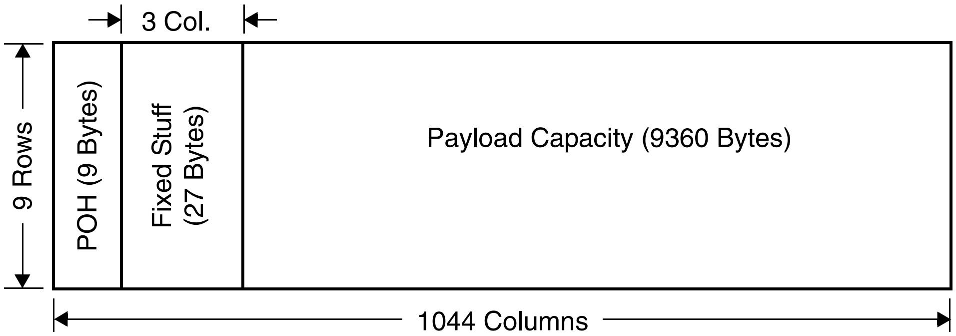


Figure 4: STS-12c SPE or VC-4-4c Structure

The structure of the STS-3c SPE or VC-4 is shown in Figure 5.

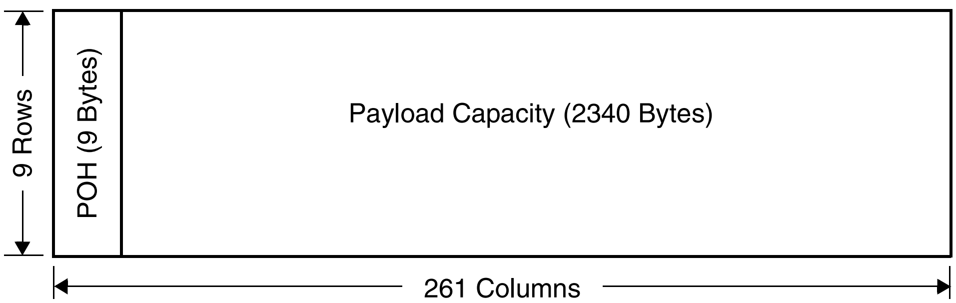


Figure 5. STS-3c SPE or VC-4 Structure

5.5.2 POH

There are 9 bytes of path overhead. The first byte of the path overhead is the path trace byte, J1. Its location with respect to the SONET/SDH TOH/SOH is indicated by the associated STS/AU pointer (see section 6.5.2). The following sections define the transmitted values of the POH bytes. Where the byte names differ between SONET and SDH, the SONET name will be listed first.

5.5.2.1 Path Trace (J1)

The CONGO can be provisioned to transmit either a 16-byte or a 64-byte path trace message in the J1 byte. The messages are stored in **TX_J1_[63:0]_[7:0]**. If **TX_J1SEL** = 0, the J1 byte is transmitted repetitively as the 16-byte sequence in **TX_J1_[15]_[7:0]** down to **TX_J1_[0]_[7:0]**. Otherwise, the 64-byte sequence in **TX_J1_[63]_[7:0]** down to **TX_J1_[0]_[7:0]** is transmitted. (The 16-byte sequence is normally used in the SDH mode, and the 64-byte sequence in the SONET mode.)

5.5.2.2 Path BIP-8 (B3)

The Bit Interleaved Parity 8 (BIP-8) is transmitted as even parity (normal) if **B3_INV** = 0. Otherwise, odd parity (incorrect) is generated. The BIP-8 is calculated over all bits of the previous SPE/VC (including the POH) and placed into the B3 byte of the current SPE/VC.

By definition of BIP-8, the first bit of B3 provides parity over the first bit of all bytes of the previous SPE/VC, the second bit of B3 provides parity over the second bit of all bytes of the previous SPE/VC, etc.

5.5.2.3 Signal Label (C2)

The signal label byte indicates the composition of the SPE/VC. The provisioned value, **TX_C2_[7:0]**, is inserted into the generated C2 bytes.

5.5.2.4 Path Status (G1)

Path REI. The Receive Side monitors B3 bit errors in the received SPE/VC (see section 6.7.2). The number of B3 errors detected each frame (0 to 8) is transferred from the Receive Side to the Transmit Side for insertion into the transmit path status byte, G1, as a Remote Error Indication.

If **FORCE_G1ERR** = 1, the 4 MSBs of G1 will continuously be transmitted as 1000 (for testing purposes). Else if **PREI_INH** = 0, they are set to the binary value (0000 through 1000, indicating between 0 and 8) equal to the number of B3 errors most recently detected by the Receive Side POH monitoring block. Otherwise, they are set to all zeros.

Path RDI. Bit 5 of G1 can be used as a Path/AU Remote Defect Indication, RDI-P, or bits 5, 6, and 7 of G1 can be used as an enhanced RDI-P indicator. The values transmitted in bits 5, 6, and 7 of G1 are taken either from the **TX_G1_[2:0]** registers (if **PRDI_AUTO** = 0), or the CONGO automatically generates an enhanced RDI signal (if **PRDI_AUTO** = 1 and **PRDI_ENH** = 1), or a one bit RDI signal (if **PRDI_AUTO** = 1 and **PRDI_ENH** = 0). The values transmitted in bits 5, 6, and 7 of G1 are shown in Table 31.

Table 11. Path RDI Bit Values

PRDI_ AUTO	PRDI_ ENH	RX_PAIS || RX_LOP	RX_UNEQ	RX_PLM || RX_ATM_LCD	G1 Bits 5, 6, & 7
0	x	x	x	x	**TX_G1_[2:0]**
1	0	1	x	x	100
		0	x	x	000
	1	1	x	x	101
		0	1	x	110
		0	0	1	010
		0	0	0	001

If **PRDI_AUTO** = 1, the values shown above are transmitted for a minimum of 20 frames. Once 20 frames have been transmitted with the same value, the value corresponding to the current state of the defect indication values listed in Table 31 will be transmitted.

Bit 8 of G1 (the LSB) is unused, and it is set to 0.

5.5.2.5 Other POH Bytes

The remaining POH bytes are not supported by the CONGO and are transmitted as fixed all-zeros bytes. These include the path user channel (F2), the position indicator (H4), the path growth/user channel (Z3/F3), the path growth/path APS channel (Z4/K3), and the tandem connection monitoring (Z5/N1) bytes.

5.6 SONET/SDH Frame Generation

The SONET/SDH frame generation block creates an STS-12c/STM-4 or STS-3c/STM-1 by generating the Transport (Section) Overhead (TOH/SOH) bytes, filling the payload with bytes from SPE/VC, and scrambling all bytes of the SONET/SDH signal except for the first row of TOH/SOH bytes. The structure of an STS-12c/STM-4 is shown in Figure 6.

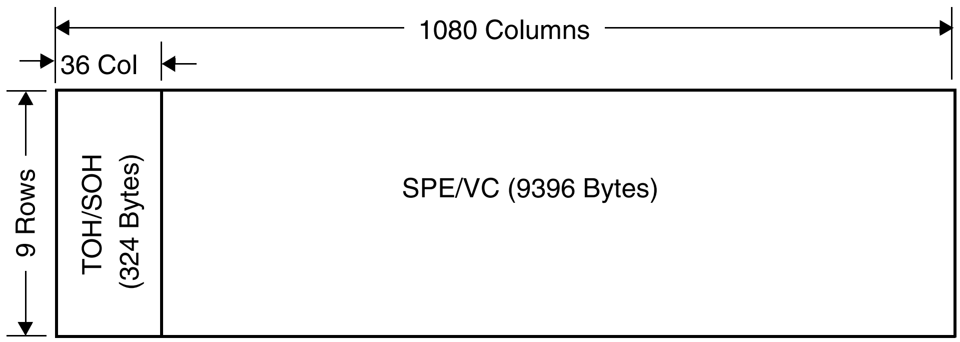


Figure 6: STS-12c/STM-4 Structure

In Figure 6, the first 36 columns of each row are shown as the TOH or SOH. This is not strictly true for SDH, because the first 36 columns of the fourth row of SDH frames is not considered part of the SOH. Instead, the Administrative Unit (AU) pointer bytes in this row are grouped with the VC to form an AU-4-4c. For simplicity, we will follow the SONET convention and include them with the TOH/SOH description.

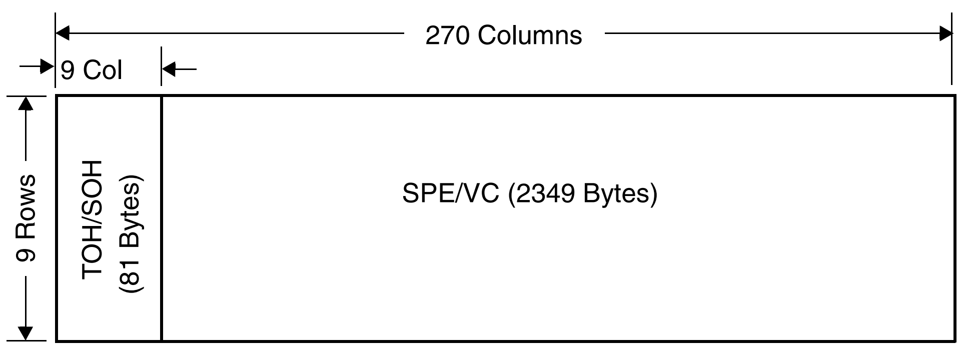


Figure 7: STS-3c/STM-1 Structure

For completeness, the structure of the STS-3c/STM-1 is illustrated also, in Figure 7. The first 9 columns of each row are shown as the TOH or SOH. This is not strictly true for SDH, because the first 9 columns of the fourth row of SDH frames is not considered part of the SOH. Instead, the Administrative Unit (AU) pointer bytes in this row are grouped with the VC to form an AU-4. Again, we will follow the SONET convention and include them with the TOH/SOH description.

5.6.1 Frame Alignment

The position of the generated frame is fixed with respect to the input, *TX_FRAME_IN*. A start-of-frame indication output, *TX_FRAME_OUT*, has a fixed but unspecified relationship to the *TX_FRAME_IN* input. The relationship of the 1 clock cycle wide pulses on *TX_FRAME_OUT* to the data bytes on the Transmit Line output *TX_DATA[7:0]* is controlled by the **TX_FOUT_BYTE_TYPE[1:0]** and **TX_FOUT_BYTE_NUMBER[3:0]** registers. For STS-12c/STM-4 operation (**TX_SIG_MODE** = 1), these registers should be provisioned as shown in Table 12, which is similar to Table 17.

Table 12. STS-12c/STM-4 Provisioning for TX_FOUT_BYTE_TYPE[1:0] and TX_FOUT_BYTE_NUMBER[3:0]

Data on *TX_DATA[7:0]* when *TX_FRAME_OUT* = 1	TX_FOUT_BYTE_TYPE[1:0] allowed range = {0 to 3} decimal	TX_FOUT_BYTE_NUMBER[3:0] allowed range = {0 to 11} decimal
last byte of frame	00	0000
first A1 byte	00	0001
. . .	. . .	. . .
eleventh A1 byte	00	1011
last A1 byte	01	0000
first A2 byte	01	0001
. . .	. . .	. . .
last Z0 byte	11	0000
first byte after last Z0 byte	11	0001
. . .	. . .	. . .
eleventh byte after last Z0 byte	11	1011

For STS-3c/STM-1 operation (**TX_SIG_MODE** = 0), these registers should be provisioned as shown in Table 13. Note that only the two LSBs of register **TX_FOUT_BYTE_NUMBER** are used.

Table 13. STS-3c/STM-1 Provisioning for TX_FOUT_BYTE_TYPE[1:0] and TX_FOUT_BYTE_NUMBER[3:0]

Table 14. Data on *TX_DATA[7:0]* when *TX_FRAME_OUT* = 1	TX_FOUT_BYTE_TYPE[1:0] allowed range = {0 to 3} decimal	TX_FOUT_BYTE_NUMBER[1:0] allowed range = {0 to 2} decimal
last byte of frame	00	00
first A1 byte	00	01
second A1 byte	00	10
third A1 byte	01	00
first A2 byte	01	01
second A2 byte	01	10
third A2 byte	10	00
J0 byte	10	01
first Z0 byte	10	10
last Z0 byte	11	00

Table 14. Data on *TX_DATA[7:0]* when *TX_FRAME_OUT* = 1	TX_FOUT_BYTE_TYPE[1:0] allowed range = {0 to 3} decimal	TX_FOUT_BYTE_NUMBER[1:0] allowed range = {0 to 2} decimal
first byte after last Z0 byte	11	01
second byte after last Z0 byte	11	10

5.6.2 Payload Generation

The SONET or SDH payload is normally filled with bytes from the SPE/VC. The J1 byte of the SPE/VC is placed into column 37 of row 1 of the SONET/SDH frame when the CONGO is creating a STS-12c/STM-4 (**TX_SIG_MODE = 1**). The J1 byte of the SPE/VC is placed into column 10 of row 1 in STS-3c/STM-1 mode (**TX_SIG_MODE = 0**).

5.6.2.1 AIS Generation

Normal generation of SONET/SDH payload is suspended during transmission of the Line (Multiplex Section, MS) Alarm Indication Signal, LAIS, or the Path (Administrative Unit, AU) AIS signals, PAIS. AIS generation is controlled by the **TX_LAIS** and **TX_PAIS** registers.

If **TX_LAIS** or **TX_PAIS** = 1, the entire payload (9396 or 2349 bytes) is filled with all-ones bytes.

5.6.2.2 Unequipped Generation

Unless AIS is active, unequipped SPE/VC (all SPE/VC bytes are filled with all-zeros) is generated if **TX_UNEQ** = 1.

5.6.3 TOH/SOH Generation

The SONET TOH bytes are generally the same as the SDH SOH bytes.The following sections define the values generated for all TOH/SOH bytes. Where the byte names differ between SONET and SDH, the SONET name will be listed first. Entries that are blank in Table 15 are SONET undefined or SDH non-standardized reserved bytes. The CONGO fills these bytes with all zeros.

Table 15. STS-12c/STM-4 TOH/SOH

	Column					
Row	1	2-12	13	14-24	25	26-36
1	A1[1]	A1[2:12]]	A2[1]	A2[2:12]	J0[1]	Z0[2:12]
2	B1		E1		F1	
3	D1		D2		D3	
4	H1[1]	H1[2:12]	H2[1]	H2[2:12]	H3[1]	H3[2:12]
5	B2[1]	B2[2:12]	K1		K2	
6	D4		D5		D6	
7	D7		D8		D9	
8	D10		D11		D12	
9	S1	Z1[2:12][b]	Z2[1][b]	Z2[2][b], M1, Z2[4:12][b]	E2	

[b]The Z1 and Z2 bytes are non-standardized reserved bytes for STM-4.

Table 16. STS-3c/STM-1 TOH/SOH

	Column					
Row	1	2-3	4	5-6	7	8-9
1	A1[1]	A1[2,3]	A2[1]	A2[2,3]	J0[1]	Z0[2,3]
2	B1		E1		F1	
3	D1		D2		D3	
4	H1[1]	H1[2,3]	H2[1]	H2[2,3]	H3[1]	H3[2,3]
5	B2[1]	B2[2,3]	K1		K2	
6	D4		D5		D6	
7	D7		D8		D9	
8	D10		D11		D12	
9	S1	Z1[2,3][b]	Z2[1][b]	Z2[2][b], M1	E2	

[b]The Z1 and Z2 bytes are non-standardized reserved bytes for STM-1

5.6.3.1 AIS Generation

Normal generation of TOH/SOH bytes is suspended during transmission of LAIS or PAIS. If **TX_LAIS** = 1, the first 3 rows of the TOH/SOH are generated normally, but the remainder of the TOH/SOH (as well as all SPE/VC bytes) are transmitted as all-ones bytes. If **TX_PAIS** = 1, all rows of the TOH/SOH are generated normally, except for the pointer bytes in row 4. The H1, H2, and H3 bytes (as well as all SPE/VC bytes) are transmitted as all-ones bytes.

5.6.3.2 Frame Bytes (A1 and A2)

The frame bytes are normally generated with the fixed patterns:

- A1: 1111_0110 = F6
- A2: 0010_1000 = 28

For testing purposes, A1 and A2 can be generated with errors. If **A1A2_ERR**= 0, no errors are inserted. When **A1A2_ERR** is one, then m consecutive frames (where m is the binary equivalent of **A1A2_ERR_NUM[2:0]**) in each group of 8 frames, is generated with A1 and A2 exclusive-ORed with the contents of **A1A2_ERR_PAT[15:0]**. The MSB of A1 is XORed with **A1A2_ERR_PAT[15]**, and the LSB of A2 is XORed with **A1A2_ERR_PAT[0]**.

5.6.3.3 Section Trace/Regenerator Section Trace (J0) and Section Growth/Spare (Z0)

Section Trace. Over periods of 16 consecutive frames, the CONGO continuously transmits the 16-byte pattern contained in **TX_J0_[15:0]_[7:0]**. The bytes are transmitted in descending order starting with **TX_J0_[15]_[7:0]**.

The SDH G.707 standard states that a 16-byte section trace frame containing the Section Access Point Identifier (SAPI) defined in clause3/G.831 should be transmitted continuously in consecutive J0 bytes. Note that only the frame start marker byte should contain a 1 in its MSB.

The Section Trace function is not currently defined for SONET. Unless a similar section trace is defined for SONET, all of the **TX_J0** bytes should be filled with 0000_0001 so that a decimal 1 is transmitted continuously in J0.

Section Growth/Spare. The Z0 bytes are transmitted in order as the binary equivalent of 2 to 12 in STS-12c/STM-4 (**TX_SIG_MODE = 1**) mode, or 2 to 3 in STS-3c/STM-1 (**TX_SIG_MODE = 0**) mode (this is specified in GR-253).

5.6.3.4 Section BIP-8 (B1)

The B1 Bit Interleaved Parity 8 (BIP-8) is transmitted as even parity (normal) if **B1_INV** = 0. Otherwise, odd parity (incorrect) is generated. The BIP-8 is calculated over all bits of the previous STS-12c/STM-4 or STS-3c/STM-1 frame after scrambling and placed into the B1 byte of the current frame before scrambling.

By definition of BIP-8, the first bit of B1 provides parity over the first bit of all bytes of the previous frame, the second bit of B1 provides parity over the second bit of all bytes of the previous frame, etc.

5.6.3.5 Orderwire (E1 and E2) and Section User Channel (F1)

The orderwire bytes are defined for the purpose of carrying two 64kb/s digitized voice signals. The F1 byte is available for use by the network provider. The transmit block accepts three serial inputs, *TX_E1_DATA*, *TX_E2_DATA*, and *TX_F1_DATA*, for insertion into the transmitted E1, E2, and F1 bytes. A single 64 kHz clock (*TX_E1E2F1_CLK*) is output from the CONGO in order to provide a timing reference for these three serial inputs. The first bit (the MSB) of these bytes should be aligned with the incoming frame start pulse, *TX_FRAME_IN*. The received E1, E2 and F1 bytes will be inserted into the outgoing SONET/SDH frame which follows the reception of the last bit of the E1, E2 and F1 bytes.

5.6.3.6 Data Communications Channels, DCC, (D1-D12)

There are two DCCs defined in the TOH/SOH. The Section/Regenerator Section DCC uses the D1, D2, and D3 bytes to create a 192 kb/s channel. The Line/Multiplex Section DCC uses bytes D4 through D12 to create a 576 kb/s channel.

The Transmit Side accepts DCC data on two serial inputs, *TX_SDCC_DATA* and *TX_LDCC_DATA*. In order to assure bit synchronization, the Transmit Side outputs two clocks, *TX_SDCC_CLK* at 192 kHz and *TX_LDCC_CLK* at 576 kHz. The clock signals enable the retiming of bits from *TX_SDCC_DATA* and *TX_LDCC_DATA* into registers for inserting into the TOH/SOH. The *TX_SDCC_DATA* and *TX_LDCC_DATA* inputs should change on the falling edges of *TX_SDCC_CLK* and *TX_LDCC_CLK*, since the retiming is done on the rising edges.

5.6.3.7 Pointer Bytes (H1, H2) and Pointer Action Byte (H3)

The H1 and H2 bytes contain 3 fields, as is shown in Figure 8.

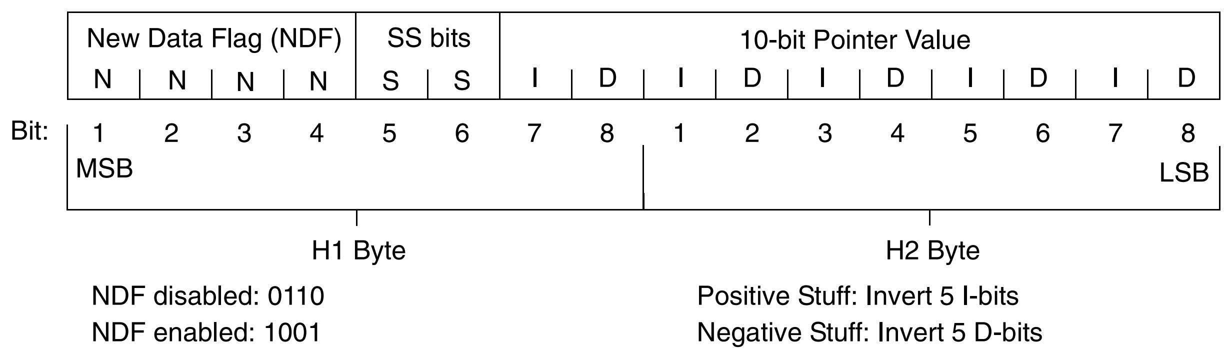


Figure 8: Pointer Byte Fields

Because the SPE/VC is generated synchronously with the TOH, variable pointer generation is not required. Instead, active H1 and H2 bytes are generated with the fixed pointer value of 522 (decimal) = 10_0000_1010 (binary), and the H3 bytes are fixed at all-zeros. Thus, the J1 byte of the SPE/VC is placed into column 37 of row 1 of the SONET/SDH frame in the STS-12c/STM-4 mode (**TX_SIG_MODE = 1**). The J1 byte of the SPE/VC is placed into column 10 of row 1 in the STS-3c/STM-1 mode (**TX_SIG_MODE = 0**).

AIS Generation. If **TX_LAIS** or **TX_PAIS** is active, the H1, H2, and H3 bytes are transmitted as all-ones. When **TX_LAIS** or **TX_PAIS** transitions so that both bits become 0, the CONGO transmits the first H1 byte in the next frame with an enabled New Data Flag. Succeeding frames are generated with the NDF field disabled in the first H1 byte.

Non-AIS Generation. The first H1-H2 byte pair is transmitted as a normal pointer, with

- NDF = 0110
- SS = **TX_SDH_PG**, 0
- Pointer Value = 10_0000_1010

all other H1-H2 byte pairs are transmitted as concatenation indication bytes, with

- NDF =1001
- SS = **TX_SDH_PG**, 0
- Pointer Value = 11_1111_1111.

5.6.3.8 Line/MS BIP-96/24 (B2)

In the following B2 description, the numbers vary slightly dependent upon the mode of the device (STS-12c mode vs. STS-3c). To describe the operation of both cases, the following convention will be used to identify the requirement that applies to each mode: STS-12c [STS-3c]. The STS-3c/STM-1 requirement will follow the STS-12c/STM-4 requirement in braces.

There are 12 [3] B2 bytes in the TOH/SOH, and together they provide a BIP-96 [BIP-24] error detection capability. Each B2 byte provides BIP-8 parity over bytes in 1 of 12 [3] groups of bytes in the previous frame. The B2 byte in column j, provides BIP-8 parity over bytes in the previous frame (except those in the first 3 rows of TOH/SOH) that appear in columns j + 12k (j + 3k), where k = 0 through 89. The BIP-8 is transmitted as even parity (normal) if **B2_INV** = 0. Otherwise, odd parity (incorrect) is generated. The BIP-8 values are calculated over bytes in the previous STS-12c/STM-4 [STS-3c/STM-1] frame before scrambling and placed into the B2 bytes of the current frame before scrambling.

5.6.3.9 APS Channel and Line/MS AIS/RDI (K1 and K2)

K1 and the 5 MSBs of K2 are used for automatic protection switching (APS) signaling. The 3 LSBs of K2 are used as an AIS or Remote Defect Indication (RDI) at the line/MS level, and in SONET, they are also used for APS signalling. The CONGO inserts **TX_K1_[7:0]** in the transmitted K1 bytes and **TX_K2_[7:3]** in the transmitted 5 MSBs of K2 bytes.

The 3 LSBs of K2 are controlled from 3 sources. In order of priority, these are

- If **TX_LAIS** = 1, they are transmitted as all-ones (as are all line/MS overhead bytes)
- else if **LRDI_INH** = 0 and if any of (**RX_LOS AND NOT RX_LOS_INH)***,* **RX_LOF, RX_LOC** or **RX_LAIS** = 1, they are transmitted as 110. Any time this particular event is active, the K2 is set to 110 for a minimum of 20 frames.
- else **TX_K2_[2:0]** is transmitted.

RX_LOS can be active high (**RX_LOS_LEVEL** = 0, the default) or active low (**RX_LOS_LEVEL** = 1). Internally, if **RX_LOS_LEVEL** = 1, *RX_LOS* is inverted to produce **RX_LOS**.

Requirements R6-180 through R6-182 of GR-253 specify that RDI should be inserted and removed within 125 us of detection and removal of received LOS, LOF, or LAIS.

5.6.3.10 Synchronization Status (S1)

The 4 LSBs of this byte convey synchronization status messages. The transmitted S1 byte is set equal to **TX_S1_[7:0]**.

5.6.3.11 Line/MS REI (M1)

The Receive Side monitors B2 bit errors in the received signal. The number of B2 errors detected each frame can range from 0 to 96 B2 bits per frame in STS-12c/STM-4 mode, or from 0 to 24 B2 bits per frame in STS-3c/STM-1 mode. The line/MS Remote Error Indication (REI) byte, the M1 byte, normally conveys the count of B2 errors detected in the received signal.

The user can force the transmission of REI error indications by setting **TX_M1_ERR** = 1. This causes a count of either 96 (for STS-12c/STM-4 mode) or 24 (STS-3c/STM-1 modes) to be transmitted in the M1 byte. Else if **LREI_INH** = 0, the M1 byte is set equal to the most recent B2 error count. Otherwise, the M1 byte is set to all zeros.

5.6.3.12 Growth/Undefined (Z1 and Z2)

The use of the Z1 and Z2 bytes is not standardized. The CONGO fills these bytes with all-zeros.

5.6.4 Scrambling

The input is scrambled with a frame synchronous scrambling sequence generated from the polynomial **$g(x) = x^7 + x^6 + 1$**. The scrambler is initialized to 1111111 at the beginning of the first SPE/VC byte (the byte in column 37 of row 1 in STS-12c/STM-4 mode, or the byte in column 10 of row 1 in STS-3c/STM-1 mode), and it scrambles the entire SONET/SDH signal except for the first row of TOH/SOH. For testing purposes, the scrambler can be disabled by setting the **SCRINH** bit to 1.

6.0 Processing of Data in the Receive Direction

6.1 T-to-R Loopback and LOC

The CONGO receive section can be configured to loopback the generated transmit signal if **SONET_T_TO_R_LOOP** = 1. Otherwise, the received signal from the SONET/SDH interface is selected. While in loopback, the *TX_SONETCLK* input is used to clock the receiver framer and other receiver circuitry. If loopback is not selected, the *RX_SONETCLK* input is used to clock this circuitry.

The *RX_SONETCLK* input is monitored for loss of clock using the *TX_CLK* input. If no transitions are detected on *RX_SONETCLK* for 16 periods of *TX_CLK*, the **RX_LOC** bit is set. It is cleared when transitions are detected.

The **RX_LOC_D** delta bit is set if **RX_LOC** transitions from either a 0 to a 1, or from a 1 to a 0.

6.2 STS-12c/STM-4 Framer

The CONGO Receive Framer operates in two modes. If **RX_FRMR_INH** = 0 (the default), the CONGO device framer is enabled. In this mode, the parallel input signal is not assumed to be byte aligned. The SONET/SDH framer locates the framing bytes in the selected data signal, and by doing so is able to find byte alignment and determine the position of all TOH/SOH bytes. After finding frame, the framer shifts the data so that its output data is byte aligned. It also descrambles the data, performs B1 monitoring, and provides frame counter outputs to the TOHMON and Pointer Interpreter blocks.

If **RX_FRMR_INH** = 1, the framer circuitry in the CONGO is bypassed. In this mode, the CONGO requires a frame start indication, *RX_FRAME_IN*, as well as data and clock. The data may have originated from a high-speed device that performs framing and serial-to-parallel conversion of an STS-12c/STM-4 signal or from a high-speed device that locates frame, does byte disinterleaving, and performs serial-to-parallel conversion of an STS-48/STM-16 signal.

6.2.1 Framer Enabled Operation

If the framer is enabled (**RX_FRMR_INH** = 0), the CONGO devices performs the following framer processing:

When the framer state machine is out-of-frame (**RX_OOF** = 1), it searches for the 32-bit A1-A1-A2-A2 framing byte sequence of 0xF6F6_2828. This pattern may start on any of the 8 input data lines and span up to 5 input bytes. When the framer finds 2 successive sequences separated in time by 125 μs that exactly match the framing pattern, it goes into frame (**RX_OOF** = 0) and byte aligns its output data bus.

The framer remains in-frame, until it receives 5 successive frames with at least 1 bit error in the A1-A1-A2-A2 framing pattern. When this occurs, **RX_OOF** is set to 1, and a new frame search is begun.

The framer also provides a loss-of-frame indication. If **RX_OOF** is active (1) continuously for 24 consecutive frames (3 ms), the **RX_LOF** bit is set to 1. Once **RX_LOF** is set, it remains high until **RX_OOF** is inactive (0) continuously for either 24 (if **RX_LOF_ALG** = 1) or 8 (if **RX_LOF_ALG** = 0) consecutive frames.

The out-of-frame and loss-of-frame indications are also available as CONGO outputs, *RX_OOF_OUT* and *RX_LOF_OUT*. The **RX_OOF_D** and **RX_LOF_D** delta bits contribute to the summary interrupt, and the **RX_OOF_SECE** and **RX_LOF_SECE** second event bits are set at the end of each second that the **RX_OOF** and **RX_LOF** bits are in the active state at any time during the second.

The framer also outputs the *RX_FRAME_OUT* signal. This signal is nominally 8 kHz and is high during the first row of overhead of the received frame. The *RX_FRAME_OUT* signal is also used for byte alignment of the received E1, E2, and F1 data outputs (see section 6.4.1).

6.2.2 Framer Bypass Operation

If the framer is bypassed (**RX_FRMR_INH** = 1), the CONGO devices performs the following:

An external framer must supply the CONGO with a start of frame indication, *RX_FRAME_IN.* The CONGO sets its internal frame counter when the *RX_FRAME_IN* input transitions from 0 to 1. The relationship of the start of frame to the 0 to 1 transition of *RX_FRAME_IN* is provisioned through the **RX_FIN_BYTE_TYPE[1:0]** and

RX_FIN_BYTE_NUMBER[3:0] registers. These provisioning registers allow the CONGO to interface directly to external framers that supply a start of frame indication anywhere between the last byte of the SONET/SDH frame to the eleventh payload byte following the first row of section/multiplex section overhead.The values that should be provisioned in the **RX_FIN_BYTE_TYPE[1:0]** and **RX_FIN_BYTE_NUMBER[3:0]** registers for STS-12c/STM-4 operation (**RX_SIG_MODE** = 1) are given in Table 17.

Table 17. STS-12c/STM-4 Provisioning for RX_FIN_BYTE_TYPE[1:0] and RX_FIN_BYTE_NUMBER[3:0]

Data on *RX_DATA[7:0]* when *RX_FRAME_IN* transitions to 1	RX_FIN_BYTE_TYPE[1:0] allowed range = {0 to 3} decimal	RX_FIN_BYTE_NUMBER[3:0] allowed range = {0 to 11} decimal
last byte of frame	00	0000
first A1 byte	00	0001
second A1 byte	00	0010
. . .	. . .	. . .
eleventh A1 byte	00	1011
last A1 byte	01	0000
first A2 byte	01	0001
. . .	. . .	. . .
eleventh A2 byte	01	1011
last A2 byte	10	0000
J0 byte	10	0001
. . .	. . .	. . .
last Z0 byte	11	0000
first byte after last Z0 byte	11	0001
. . .	. . .	. . .
eleventh byte after last Z0 byte	11	1011

The values that should be provisioned in the **RX_FIN_BYTE_TYPE[1:0]** and **RX_FIN_BYTE_NUMBER[1:0]** registers for STS-3c/STM-1 operation (**RX_SIG_MODE** = 0) are given in Table 17. Note that only the two LSBs of the **RX_FIN_BYTE_NUMBER** register are used.

Table 18. STS-3c/STM-1 Provisioning for RX_FIN_BYTE_TYPE[1:0] and RX_FIN_BYTE_NUMBER[1:0]

Data on *RX_DATA[7:0]* when *RX_FRAME_IN* transitions to 1	RX_FIN_BYTE_TYPE[1:0] allowed range = {0 to 3} decimal	RX_FIN_BYTE_NUMBER[3:0] allowed range = {0 to 2} decimal
last byte of frame	00	00

Table 18. STS-3c/STM-1 Provisioning for RX_FIN_BYTE_TYPE[1:0] and RX_FIN_BYTE_NUMBER[1:0]

Data on *RX_DATA[7:0]* when *RX_FRAME_IN* transitions to 1	**RX_FIN_BYTE_TYPE[1:0] allowed range = {0 to 3} decimal**	**RX_FIN_BYTE_NUMBER[3:0] allowed range = {0 to 2} decimal**
first A1 byte	00	01
second A1 byte	00	10
last A1 byte	01	00
first A2 byte	01	01
second A2 byte	01	10
last A2 byte	10	00
J0 byte	10	01
first Z0 byte	10	10
last Z0 byte	11	00
first byte after last Z0 byte	11	01
second byte after last Z0 byte	11	10

Based on the *RX_FRAME_IN* input and the values of **RX_FIN_BYTE_TYPE[1:0]** and **RX_FIN_BYTE_NUMBER[3:0]**, the CONGO monitors all A1 and A2 bytes for errors. The **RX_OOF** and **RX_LOF** monitors operate as described in section 6.2.1. However, while out of frame in the framer bypass mode, the CONGO does not search for frame. It continues to keep its internal frame counter aligned with the *RX_FRAME_IN* input.

6.2.3 Descrambling

In either framer enabled or framer bypass mode, before the data is output from the Framer block, it can be descrambled using the same frame synchronous sequence that is used to scramble the transmit data. (See section 5.6.4). The descrambler is reset to 1111111 at the beginning of the first SPE/VC byte (the byte in column 37 of row 1 in STS-12c/STM-4 mode, or the byte in column 10 of row 1 in STS-3c/STM-1 mode), and it descrambles the entire SONET/SDH signal except for the first row of TOH/SOH. For testing purposes, the descrambler can be disabled by setting **DSCRINH** to 1.

6.2.4 B1 Monitor

In both modes, the CONGO checks the received B1 bytes for correct Bit Interleaved Parity 8 (BIP-8) values. Even parity BIP-8 is calculated over all bytes of each frame before descrambling. This value is then compared to the received B1 value in the following frame after descrambling. The comparison can result in from 0 to 8 mismatches (B1 bit errors).

The CONGO contains a 16-bit B1 error counter that either counts every B1 bit error (if **BIT_BLKCNT** = 0) or every frame with at least one B1 bit error (if **BIT_BLKCNT** = 1). When the performance monitoring counters are latched (LATCH_EVENT transitions high), the value of this counter is latched to the **B1_ERRCNT[15:0]** register, and the B1 error counter is cleared. (See section 4.2).

If there has been at least one B1 error since the last rising edge of LATCH_EVENT, then the B1 error second event bit, **B1ERR_SECE**, is set.

6.3 Transport Overhead Monitoring

The TOH/SOH monitoring block consists of J0, B2, K1K2, S1 and M1 monitoring. These TOH/SOH bytes are monitored for errors or changes in states.

6.3.1 J0 Monitoring

There are two modes of operation for J0 monitoring, one typically used in SONET applications, the other used in SDH applications.

In the **RX_SDH_J0** = 0 mode (SONET), J0 monitoring consists of examining the received J0 bytes for values that match consistently for 3 consecutive frames. When a consistent J0 value is received, it is written to **RX_J0_[15]_[7:0]**.

In the **RX_SDH_J0** = 1 case (SDH), the J0 byte is expected to contain a repeating 16-byte section trace frame that includes the Section Access Point Identifier. J0 monitoring consists of locking on to the start of the 16-byte section trace frame and examining the received section trace frames for values that match consistently for 3 consecutive section trace frames. When a consistent frame value is received, it is written to **RX_J0_[15:0]_[7:0]**. The first byte of the section trace frame (which contains the frame start marker) is written to **RX_J0_[15]_[7:0]**.

6.3.1.1 Framing

The MSBs of all section trace frame bytes are 0, except for the MSB of the frame start marker byte. The J0 monitor framer searches for 15 consecutive J0 bytes that have a 0 in their MSB, followed by a J0 byte with a 1 in its MSB. When this pattern is found, the framer goes into frame, **J0_OOF** = 0. Once the J0 monitor framer is in-frame, it remains in frame until 3 consecutive section trace frames are received with at least 1 MSB bit error. If **RX_SDH_J0** = 0, the J0 frame indication is held in the In-frame state, **J0_OOF** = 0. The **J0_OOF_D** delta bit is set when **J0_OOF** changes state.

6.3.1.2 Pattern Acceptance and Comparison

Once in frame, the J0 monitor block looks for 3 consecutive 16 byte (**RX_SDH_J0** = 1) or 1 byte (**RX_SDH_J0** = 0) section trace frames. When 3 consecutive identical frames are received, the accepted frame is stored in **RX_J0_[15:0]_[7:0]** (or **RX_J0_[15]_[7:0]** in the SONET mode).

Accepted frames are compared to the previous contents of these registers. When a new value is stored, the **RX_J0_D** delta bit is set.

6.3.2 BIP-96 (B2) Checking

In the following B2 description, the numbers vary slightly dependent upon the mode of the device (STS-12c mode vs. STS-3c). To describe the operation of both cases, the following convention will be used to identify the requirement that applies to each mode: STS-12c [STS-3c]. The STS-3c/STM-1 requirement will follow the STS-12c/STM-4 requirement in braces.

The CONGO checks the received B2 bytes for correct BIP-8 values. (The 12 [3] B2 bytes together form a BIP-96 [BIP-24].) Even parity BIP-96 [BIP-24] is calculated over all groups of 12 [3] bytes of each frame, except the first three rows of TOH (SOH in SONET and RSOH in SDH). The calculation is done on the received data after descrambling. This value is then compared to the B2 values in the following frame after descrambling. The comparison can result in from 0 to 96 [0 to 24] mismatches (B2 bit errors). The number of B2 bit errors detected each frame may be inserted into the transmitted M1 byte (see section 5.6.3.11).

6.3.2.1 B2 Error Counting

The CONGO contains a 20-bit B2 error counter that either counts every B2 bit error (if **BIT_BLKCNT** = 0) or every frame with at least one B2 bit error (if **BIT_BLKCNT** = 1). When the performance monitoring counters are latched (LATCH_EVENT transitions high), the value of this counter is latched to the **B2_ERRCNT[19:0]** register, and the B2 error counter is cleared. (See section 4.2).

If there has been at least one B2 error since the last rising edge of LATCH_EVENT, then the B2 error second event bit, **B2ERR_SECE**, is set.

6.3.2.2 B2 Error Rate Threshold Blocks

For the purpose of determining whether or not the bit error rate of the received signal is above or below two different provisionable thresholds (the Signal Fail and the Signal Degrade conditions), the CONGO provides two B2 error rate threshold blocks. If the SF block or the SD block determines that the error rate is above the threshold, it sets **B2_ERR_SF** or **B2_ERR_SD**. The delta bits **B2_ERR_SF_D** or **B2_ERR_SD_D** are set if the corresponding error rate bit changes value.

For each error rate threshold block, the user may provision a BLOCK register and 2 pairs of THRESH and GROUP registers. In order to allow hysteresis in setting and clearing the state bits, each error rate threshold block has 1 pair of THRESH and GROUP registers for setting the state and 1 pair of THRESH and GROUP registers for clearing the state. Thus, the registers used in the error rate threshold blocks are

- while **B2_ERR_SF** = 0, determine if it should be set using: **B2_BLOCK_SF[7:0]**, **B2_THRESH_SET_SF[7:0]**, and **B2_GROUP_SET_SF[5:0]**
- while **B2_ERR_SF** = 1, determine if it should be cleared using: **B2_BLOCK_SF[7:0]**, **B2_THRESH_CLR_SF[7:0]**, and **B2_GROUP_CLR_SF[5:0]**
- while **B2_ERR_SD** = 0, determine if it should be set using: **B2_BLOCK_SD[15:0]**, **B2_THRESH_SET_SD[5:0]**, and **B2_GROUP_SET_SD[5:0]**
- while **B2_ERR_SD** = 1, determine if it should be cleared using: **B2_BLOCK_SD[15:0]**, **B2_THRESH_CLR_SD[5:0]**, and **B2_GROUP_CLR_SD[5:0]**

6.3.3 K1K2 Monitoring

The K1 and K2 bytes, which are used for sending Line/MS AIS or RDI and for APS signalling, are monitored for change in status.

6.3.3.1 Line/MS AIS Monitoring and LRDI Generation

The 3 LSBs of K2 can be used as an AIS or Remote Defect Indication (RDI) at the line/MS level.

If they are received as “111” for **K2_CONSEC[3:0]** consecutive frames, **RX_LAIS** is set, and the *RX_LAIS_OUT* output is high. If for **K2_CONSEC[3:0]** consecutive frames, they are not received as “111”, then **RX_LAIS** and *RX_LAIS_OUT* are cleared. The **RX_LAIS_D** delta bit is set when **RX_LAIS** changes state.

6.3.3.2 Line/MS RDI Monitoring

The 3 LSBs of K2 are also monitored for **K2_CONSEC[3:0]** consecutive receptions or non-receptions of “110”. When this is received, **RX_LRDI** is set or cleared. **RX_LRDI_D** is set when **RX_LRDI** changes state.

6.3.3.3 APS Monitoring

If the K1 byte and the 4 MSBs of the K2 byte, which are used sending APS requests and channel numbers, are received identically for 3 consecutive frames, their values are written to **RX_K1_[7:0]** and **RX_K2_[7:4]**. Accepted values are compared to the previous contents of these registers, and when a new 12-bit value is stored, the **RX_K1_D** delta bit is set.

The K1 byte is checked for instability. If, for 12 successive frames, no 3 consecutive frames are received with identical K1 bytes, the **K1_UNSTAB** bit is set. It is cleared when 3 consecutive identical K1 bytes are received. When **K1_UNSTAB** changes state, the **K1_UNSTAB_D** delta bit is set.

Bits 3 down to 0 of K2 may contain APS mode information. These bits are monitored for **K2_CONSEC[3:0]** consecutive identical values. **RX_K2_[3:0]** is written when this occurs, *unless the value of bits 2 and 1 of K2 is “11” (indicating Line/MS AIS or RDI, section 6.3.3.1).* The **RX_K2_D** delta bit is set when a new value is written to **RX_K2_[3:0]**.

The three delta bits associated with APS monitors, **RX_K1_D, RX_K2_D** and **K1_UNSTAB_D** all contribute to an APS interrupt signal, *APS_INTB.* In addition, these three deltas also contribute to the standard summary interrupt signal, *INTB*.

6.3.4 S1 Monitoring

The 4 LSBs of received S1 bytes are monitored for consistent values in either 8 consecutive frames in the SONET mode, **RX_SDH_S1** = 0, or 3 consecutive frames in the SDH (**RX_SDH_S1** = 1) mode. When these bits contain a consistent synchronization status message, the accepted value is written to **RX_S1_[3:0]**. Accepted values are compared to the previous contents of this register, and when a new value is stored, the **RX_S1_D** delta bit is set.

The S1 byte is also checked for message failure. If no message has met the above validation criterion (whether it is the same or different from the last accepted value) at any time since the last rising edge of LATCH_EVENT, then the S1 fail second event bit, **S1_FAIL_SECE**, is set.

6.3.5 M1 Monitoring

The M1 byte indicates the number of B2 errors that were detected by the remote terminal in its received signal. The CONGO contains a 20-bit M1 error counter that either counts every error indicated by M1 (if **BIT_BLKCNT** = 0) or every frame received with M1 not equal to 0 (if **BIT_BLKCNT** = 1). When **RX_SIG_MODE** = 1, the valid values of M1 for **BIT_BLKCNT** = 0 are 0 to 96; any other value is interpreted as 0 errors. When **RX_SIG_MODE =** 0 and **BIT_BLKCNT** = 0, the valid values of M1 are 0 to 24; any other value is interpreted as 0 errors. When the performance monitoring counters are latched, the value of this counter is latched to the **M1_ERRCNT[19:0]** register, and the M1 error counter is cleared. (See section 4.2).

If there has been at least one received M1 error indication since the last rising edge of LATCH_EVENT, then the M1 error second event bit, **M1_ERR_SECE**, is set.

6.4 Transport Overhead Drop

The TOH/SOH drop block outputs the received E1, F1, and E2 bytes and 2 serial DCC channels.

6.4.1 Orderwire (E1 and E2) and Section User Channel (F1)

The three serial outputs, *RX_E1_DATA*, *RX_E2_DATA*, and *RX_F1_DATA*, contain the values of the received E1, E2, and F1 bytes. A single 64 kHz clock reference output (*RX_E1E2F1_CLK*) is provided as well. The MSB of the E1, E2 and F1 bytes appears in the first 64 kHz clock cycle after a rising edge of *RX_FRAME_OUT.*

6.4.2 Data Communications Channels, DCC, (D1-D12)

There are two DCCs defined in the TOH/SOH. The Section/Regenerator Section DCC uses the D1, D2, and D3 bytes to create a 192 kb/s channel. The Line/Multiplex Section DCC uses bytes D4 through D12 to create a 576 kb/s channel.

The TOH/SOH drop block outputs DCC data on two serial channels, *RX_SDCC_DATA* and *RX_LDCC_DATA*. These channels are synchronous to the outputs *RX_SDCC_CLK* and *RX_LDCC_CLK*. The DCC data outputs change on the falling edges of *RX_SDCC_CLK* and *RX_LDCC_CLK*.

6.5 Pointer State Determination

Pointer state determination involves examining H1-H2 bytes to establish the state of the STS-12c/AU-4-4c or STS-3c/AU-4 received pointer.

6.5.1 State Transition Rules

In the following pointer state determination description, the numbers vary slightly dependent upon the mode of the device (STS-12c mode vs. STS-3c). To describe the operation of both cases, the following convention will be used to identify the requirement that applies to each mode: STS-12c [STS-3c]. The STS-3c/AU-4 requirement will follow the STS-12c/AU-4-4c requirement in braces.

The first pair of H1-H2 bytes contain the STS-12c/AU-4-4c [STS-3c/AU-4] pointer. They are monitored and are considered to be in 1 of the following 3 states:

- Normal (NORM = 00)
- Alarm Indication Signal (AIS = 01)
- Loss of Pointer (LOP = 10)

The remaining 11 [2] pairs of H1-H2 bytes are monitored for correct concatenation indication. They are considered to be in 1 of the following 3 states:

- Concatenated (CONC = 11)
- Alarm Indication Signal (AISC = 01)
- Loss of Pointer (LOPC = 10)

The individual states are stored in **PTR_STATE_[1:12]_[1:0]** [**PTR_STATE_[1:3]_[1:0]**], where **PTR_STATE_[i]_[1:0]** indicates the state of the **i**'th pair of H1-H2 bytes. The states of individual pairs of H1-H2 bytes are then combined to determine the state of the STS-12c/AU-4-4c [STS-3c/AU-4] pointer.

6.5.2 State of STS-12c/AU-4-4c [STS-3c/AU-4] Pointer

The CONGO supplies the register state bits **RX_PAIS** and **RX_LOP** that indicate the pointer state of the received STS-12c/AU-4-4c [STS-3c/AU-4] pointer. These may be in 1 of 3 states:

- Normal (**RX_PAIS** = 0 and **RX_LOP** = 0) - **PTR_STATE_[1]_[1:0]** is NORM (00) and all other **PTR_STATE_[i]_[1:0]** are CONC (11).
- Path/AU AIS (**RX_PAIS** = 1 and **RX_LOP** = 0) - All **PTR_STATE_[i]_[1:0]** are AIS or AISC (01).
- Loss of Pointer (**RX_PAIS** = 0 and **RX_LOP** = 1) - All others (The **PTR_STATE_[i]_[1:0]** values do not satisfy either Normal or Path/AU AIS criteria).

The **RX_PAIS** and **RX_LOP** signals contribute to the Path Remote Defect Indication (PRDI), see section 5.5.2.4. Changes in these state values are indicated by the **RX_PAIS_D** and **RX_LOP_D** delta bits.

6.6 Pointer Interpretation

The first H1-H2 byte pair is interpreted to locate the start of the SPE/VC. The rules for pointer interpretation are:

1. During normal operation, the pointer locates the start of the SPE/VC.
2. Any variation from the current accepted pointer is ignored unless a consistent new value is received 3 times consecutively, or it is preceded by one of the rules 3, 4, or 5. Any consistent new value received 3 times consecutively overrides rules 3 or 4.
3. For **RX_SDH_PI** = 0,

   if at least 3 out of 4 of the NDF bits match the disabled indication (0110) and at least 8 out of 10 of the pointer value bits match the current accepted pointer with its I-bits inverted, a positive justification is indicated. The byte following the H3 byte is considered a positive stuff byte, and the current accepted pointer value is incremented by 1 (mod 783).

   For **RX_SDH_PI** = 1,

   if at least 3 out of 4 of the NDF bits match the disabled indication (0110), 3 or more of the pointer value I-bits and 2 or fewer of the pointer value D-bits match the current accepted pointer with all its bits inverted, and either the received SS-bits are 10 or **RX_SS_EN** = 0, a positive justification is indicated. The byte following the H3 byte is considered a positive stuff byte, and the current accepted pointer value is incremented by 1 (mod 783).

4. For **RX_SDH_PI** = 0,

   if at least 3 out of 4 of the NDF bits match the disabled indication (0110) and at least 8 out of 10 of the pointer value bits match the current accepted pointer with its D-bits inverted, a negative justification is indicated. The H3 byte is considered a negative stuff byte (it is part of the SPE), and the current accepted pointer value is decremented by 1 (mod 783).

   For **RX_SDH_PI** = 1,

   if at least 3 out of 4 of the NDF bits match the disabled indication (0110), 3 or more of the pointer value D-bits and 2 or fewer of the pointer value I-bits match the current accepted pointer with all its bits inverted, and either the received SS-bits are 10 or **RX_SS_EN** = 0, a negative justification is indicated. The H3 byte is considered a negative stuff byte (it is part of the VC), and the current accepted pointer value is decremented by 1 (mod 783).

5. For **RX_SDH_PI** = 0,

   if at least 3 out of 4 of the NDF bits match the enabled indication (1001), and the pointer value is between 0 and 782, the received pointer replaces the current accepted pointer value.

   For **RX_SDH_PI** = 1,

   if at least 3 out of 4 of the NDF bits match the enabled indication (1001), the pointer value is between 0 and 782, and either the received SS-bits are 10 or **RX_SS_EN** = 0, the received pointer replaces the current accepted pointer value.

Using these pointer interpretation rules, the Pointer Interpreter block determines the location of SPE/VC payload and POH bytes.

6.7 Path Overhead Monitoring

The POH monitoring block consists of J1, B3, C2, and G1 monitoring. These POH bytes are monitored for errors or changes in states.

6.7.1 Path Trace (J1) Capture/Monitor

As with J1 insertion, the CONGO supports two methods of Path Trace (J1) capture. The first, typically used in SONET applications, captures 64 consecutive J1 bytes in the STS-12c/AU-4-4c or STS-3c/AU-4. The second, used in SDH applications, looks for a repeating 16 consecutive J1 byte pattern. When it has detected a consistent 16 byte pattern for three consecutive instances, the J1 pattern is stored in designated registers.

6.7.1.1 SONET J1 Capture

When **RX_SDH_J1** = 0 (SONET mode), the CONGO can be provisioned to capture a sample of the path trace message. When **J1_CAP** transitions from 0 to 1, the CONGO captures 64 consecutive J1 bytes from the specified tributary and writes them to **RX_J1_[63:0]_[7:0]**.

No path trace frame structure is defined for SONET, but GR-253 does recommend that the 64-byte sequence consist of a string of ASCII characters padded out to 62 bytes with NULL characters (00) and terminated with <CR> (0D) and <LF> (0A) bytes. If the **J1_CRLF** bit is set, the CONGO captures the first 64 byte string it receives in the J1 byte position that ends with {0D, 0A}. If the **J1_CRLF** bit is 0, the CONGO captures the next 64 J1 bytes without regard to their content. On completion of the capture, the CONGO sets the **J1_CAP_E** event bit.

6.7.1.2 16-Byte J1 Monitoring

If **RX_SDH_J1** =1 (normally used in the SDH mode), the J1 bytes are expected to contain a repeating 16-byte path trace frame that includes the PAPI. In this mode, the **J1_CAP, J1_CRLF,** and **J1_CAP_E** bits are not used. J1 monitoring consists of locking on to the start of the 16-byte path trace frame and examining the received path trace frames for values that match consistently for 3 consecutive path trace frames. When a consistent frame value is received, it is written to **RX_J1_[15:0]_[7:0]**. The first byte of the path trace frame (which contains the frame start marker) is written to **RX_J1_[15]_[7:0]**.

Framing. The MSBs of all path trace frame bytes are 0, except for the MSB of the frame start marker byte. The J1 monitor framer searches for 15 consecutive J1 bytes that have a 0 in their MSB, followed by a J1 byte with a 1 in its

MSB. When this pattern is found, the framer goes into frame, **J1_OOF** = 0. Once the J1 monitor framer is in-frame, it remains in frame until 3 consecutive path trace frames are received with at least 1 MSB bit error. (In the SONET mode, the J1 frame indication is held in the In-frame state, **J1_OOF** = 0.) The **J1_OOF_D** delta bit is set when **J1_OOF** changes state.

Pattern Acceptance and Comparison. Once in frame, the J1 monitor block looks for 3 consecutive 16-byte path trace frames. When 3 consecutive identical frames are received, the accepted frame is stored in **RX_J1_[15:0]_[7:0]**. Accepted frames are compared to the previous contents of these registers. When a new value is stored, the **RX_J1_D** delta bit is set.

6.7.2 BIP-8 (B3) Checking

The CONGO checks the received B3 bytes for correct BIP-8 values. Even parity BIP-8 is calculated over all bits in the SPE/VC (including the POH) each frame. These values are then compared to the B3 values received in the following frame. The comparison can result in from 0 to 8 mismatches (B3 bit errors). This value may be inserted into the Transmit Side G1 byte (see section 5.5.2.4).

The CONGO contains a 16-bit B3 error counter that either counts every B3 bit error (if **BIT_BLKCNT** = 0) or every frame with at least one B3 bit error (if **BIT_BLKCNT** = 1). When the performance monitoring counters are latched (LATCH_EVENT transitions high), the value of this counter is latched to the **B3ERRCNT_[15:0]** register, and the B3 error counter is cleared. (See section 4.2).

If there has been at least one B3 error since the last rising edge of LATCH_EVENT, then the B3 error second event bit, **B3ERR_SECE**, is set.

6.7.3 Signal Label (C2) Monitoring

The received C2 bytes are monitored so that reception of the correct type of payload can be verified. When a consistent C2 value is received for 5 consecutive frames, the accepted value is written to **RX_C2[7:0]**. The **RX_C2_D** delta bit is set when a new C2 value is accepted.

The expected value of the received C2 bytes is provisioned in **EXP_C2[7:0]**. If the current accepted value does not match the expected value, and the accepted value is NOT

- the all zeros Unequipped label,
- the 01(hex) Equipped - non-specific label,
- the FC(hex) payload defect label,
- the FF(hex) reserved label,

then the Payload Label Mismatch register bit, **RX_PLM**, is set high.

If the current accepted value is the all zeros Unequipped label, and the provisioned **EXP_C2[7:0]** != 00(hex), then the Unequipped register bit, **RX_UNEQ**, is set high.

The **RX_PLM** and **RX_UNEQ** signals contribute to the insertion of Path RDI on the Transmit Side (see section 5.5.2.4). When **RX_PLM** or **RX_UNEQ** changes state, the **RX_PLM_D** or the **RX_UNEQ_D** delta bit is set.

6.7.4 Path Status (G1) Monitoring

6.7.4.1 Path REI Monitoring

Bits 1 through 4 (the 4 MSBs) of the path status byte indicate the number of B3 errors that were detected by the remote terminal in its received SPE/VC signal. Only the binary values between 0 and 8 are legitimate. If a value greater than 8 is received, it is interpreted as 0 errors (as is specified in GR-253 and G.707). The CONGO contains a 16-bit G1 error counter that either counts every error indicated by G1 (if **BIT_BLKCNT** = 0) or every frame received with the first 4 bits of G1 not equal to 0 (if **BIT_BLKCNT** = 1). When the performance monitoring counters are latched (LATCH_EVENT transitions high), the value of this counter is latched to the **G1_ERRCNT[15:0]** register, and the G1 error counter is cleared. (See section 4.2).

If there has been at least one received G1 error indication since the last rising edge of LATCH_EVENT, then the G1 error second event bit, **G1ERR_SECE**, is set.

6.7.4.2 Path RDI Monitoring

The CONGO can be provisioned to monitor bit 5 of G1 (RDI-P indicator), if **RX_PRDI5** = 1; or bits 5, 6 and 7 of G1 (enhanced RDI-P indicator), if **RX_PRDI5** = 0. Monitoring consists of checking for **G1_CONSEC[3:0]** consecutive received values of the monitored bit(s) that are identical. When a consistent value is received, bits 5, 6 and 7 of G1 are written to **RX_G1[2:0]**. Accepted values are compared to the previous contents of this register. (All 3 bits are written, but if **RX_PRDI5** = 1, only G1 bit 5 and **RX_G1[2]** are involved in the comparisons.) When a new value is stored, the **RX_G1_D** delta bit is set.

6.7.5 Other POH Bytes

The remaining POH bytes are not monitored by the CONGO. These include the path user channel (F2), the position indicator (H4), the path growth/user channel (Z3/F3), the path growth/path APS channel (Z4/K3), and the tandem connection monitoring (Z5/N1) bytes.

6.8 Receive Payload Descrambling

After the payload is extracted from the SONET/SDH signal, the payload data is descrambled using a self-synchronizing $X^{43} + 1$ descrambler. In all modes, register **RX_DSCR_INH** controls the operation of the descrambler. When **RX_DSCR_INH = 0** (the default), the descrambler is enabled. When **RX_DSCR_INH = 1**, operation of the descrambler is inhibited.

The CONGO provides a self-synchronizing descrambler based on the following generator polynomial:

$$X^{43} + 1$$

6.8.1 ATM Descrambler Operation

In ATM operation (**TX_POS** = 0), the operation of the descrambler adheres to the following requirements:

- the descrambler operates on the bits of the information fields only
- during the five octet header the descrambler operation is suspended and the descrambler state retained

In order to meet these requirements, the ATM Processing Block provides cell delineation information to the descrambler.

6.8.2 POS and Direct Mapping Descrambler Operation

In POS and direct mapping mode (**RX_POS** = 1 or **RX_DIRECT_MAP** = 1), the descrambler operates on the entire payload, including interframe fill flags.

6.9 Receive HDLC Processing

At this point the SPE has been extracted from the SONET/SDH frame, and is passed on to either the HDLC or ATM processor for further processing. In POS mode (**RX_POS = 1**), the HDLC processing provides the extraction of PPP packets from the SPE.

6.9.1 Direct Mapping of Data into SPE

In the direct mapping mode (**RX_DIRECT_MAP** = 1), data passes through the HDLC processing block, before output over the Receive POS-PHY™ System Interface. Most HDLC functions are disabled in this mode of operation, with the exception of the Transparency processing (optional) and the POS-PHY™ System Interface, which operates slightly differently in this mode (i.e. *RX_SOC/P, RX_ERR, RX_MOD* and *RX_EOP* are disabled).

6.9.2 HDLC Framer

In POS mode (**RX_POS** = 1), HDLC frames are extracted from the SPE payload by identifying the Flag Sequence (0x7e) that begins/ends a frame.

The CONGO examines each octet of the payload. When an octet with bit pattern 0x7e is discovered, the CONGO recognizes this as the start/end of a packet. The octets that follow this Flag Sequence are then examined. If these are also 0x7e, they are Flag Sequences used to fill the Inter-Packet gap, and are discarded. The first octet NOT equal to 0x7e that follows the initial Flag Sequence is considered the first octet of the HDLC frame.

After the start of frame flag, the CONGO continues to examine each octet of the payload for the Flag Sequence. If it locates the bit pattern 0x7e and the immediately preceding octet is Control Escape (0x7d), the frame is aborted, see section 6.9.4. Otherwise, a normal end of the current frame is declared.

In the special case when termination of the FCS field is inhibited (see section 6.9.5), a minimum of two Flag Sequences must be detected between frames.

6.9.3 Removal of Transparency Byte Stuffing

6.9.3.1 POS Mode

In POS mode (**RX_POS** = 1) following the HDLC framer, the CONGO reverses the transparency byte stuffing process specified in section 5.2.4 to recover the original packet stream. The FIFO underflow byte sequence, which may be inserted by the transmit side during periods of FIFO underflow, will be detected and removed during the transparency processing if **RX_POS_FIFOUNDR_MODE** = 1. The default value is disabled, **RX_POS_FIFOUNDR_MODE** = 0. The special FIFO underflow byte code is programmed using register **RX_POS_FIFOUNDR_BYTE[7:0]**.

6.9.3.2 Direct Map Mode

In direct mapping mode (**RX_DIRECT_MODE** = 1), the transparency processing is controlled by **RX_POS_FIFOUNDR_MODE.** If **RX_POS_FIFOUNDR_MODE** = 1, transparency byte destuffing will be performed with the exception that 0x7e bytes that follow 0x7d bytes do not cause “aborts”, and they are treated as all other bytes (i.e. they are output as 0x5e). If **RX_POS_FIFOUNDR_MODE** = 0, transparency byte destuffing is disabled.

6.9.3.3 Underflow Byte Removal

In either direct map or POS mode, if **RX_POS_FIFOUNDR_MODE** = 1, bytes that match the FIFO underflow byte code (**RX_POS_FIFOUNDR_BYTE[7:0]**) are discarded if they are not immediately preceded by the Control Escape code (0x7d).

6.9.4 Errored Frames

In POS mode (**RX_POS** = 1), a special byte code (0x7d7e) is utilized in POS mode to indicate that a frame has been aborted. If this byte code is received, the frame that contains it is aborted. No further octets from the packet are sent to the FIFO, and if the packet is transmitted to the Link Layer device, it is marked as errored (see *RX_ERR*, section 7.0).

The CONGO contains an 8-bit error counter that counts every packet in which the abort sequence is detected. When the performance monitoring counters are latched (LATCH_EVENT transitions high), the value of this counter is latched to the **RX_POS_PABORT_ERRCNT[7:0]** register, and the packet abort error counter is cleared. (See section 4.2).

If there has been at least one packet abort error since the last rising edge of LATCH_EVENT*,* then the packet abort error second event bit, **RX_POS_PABORT_ERR_SECE**, is set.

As an alternative, a packet can also be aborted by inverting the FCS bytes. This will appear to the CONGO Receive HDLC/ATM Processor as simply an FCS error, and is handled as described in the following section.

The CONGO also, as an option, views a packet as being errored and marks it accordingly if it violates minimum or maximum packet sizes.The packet sizes refer to the size of the packets output from the CONGO only, and do not include the dropped flag sequence, address, control, transparency, FIFO underflow and FCS bytes. These minimum and maximum sizes are programmable via the management interface. Register **RX_POS_PMIN[3:0]** contains the minimum packet size. The default value of this register is **0**.

Register **RX_POS_PMAX[15:0]** contains the maximum packet size. The default value of this register is **0x05E0** (RFC 1661, pg 4).

The CONGO disables/enables minimum and maximum size packet checking when instructed to through the management interface. Registers **RX_POS_PMIN_ENB** and **RX_POS_PMAX_ENB** (both default to 0) control how violations of the minimum and maximum packet sizes are handled. When either is set to 1, any violation of the corresponding packet size restriction is marked as errored.

The CONGO contains two 8-bit error counters that count every violation of the maximum and minimum packet size limits. When the performance monitoring counters are latched (LATCH_EVENT transitions high), the value of these counters are latched to the **RX_POS_PMIN_ERRCNT[7:0]** and **RX_POS_PMAX_ERRCNT[7:0]** registers, and the packet size violation counters are cleared. (See section 4.2).

If there has been at least one packet size violation error since the last rising edge of LATCH_EVENT, then the appropriate packet size violation second event bit, **RX_POS_PMIN_ERR_SECE** or **RX_POS_PMAX_ERR_SECE**, is set.

6.9.5 Frame Check Sequence (FCS) Field

In POS mode (**RX_POS** = 1), an FCS is then calculated and checked against the FCS bytes at the end of each frame. This option is controlled by register **RX_POS_FCS_INH**. A value of **RX_POS_FCS_INH = 0** enables the FCS. A value of **RX_POS_FCS_INH = 1** disables it. Two types of FCS have been defined in RFC 1662, a 16 bit check sequence (CRC-16) and a 32 bit check sequence (CRC-32). The device supports both types. **RX_POS_FCS_MODE = 0** places the device in FCS-32 mode, and is the default. **RX_POS_FCS_MODE = 1** places the device in FCS-16 mode.

The CONGO provides CRC-16 functionality, using the following generator polynomial:

$$1 + X^5 + X^{12} + X^{16}$$

The CONGO provides CRC-32 functionality, using the following generator polynomial:

$$1 + X + X^2 + X^4 + X^5 + X^7 + X^8 + X^{10} + X^{11} + X^{12} + X^{16} + X^{22} + X^{23} + X^{26} + X^{32}$$

The FCS field is calculated over all bits frame, except the Flag Sequence and the FCS field itself.

If **RX_POS_FCS_BIT_ORDR** = 0 (the default), the received data is read into the shift register in big endian bit order (MSB first). If **RX_POS_FCS_BIT_ORDR** = 1, the received data is read into the shift register in little endian bit order (LSB first). In either case, the data is restored to big endian order for processing after the FCS calculation.

The resulting FCS is compared against the value in the received FCS field. If an error is detected, the management interface is notified, the appropriate counter incremented, and the last word of the packet is marked as errored in the FIFO. The CONGO contains a 20-bit FCS error counter that counts every FCS CRC violation. When the performance monitoring counters are latched (LATCH_EVENT transitions high), the value of this counter is latched to the **RX_POS_FCS_ERRCNT[19:0]** register, and the FCS error counter is cleared. (See section 4.2).

If there has been at least one FCS error since the last rising edge of LATCH_EVENT, then the FCS error second event bit, **RX_POS_FCS_ERR_SECE**, is set.

Following FCS checking, the FCS bytes are terminated (they are not stored in the FIFO). If the FCS checking is disabled via the management interface, the last 2 or 4 bytes are sent on to the FIFO.

Should an FCS error be detected, the packet is marked as errored (*RX_ERR*) when transmitted to the Link Layer device (see section 7.0).

6.9.6 HDLC Frame Termination

In POS mode (**RX_POS** = 1), after FCS calculation, the following HDLC bytes are monitored and optionally terminated:

6.9.6.1 Flag Sequence

All occurrences of the Flag Sequence, used for frame delineation and inter-frame fill purposes are deleted. The start and end of frame information is retained by the CONGO and transmitted to the Link Layer via the *RX_SOC/P* and *RX_EOP* signals.

6.9.6.2 Address and Control Bytes

The address and control bytes (the first two bytes of the HDLC frame following the Flag Sequence) are monitored by the CONGO. Monitoring consists of checking for the valid Address and Control fields (0xFF03). If no match is detected, this field is assumed to be compressed and was not sent. If invalid values are detected, these two bytes are not dropped, and are passed on the Link Layer via the POS-PHY™ interface. The management interface is notified of the detection of invalid Address and Control fields by setting **RX_POS_ADRCTL_INVALID** = 1. Changes in the state of **RX_POS_ADRCTL_INVALID** are indicated by setting its corresponding delta bit **RX_POS_ADRCTL_INVALID_D** to 1.

If valid Address and Control fields (0xFF03) are detected, the CONGO terminates these two bytes, and does not pass them on to the RX FIFO. The deletion of valid address and control bytes can be inhibited by setting **RX_POS_ADRCTL_DROP_INH** = 1. The default value of this register is 0 (automatic drop enabled).

6.9.6.3 FCS Bytes

As mentioned in the FCS section, the two or four FCS bytes are also terminated by the CONGO. If the FCS checking is disabled via the management interface (**RX_POS_FCS_INH** = 1), this termination is also disabled, and the last two or four bytes in the HDLC frame are sent on to the Link Layer.

6.10 Receive ATM Processing

In ATM mode (**RX_POS = 0**), the ATM processor provides the extraction of ATM cells from the SPE.

6.10.1 SPE Payload Deconstruction

6.10.1.1 ATM Cells into STS-3c/AU-4

The bit rate available for the ATM cells (user information cells, signalling cells, OAM cells, unassigned cells and cells used for cell rate decoupling) excluding SONET overhead packets is 149 760 kbit/s.

For STS-3c/STM-1 applications, the CONGO devices remove the path overhead from the VC-4, producing a C-4 container (VC-4 without the POH row). The ATM cell boundaries are aligned with the STM-1 octet boundaries. Since the C-4 capacity (2340 octets) is not an integer multiple of the cell length (53 octets), a cell may cross a C-4 boundary.

6.10.1.2 ATM Cells into STS-12c/AU-4-4c

The bit rate available for the ATM cells (user information cells, signalling cells, OAM cells, unassigned cells and cells used for cell rate decoupling) is 599 040 kbit/s.

For STS-12c/STM-4 applications, the CONGO device removes the path overhead from the VC-4-4c, producing a C-4-4c container (VC-4-4c without the POH and fixed stuff rows). The ATM cell boundaries are aligned with the STM-4 octet boundaries. Since the C-4-4c capacity (9360 octets) is not an integer multiple of the cell length (53 octets), a cell may cross a C-4-4c boundary.

6.10.2 ATM Cell Delineation

The cell delineation process is the procedure by which the ATM cell boundaries are identified. The HEC field is used by the CONGO device to achieve cell delineation, according to the algorithm defined in ITU-T I.432.1.

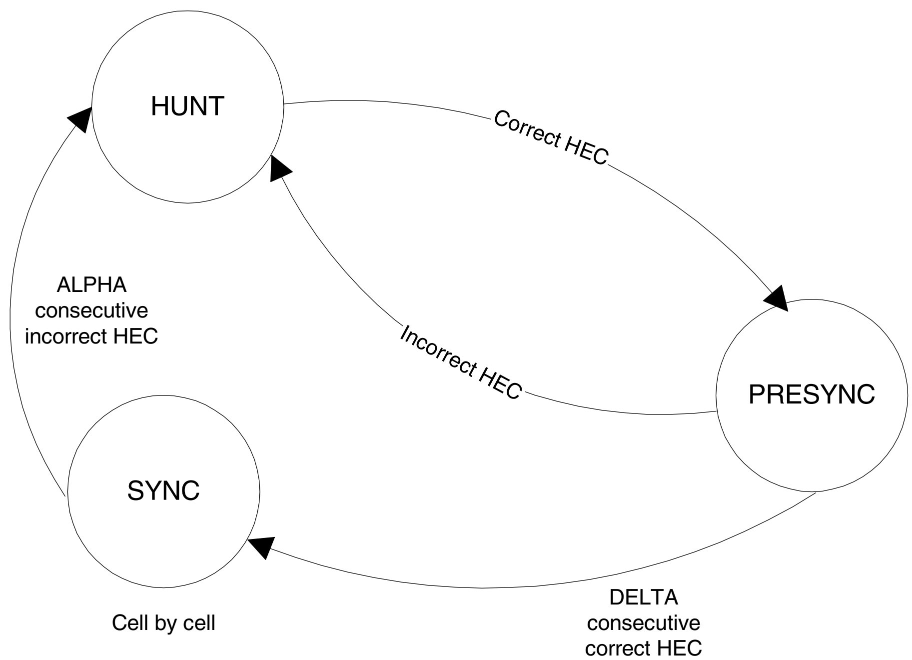
Cell Delineation Algorithm

Cell delineation is performed by using the correlation between the header bits to be protected (32 bits) and the relevant control bits (8 bits) introduced in the header by the HEC using a shortened cyclic code with generating polynomial $X^8 + X^2 + X + 1$. See section 5.3.4 for detailed requirement on CRC calculation.

The CONGO device takes the four ATM header bytes (or 4 consecutive octets, if it is in the HUNT state) and uses the generating polynomial to recalculate the HEC sequence. This recalculated sequence is then modulo 2 added to the received HEC byte. The result is referred to as the “syndrome”. The CONGO also supports the optional modulo 2 addition of the byte pattern 01010101 to the received HEC byte, prior to the comparison (modulo 2 addition) to the recalculated sequence. The option is configurable via the management interface.

Figure 9 shows the state diagram of the HEC cell delineation method.

Figure 9. Cell Delineation State Diagram



NOTE - The "correct HEC" means the header has no bit error (syndrome is zero) and has not been corrected

The details of the state diagram are described below:

1) In the HUNT state, the delineation process is performed by checking octet by octet for the correct HEC (i.e. syndrome equals zero) for the assumed header field. Once such an agreement is found, it is assumed that one header has been found, and the process enters the PRESYNC state.
2) In the PRESYNC state, the delineation process is performed by checking cell by cell for the correct HEC. The process repeats until the correct HEC has been confirmed DELTA times consecutively, at which point the process moves the SYNC state. If an incorrect HEC is found, the process returns to the HUNT state. The total number of consecutive correct HEC required to move from the HUNT state to the SYNC state is therefore DELTA + 1.
3) In the SYNC state the cell delineation is assumed to be lost if an incorrect HEC is obtained ALPHA times consecutively.
4) Cell with correct HECs (or cell headers with single bit errors which are corrected) that are processed while in the SYNC state are passed to the ATM layer.

The CONGO device uses an ALPHA of 7 and a DELTA of 6, as defined in [12].

Register **RX_ATM_HEC_ENH** enables/disables MOD2 addition of alternating 01010101 pattern to HEC calculation. A value of 1 (the default) enables, a value of 0 disables it.

6.10.2.1 Cell delineation signals

ITU Recommendation I.432.2 describes two cell delineation signals to be provided for performance monitoring purposes.The CONGO provides both of these performance indicators through the management interface.

Out of Cell Delineation (OCD). An OCD anomaly occurs when the cell delineation process changes from SYNC state to HUNT state while in a working state (see Figure 9). An OCD anomaly terminates when the PRESYNC to SYNC state transition occurs (see Figure 9).

An OCD anomaly is indicated by setting **RX_ATM_OCD** = 1. This register is cleared when the OCD terminates (see previous paragraph). The **RX_ATM_OCD_D** delta bit contributes to the summary interrupt, and the **RX_ATM_OCD_SECE** second event bits are set at the end of each second that the **RX_ATM_OCD** is in the active state at any time during the second.

Loss of Cell Delineation (LCD). An LCD defect occurs when an OCD anomaly (see above) has persisted for *y* ms., where *y* is in the range 0 to 4, and is provisioned via the registers **RX_ATM_LCD_TIME[5:0]**. An **RX_ATM_LCD_TIME** = 000 000 corresponds to 0 ms., **RX_ATM_LCD_TIME** = 100 000 corresponds to 4 ms. Increasing **RX_ATM_LCD_TIME** by one corresponds to a time increase of 125 µs. An LCD defect terminates when the cell delineation process enters and remains in the SYNC state for *y* continuous milliseconds.

An LCD defect is indicated by setting **RX_ATM_LCD** = 1. This register is cleared when the LCD terminates. The **RX_ATM_LCD_D** delta bit contributes to the summary interrupt, and the **RX_ATM_LCD_SECE** second event bits are set at the end of each second that the **RX_ATM_LCD** is in the active state at any time during the second.

6.10.3 Header Error Control Functions

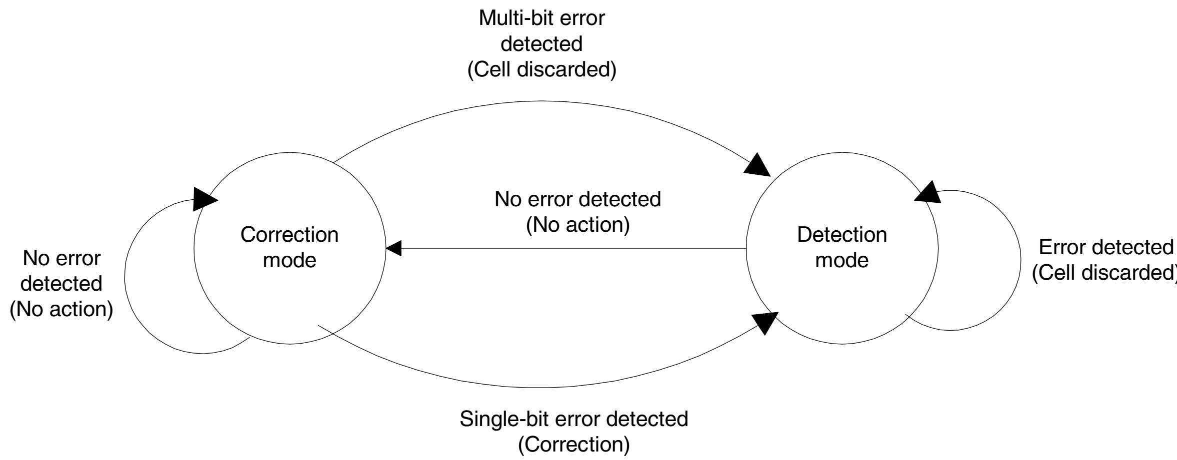
The following error processing procedure is performed by the CONGO whenever it is in SYNC state.

The HEC byte covers the entire cell header. The code used for this function is capable of either:

- single bit error correction; or
- multiple bit error detection

The detailed description of the HEC procedure is given in section 5.3.4 and section 6.10.2. As described in section 5.3.4, the transmitting side computes the HEC field value. The CONGO supports the two modes of operation shown in Figure 10. The default mode provides for single-bit error correction. Each cell header is examined and, if an error is detected, one of two actions takes place. The action taken depends on the state of the receiver. In “correction mode” only single bit errors can be corrected and the receiver switches to “detection mode”. In “detection mode”, all cells with detected header errors are discarded. When a header is examined and found not to be in error, the receiver switches to “correction mode”. The term “no action” in Figure 10 means no correction is performed and no cell is discarded.

Figure 10. HEC: Receiver mode of operation



The CONGO also provides an HEC detection only mode, where single error correction is disabled. The CONGO remains in the Detection mode shown in Figure 10, and discards all cells with errored headers. This mode is enabled by setting **RX_ATM_HEC_INH** = 1. The default value for this register is 0 (single error correction enabled).

The CONGO device furnishes performance monitoring registers to provide visibility into the Header Error Control Processing. The number of single bit errors that are corrected by the HEC processing is provided in **RX_ATM_HEC_CORR_[15:0]**. The number of cells that are discarded due errored Headers is provided in **RX_ATM_HEC_DROP_[15:0]**. The counter is large enough to count the expected number of error events received in a one second period during an error rate of 10^{-3}. The **RX_ATM_HEC_CORR_SECE** and **RX_ATM_HEC_DROP_SECE** second events are set whenever their corresponding counter registers are non-zero during a LATCH_EVENT transition from low to high.

6.10.4 ATM Idle Cell Removal

The CONGO deletes all idle cells, they are not sent to the ATM Layer device. The CONGO provides the user with the ability to specify the GFC, PTI, and CLP fields of the idle cell header. See section 5.3.3 for the structure of the ATM cell header and the location of the user programmable fields. The registers used to program these fields on the receive side are **RX_ATM_IDLE_GFC[3:0]**, **RX_ATM_IDLE_PTI[2:0]** and **RX_ATM_IDLE_CLP**. The default values for these registers are the same as the defaults for the corresponding registers on the transmit side.

The CONGO locates the user defined idle cell header (defined by **RX_ATM_IDLE_GFC[3:0]**, **RX_ATM_IDLE_PTI[2:0]**, and **RX_ATM_IDLE_CLP**) within the incoming data stream, and drops any cell with the idle cell header.

The CONGO also provides the capability for the user to monitor the contents of the data bytes of the idle cells. A byte indicator is provided (**RX_ATM_IDLE_BYTE[5:0]**) to indicate which byte of the ATM idle cell payload is monitored.This register is interpreted as directly identifying the byte position in the idle cell payload; values 1 through 48 indicate the first through 48th byte of the idle payload, other values are undefined. When **RX_ATM_IDLE_CAP** is written from 0 to 1, the CONGO captures the next ATM idle cell it detects in the indicated payload byte position.The value of the captured idle cell is written into **RX_ATM_IDLE_DATA[7:0]**, and **RX_ATM_IDLE_CAP_E** is written to 1 to indicate the capture is completed.

6.10.5 Receive Valid Cell Count

The CONGO contains an ATM cell counter that counts every valid non-idle ATM cell received from the SONET/SDH line. When the performance monitoring counters are latched (LATCH_EVENT transitions high), the value of this counter is latched to the **RX_ATM_CELL_CNT[20:0]** register, and the ATM non-idle cell counter is cleared. (See section 4.2).

6.11 Receive FIFO Interface

6.11.1 System Side Cell/Packet Loopback

The CONGO provides the capability for the user to loopback the cells/packets received via the System Interface. When **SYS_T_TO_R_LOOP** = 1, the cells/packets received from the ATM or Link Layer device are routed from the transmit FIFO directly to the receive FIFO, and output back to the ATM or Link Layer device that originated the cell data. When **SYS_T_TO_R_LOOP** is set to 0, the cells/packets/direct data received within the SONET/SDH line signals are transmitted to the receive FIFOs and then out the System Interface.

6.11.2 FIFO Processing

The CONGO writes cells/packets/direct data into the FIFO in preparation for output via the Receive System Interface to the ATM or Link Layer device. The FIFO holds 256 octets, enough for four full ATM cells. Along with the cell/packet/data, the following indicators, when applicable, must accompany each word in the FIFO: start of cell/packet, end of packet, if end of packet, how many octets in word (1 or 2), and whether or not the packet is errored. Once an error has been detected in a cell/packet, no further bytes from that cell/packet are loaded into the FIFO.

The state of the FIFO is monitored by the CONGO device. FIFO overflow events are reported to the management interface by setting **RX_FIFOOVER_E = 1**. The occurrence of a FIFO overflow also causes the appropriate performance monitoring counter to be incremented.

The CONGO contains an 8-bit FIFO overflow error counter that counts every cell/packet affected by a FIFO overflow event. When the performance monitoring counters are latched (LATCH_EVENT transitions high), the value of this counter is latched to the **RX_FIFOOVER_ERRCNT[7:0]** register, and the FIFO overflow error counter is cleared. (See section 4.2).

If there has been at least one FIFO overflow event since the last rising edge of LATCH_EVENT, then the FIFO overflow error event bit, **RX_FIFOOVER_ERR_SECE**, is set.

Once an overflow error has been detected, no further bytes from the cell/packet are sent to the FIFO. In the POS mode (**RX_POS** = 1), the last word of the packet is marked as errored (*RX_ERR*).

This FIFO immediately precedes the Receive System POS-PHY™ compatible interface. Its purpose is to perform the rate matching function between the SONET clock domain and the Link Layer clock domain.

6.11.3 Errored Cell/Packet Handling

In ATM mode (**RX_POS** = 0), as with the transmit direction, the CONGO will not forward ATM cells that have been corrupted by FIFO overflow events. These corrupted cells are deleted by the CONGO.

In POS mode (**RX_POS** = 1), the CONGO will mark as errored any packets that have been corrupted by FIFO overflow events, using *RX_ERR*. Other errored packet handling procedures in POS mode are described in section 6.9.4.

6.11.4 Receive Data Parity

As per the Utopia Level 2 and POS-PHY™ specifications, the CONGO provides a parity check bit that accompanies each one or two octet word (*RX_SYS_DAT[15:0]*) transmitted to the ATM or Link Layer device. This parity check bit is present on pin *RX_PRTY.* This bit provides an odd parity check as a default (**RX_PRTY_MODE** = 0). Even parity is provided if **RX_PRTY_MODE** = 1.

7.0 System Interface Requirements

Three slightly different system interfaces are provided, dependent upon the demands of the application. A fully compliant Utopia Level 2 interface is provided when the device is performing ATM cell extraction from the SONET SPE. A variant of the Utopia Level 2 interface, referred to as the POS-PHY™ Level 2 Interface, is provided when the device is performing HDLC frame generation and termination. This latter interface is based on the Utopia Level 2 and SCI-PHY interfaces, with modifications required to support variable length packets. A subset of the POS-PHY™ interface is provided for applications where raw data is mapped directly into the SONET/SDH SPE. In this last case, the POS-PHY™ interface remains primarily intact, with the exception that the *SOC/P*, *EOP*, *MOD* and *ERR* signals are disabled.

In all cases, the System Interface supports multi-PHY (several PHY layer devices connect to one Link Layer Device) applications.

7.1 Conventions

The interface where data flows from the ATM or Link Layer device to the CONGO device is labeled the Transmit System Interface. The interface where data flows from the CONGO to the ATM or Link Layer device is labeled the Receive System Interface.

All bytes are transmitted in big endian order (MSB first) unless otherwise specified.

7.2 Utopia Level 2 Basic Concepts

The ATM Forum has specified the Utopia Level 2 interface for transferring ATM cells between a single ATM Link Layer device and one or more PHY Layer devices. Separate interfaces are defined for the transmit and receive directions. Utopia defines that transmit and receive data transfers may occur at clock rates independent of the line bit rate. As a result, the PHY device must support cell rate decoupling using FIFOs. Control signals are provided to and from the ATM Layer device to support flow control in either direction.

7.3 Utopia Level 2 Modes of Operation

The Utopia Level 2 specification defines several different modes of operation:

Table 19. Utopia Level 2 Modes

Name	Functionality	Design Implications
Single PHY Device or Multi-PHY Device	SIngle: A single ATM layer device transmits data to/from a single PHY layer device. There may be multiple ports on the device.	PHY device does not tristate RX data bus, SOC or parity signals.
	Multi: A single ATM layer device transfers data to/from multiple PHY layer devices.	PHY device must be able to tristate RX data bus, SOC and parity signals.

Table 19. Utopia Level 2 Modes

Name	Functionality	Design Implications
Direct Status or Multiplexed Status (Polled Mode)	Direct: Each port provides both TX and RX status signals to the ATM Layer, which it uses to indicate the fill status of its FIFO. The fill level of the port is always available to the ATM Layer.	1. Each PHY port provides is own FIFO status signal to ATM Layer. 2. Port FIFO status signals driven continuously - not tristated.
	Multiplexed: Multiple PHY ports have their TX and RX status indications multiplexed onto one or more status signals. The ATM Layer device then requests that a specific port place its status indication on the multiplexed status signal; all other ports tristate.	1. PHY ports share FIFO status signals to ATM Layer - ATM device polls to arbitrate access to status signals. 2. FIFO status signals may be bussed - must be tristateable.
Full Addressing Mode or Group Addressing Mode	Full: In multiplexed polled operation, PHY port status signals driven only when PHY port's full 5 bit address appears on address bus.	PHY port reports FIFO status on shared status signals only when full address is detected on address bus.
	Group: In multiplexed polled operation, PHY port status signals driven when PHY port's Polling Group address (3 MSBs of full port address) appears on address bus.	PHY port reports FIFO status on shared status signals when Polling Group address is detected on address bus.
Octet Mode or Cell Mode	Octet: Data transfers across the Utopia interface occur in octet increments. Valid for single PHY operation only.	Data transfer based on single/two octet increments, rather than cell increments.
	Cell: Data transfers across the Utopia interface occur in cell increments. In multiplexed status mode, only cell level transfers are defined.	Data transfer based on cell increments.

In ATM mode, the CONGO supports Utopia Level 2 Multi-PHY, cell level transfer mode for multiplexed status polling (both group and full addressing), as well as direct status operation. Table 20 illustrates the Utopia modes supported by the CONGO.

Table 20. Utopia Level 2 Modes Supported by CONGO

Single-PHY		Multi-PHY			
Direct		Direct		Multiplexed	
Octet	Cell	Octet	Cell	Group Addr	Full Addr
NO	NO	NO	YES	YES	YES

7.4 POS-PHY^{TM} Level 2 Basic Concepts

The POS-PHY^{TM} interface has been specified for transferring data packets between a single Link Layer device and one or more PHY Layer devices. This interface is based on the Utopia Level 2 interface, with extensions provided to support variable length packets. As in Utopia Level 2, separate interfaces are defined for the transmit and receive directions. Transmit and receive data transfers may occur at clock rates independent of the line bit rate. As a result, the PHY device must support data rate decoupling using FIFOs. Control signals, very similar to those defined for Utopia Level 2, are provided to and from the Link Layer device to support flow control in either direction.

7.5 POS-PHY™ Level 2 Modes of Operation

POS-PHY™ supports the very similar modes of operation to those defined for Utopia Level 2. The single difference is described in the following table, which replaces the octet mode vs. cell mode entry in Table 19.

Table 21. POS-PHY™ Byte Mode/Packet Mode

Name	Functionality	Design Implications
Byte Mode or Packet Mode	Byte: Data transfers across the Utopia interface occur in single or two byte increments. Valid for direct status operation only.	Data transfer based on single/two byte increments, rather than packet increments. Address can change at any time during data transfer, without deassert/reassert of ENB signal.
	Packet: In multiplexed status mode, only packet level transfers are defined.	Address can only change when enable is deasserted.

In POS and Direct Map modes, the CONGO supports POS-PHY™ Level 2 Multi-PHY, packet level transfer mode for multiplexed status polling (both group and full addressing), as well as direct status operation. Table 22 illustrates the POS-PHY™ modes supported by the CONGO.

Table 22. POS-PHY™ Level 2 Modes Supported by CONGO

Single-PHY		Multi-PHY			
Direct		Direct		Multiplexed	
Byte	Packet	Byte	Packet	Group Addr	Full Addr
NO	NO	NO	YES	YES	YES

7.6 Common System Interface Specifications

7.7 Bus Widths

The CONGO device supports 8 and 16-bit data bus widths.

In 16-bit data bus POS-PHY™ or Direct Map modes, to accommodate packets with an odd number of bytes, signals are defined to allow a single byte word transfer, but only during the last word of a packet transfer.

Sixteen bit data bus operation (the default) is selected by setting **TX_** and **RX_SYSINT_8BIT** = 0. Eight bit data bus operation is selected by setting **TX_** and **RX_SYSINT_8BIT** = 1.

7.8 Clock Rates

7.8.1 POS-PHY™ and Direct Mode

The System Interface supports data rates from 15 MHz to 50 MHz. In the Direct Mapping mode, the Link Layer is responsible for insuring the data rate provides enough data to fill the SPE. If this cannot be guaranteed, the CONGO can be programmed to insert a particular byte sequence to fill the SPE during periods of FIFO underflow

(**TX_FIFOUNDR_BYTE[7:0]**).

7.8.2 ATM Operation

The System interface supports 25MHz and 50MHZ FIFO clock rates. For STS-12c/STM-4 operation, the System interface normally operates at 50MHz. For STS-3c/STM-1, the System interface normally operates at 25 MHz.

Table 23. Utopia Level 2 Clock Rates

Line Signal	Bit Rate (Mbit/s)	System Bus Width	Nominal System Bus Rate
STS-3c	155.52	8 bits	25 MHz
STM-1	155.52	8 bits	25 MHz
STS-12c	622.08	16 bits	50 MHz
STM-4	622.08	16 bits	50 MHz

7.9 Utopia Level 2 System Interface Requirements

7.9.1 Interface Data Structures

n ATM mode, 53 or 54-octet cells are transferred between the ATM Layer device and the CONGO. A user-defined field(s) is provided for backward compatibility. The byte arrangement is Big-Endian. Table 24 and Table 25 show the cell formats.

Table 24. Data Structure for 8-bit ATM mode

Bit 7 - Bit 0	8 bit Mode
Header 1	
Header 2	
Header 3	
Header 4	
UDF	UDF = User Defined (e.g. HEC)
Payload 1	
:	I
:	time
:	I
Payload 48	V

Table 25. Data Structure for 16-bit ATM mode

Bit 15	Bit 0	16 bit Mode
Header 1	Header 2	
Header 3	Header 4	
UDF1	UDF2	UDF = User Defined (e.g. HEC)
Payload 1	Payload 2	
:	:	l
:	:	time
:	:	l
Payload 47	Payload 48	V

Registers **TX_ATM_HEC_UDF** and **RX_ATM_HEC_UDF** define the location of the ATM HEC within the two User Defined bytes in the Utopia ATM data structure. If **TX_ATM_HEC_UDF** or **RX_ATM_HEC_UDF** = 0, the HEC is located in UDF1. If = 1, the HEC is located in UDF2.

7.9.2 ATM Utopia Level 2 Transmit Operation

The transmit system interface has data flowing in the same direction as the ATM enable. The ATM transmit block generates all output signals on the rising edge of the *TX_CLK*. Signals *TX_SYS_DAT*, *TX_SOC* and *TX_PRTY* are sampled on the rising edge of *TX_CLK*.

7.9.2.1 Direct Status Operation

Each CONGO device provides a signal that indicates the status of its FIFO to the Link Layer. In direct status operation, this signal indicates the FIFO status of only a single PHY device. This signal is called *TX_CLAV.* The CONGO is put into direct status mode by setting **TX_SYSINT_POLL** = 0. The CONGO supports only packet level transfers in direct status mode.

In the transmit direction, *TX_CLAV* is asserted when there is sufficient space available in the TX FIFO to accommodate an entire ATM cell. *TX_CLAV* is deasserted four clock cycles before (if **TX_CLAV_DSST** = 0, the default) or one clock cycle after (**TX_CLAV_DSST** = 1) the end of the cell transfer, if the TX FIFO cannot accommodate another cell.

7.9.2.2 Multiplexed Polling Operation

The CONGO supports multiplexed polling Utopia Level 2 operation. It is selected by setting **TX_SYSINT_POLL** = 1. The user can program the PHY address of the CONGO, via register **PHYADDR[4:0]**. The Utopia Level 2 specification defines a null address, equal to 0x1F (31). The CONGO tristates its *TX_CLAV* signal whenever the null address appears on *TX_ADR.* The default value of **PHYADDR** = 0x1F, the null address. This is to insure that an inactive port is not communicating invalid data or status information to the Link Layer. The user would activate only the desired ports by provisioning their corresponding **PHYADDR** to a non-null value.

7.9.3 ATM Utopia Level 2 Receive Operation

The receive system interface has data flowing in the opposite direction to the ATM Layer enable.The ATM receive block generates all output signals on the rising edge of the *RX_CLK*.

7.9.3.1 Direct Status Operation

Each CONGO device provides a signal that indicates the status of its FIFO to the Link Layer. In direct status operation, this signal indicates the FIFO status of only a single PHY device. This signal is called *RX_CLAV.* The CONGO is put into direct status mode by setting **RX_SYSINT_POLL** = 0.

In the receive direction, *RX_CLAV* is asserted when the receive FIFO has stored a full ATM cell, and is ready to transfer it to the Link Layer. *RX_CLAV* is deasserted four clock cycles before (if **RX_CLAV_DSST** = 0, the default) or one clock cycle after (**RX_CLAV_DSST** = 1) the end of the cell transfer, if the RX FIFO does not contain another full cell of data.

7.9.3.2 Multiplexed Polling Operation

In the Receive direction, multiplexed polling (selected by setting **RX_SYSINT_POLL** = 1 (the default)) operates in an identical fashion to the Transmit direction. In the Receive direction, the port status signal *RX_CLAV* is asserted to indicate that the Receive port has stored a full ATM cell and is ready to transfer it to the ATM Layer.

In the Receive direction, the CONGO uses the same assigned address (**PHYADDR[4:0])** as in the Transmit direction. This is specified by Utopia Level 2.

7.10 POS-PHY™ System Interface Requirements

7.10.1 POS Packet Format

Packets are written into the transmit FIFO and read from the receive FIFO using one defined data structure. For 8-bit bus operation, the octets are written in the same order they are to be transmitted or they were received on the SONET line. Within an octet, the MSB is the first bit to be transmitted. For 16-bit operation, all words are composed of two octets, except the last word of a packet transfer which can have one or two bytes. This does not preclude the transfer of 1-byte and 2-byte packets. In this case, both start of packet and end of packet signals are asserted simultaneously. This POS packet structure is illustrated in Table 26.

Table 26. 16-bit POS Packet Structure

	Bits 15-8	Bits 7-0
Word 1	Byte 1	Byte 2
Word 2	Byte 3	Byte 4
:	:	:
:	:	:
Word 7	Byte 13	Byte 14
Word 8	Byte 15	XX
A 15 byte packet		

7.10.2 POS-PHY™ Level 2 Transmit Operation

The transmit system interface has data flowing in the same direction as the Link Layer enable. The Link Layer transmit block generates all output signals on the rising edge of the *TX_CLK*. Signals *TX_SYS_DAT*, *TX_SOC/P* and *TX_PRTY* are sampled on the rising edge of *TX_CLK*.

7.10.2.1 Direct Status Operation

Each CONGO device provides a signal that indicates the status of its FIFO to the Link Layer. In direct status operation, this signal indicates the FIFO status of only a single PHY device. In direct mode, this signal is called *TX_CLAV*. The CONGO is put into direct status mode by setting **TX_SYSINT_POLL** = 0.

In the transmit direction, the CONGO device indicates that its' FIFO is not full by asserting this transmit packet available signal, *TX_CLAV*. *TX_CLAV* is asserted when there are less than a specified number of bytes (provisionable through **TX_FIFOEMPTY_TPA[4:0]**) available in the FIFO. *TX_CLAV* remains asserted until the transmit FIFO is almost full. Almost full implies that the CONGO device can accept at most a predefined number of writes after the current write (provisioned via **TX_FIFOFULL_TPA[4:0]**). The **TX_FIFOFULL_TPA[4:0]** and **TX_FIFOEMPTY_TPA[4:0]** registers have the following interpretation:

Table 27. TX/RX_FIFOFULL_T/RPA[4:0] and **TX/RX_FIFOEMPTY_T/RPA[4:0] Values**

TX/RX_FIFOFULL_T/RPA[4:0] or TX/RX_FIFOEMPTY_T/RPA[4:0]	Number of bytes in FIFO (< for FIFOEMPTY, >= for FIFOFULL
00000	8
00001	16
: :	: :
11111	256

The reset value of **TX_FIFOFULL_TPA[4:0]** is 11101. The reset value of **TX_FIFOEMPTY_TPA[4:0]** is 01111. To insure proper operation of this function, the **TX_FIFOFULL_TPA[4:0]** must exceed **TX_FIFOEMPTY_TPA[4:0]**.

7.10.2.2 Multiplexed Polling Operation

The CONGO supports multiplexed polling POS-PHY™ Level 2 operation. In this mode (**TX_SYSINT_POLL** = 1), the CONGO's FIFO status indication is designed to be multiplexed with the FIFO status of other PHY devices. The POS-PHY™ address bus, *TX_ADR[4:0]* is used to arbitrate access to this shared FIFO indication, now called *TX_PTPA.*

As in Utopia, the user can program the PHY address of the CONGO via register **PHYADDR[4:0]**. The POS-PHY™ Level 2 specification defines the same null address, equal to 0x1F (31). The CONGO tristates its *TX_PTPA* signal whenever the null address appears on *TX_ADR.* The default value of **PHYADDR** = 0x1F, the null address. This is to insure that an inactive port is not communicating invalid data or status information to the Link Layer. The user would activate only the desired ports by provisioning their corresponding **PHYADDR** to a non-null value.

7.10.3 POS-PHY™ Level 2 Receive Operation

The receive system interface has data flowing in the opposite direction to the Link Layer enable.The Link receive block generates all output signals on the rising edge of the *RX_CLK*.

7.10.3.1 Direct Status Operation

Each CONGO device provides a signal that indicates the status of its FIFO to the Link Layer. In direct status operation, this signal indicates the FIFO status of only a single PHY device. In direct mode, this signal is called *RX_CLAV.* The CONGO is put into direct status mode by setting **RX_SYSINT_POLL** = 0.

In the receive direction, the CONGO device indicates that its FIFO contains an end of packet that is ready to transfer by asserting this receive packet available signal, *RX_CLAV. RX_CLAV* is also asserted when there are greater than or equal to a specified number of bytes (provisionable through **RX_FIFOFULL_RPA[4:0]**) available in the FIFO. *RX_CLAV* remains asserted until the receive FIFO contains no end of packet, and is almost empty. Almost empty implies that the CONGO device can contains at most a predefined number of reads after the current read (provisioned via **RX_FIFOEMPTY_TPA[4:0]**).The interpretation of the **RX_FIFOFULL_TPA[4:0]** and **RX_FIFOEMPTY_TPA[4:0]** registers is given in Table 27.

The reset value of **RX_FIFOFULL_RPA[4:0]** is 01111. The reset value of **RX_FIFOEMPTY_RPA[4:0]** is 00011. To insure proper operation of this function, the **RX_FIFOFULL_RPA[4:0]** must exceed **RX_FIFOEMPTY_RPA[4:0]**.

7.10.3.2 Multiplexed Polling Operation

The CONGO supports multiplexed polling POS-PHY™ Level 2 operation. In this mode (**RX_SYSINT_POLL** = 1), the CONGO's FIFO status indication is designed to be multiplexed with the FIFO status of other PHY devices. The

POS-PHY^{TM} address bus, *RX_ADR[4:0]* is used to arbitrate access to this shared FIFO indication, now called *RX_PRPA.*

In the Receive direction, the CONGO uses the same assigned address (**PHYADDR[4:0])** as in the Transmit direction. This is specified by POS-PHY^{TM} Level 2. The Polling Group/CLAV Group sub-addressing scheme is also supported in the Receive direction.

7.10.4 Direct Mode Operation

Direct mode operates as a simpler subset of the POS-PHY^{TM} interface. The CONGO system interface operates as in the POS mode, except that the *TX_SOC/P, TX_EOP, TX_MOD, TX_ERR, RX_SOC/P, RX_EOP, RX_MOD* and *RX_ERR* are not used.

8.0 Management Interface

This section describes the Management Interface to the CONGO and defines the address of all registers that are available for reading or writing by an external microprocessor. Table 36 contains the Common Configuration and Summary Status Map, which holds control and monitoring parameters that are common to the entire device. Table 37 through Table 41 are the management interface register maps for the Transmit Side, and Table 42 through Table 47 are the Management Interface register maps for the Receive Side.

The MSB of the microprocessor bus address, *ADDR[8:0]*, designates whether the map is associated with the Transmit (*ADDR[8]* = 0) or Receive (*ADDR[8]* = 1) direction. *ADDR[7:0]* indicate the specific map and these values are identified with the following detailed descriptions of each map. The Common Configuration and Status Map is has *ADDR[8]* = 0.

8.1 Interrupt or Polled Operation

The Management Interface can be operated in either an interrupt driven or a polled mode. In both modes, the CONGO register bit **SUM_INT** in address 0x002 of the Common Configuration and Summary Status Map can be used to determine whether or not changes have occurred in the state of monitoring registers in the CONGO.

8.1.1 Interrupt Sources

8.1.1.1 Transmit Side

The Transmit Side register maps are almost entirely provisioning parameters that determine the composition of the SONET/SDH signal and provide the HDLC POS, ATM, SONET/SDH POH, and SONET/SDH TOH/SOH values.

In addition to these provisioning parameters, the Transmit Side register map includes System Interface and General Purpose I/O monitors. If any of these indications are active, the **SUM_INT** bit in register 0x002 will be high (logic 1). If **SUM_INT_MASK** = 0, the interrupt output for the microprocessor interface, *INTB,* becomes active (logic 0).

8.1.1.2 Receive Side

Table 36 also contains summary status bits for the Receive Side in register 0x005. These bits contribute to the **SUM_INT** bit in register 0x002. If any of the summary status bits is “1” and the corresponding mask bit is “0”, then the **SUM_INT** bit will be set to “1”.

The summary status bits in registers 0x005 of Table 36 are “1” if one or more of the corresponding group of bits in Table 42 through Table 47 is “1”. Individual TOH/SOH delta and second event bits can be masked (Table 42, addresses 0x104-0x106).

8.1.2 Interrupt Driven

In an interrupt driven mode, the **SUM_INT_MASK** bit in register 0x006 of the Common Configuration and Summary Status Map should be cleared (to logic 0). This allows the *INTB* output to become active (logic 0). This output is

INTB = !(!**SUM_INT_MASK** && **SUM_INT)**

In addition, the **RX_APS_INT_MASK** bits of the Receive side should be cleared (to logic 0). This allows the *APS_INTB* output to become active (logic 0). This output is

APS_INTB = !(!**RX_APS_INT_MASK** && **RX_APS_INT**)

If an interrupt occurs, the microprocessor can first read the summary status registers, 0x004-0x005 to determine the class(es) of interrupt source(s) that is active, and then read the specific registers in that class(es) to determine the exact cause of the interrupt.

8.1.3 Polled Mode

The **SUM_INT_MASK** and **RX_APS_INT_MASK** bits should be set (to logic 1), to suppress all hardware interrupts and operate in a polled mode. In this mode, the CONGO outputs *INTB* and *APS_INTB* are held in the inactive (logic 1) state.

Note that the **SUM_INT_MASK** and **RX_APS_INT_MASK** bits do not affect the state of the register bits **SUM_INT** and **RX_APS_INT**. These bits can be polled to determine if further register interrogation is needed.

9.0 Microprocessor Interface

This section describes the Microprocessor Interface to the CONGO. The Microprocessor Interface enables the System to access all registers within the CONGO. This interface complies with the microprocessor interface defined in the ATM Utopia Level 2 specification, [2].

The Microprocessor Interface is capable of operating in either an interrupt driven or a polled mode. In the interrupt mode, the CONGO is capable of supporting multiple Interrupt Sources. The CONGO is capable of masking out any of the interrupts in either Interrupt mode.

10.0 Register Map and Description

10.1 Register Map

Table 28. S1201 Register Map

Address	Register Name
0x000	Transmit Reset Control
0x001	Receive Reset Control
0x002	Summary Interrupt Status
0x003	Device Version
0x004	TX Summary Event
0x005	RX Summary Event
0x006	Summary Interrupt Mask
0x007	Reserved
0x008	TX Summary Event Mask
0x009	RX Summary Event Mask
0x00A	Receive Configuration
0x00B	Transmit Configuration
0x00C	Loopback Control
0x00D	GPIO Control
0x00E	GPIO Delta
0x00F	Reserved
0x010	GPIO Mask
0x011	Reserved
0x012	GPIO[3:0] Data
0x013	Reserved
0x014	GPIO[7:4] Data
0x015-0x01F	Reserved
0x020	Transmit Error Insert
0x021	Transmit AIS, RDI, REI Control
0x022	Transmit A1A2 Error Pattern - LSB
0x023	Transmit A1A2 Error Pattern - MSB
0x024 - 0x033	Transmit J0 - Bytes 1 - 16
0x034	Transmit K2 Byte
0x035	Transmit K1 Byte

Table 28. S1201 Register Map

Address	Register Name
0x036	Transmit S1 Byte
0x037	Transmit Frame Position Control
0x038-0x03F	Reserved
0x040	Transmit G1 Control
0x041	Reserved
0x042 - 0x081	Transmit J1 - Bytes 1 - 64
0x082	Reserved
0x083	Reserved
0x084	POH Error Generation
0x085	Transmit C2 Byte
0x086	Transmit J1 Mode Select
0x086-0x08F	Reserved
0x090	Transmit ATM HEC Error Mask
0x091	Reserved
0x092	Reserved
0x093	Transmit ATM HEC Control
0x094	Transmit Idle Cell Header
0x095	Transmit Idle Cell Data
0x096	Transmit ATM HEC Error Event
0x097	Reserved
0x098	Reserved
0x099	Transmit ATM HEC Inhibit
0x09A-0x09F	Reserved
0x0A0	Transmit Valid Cell Count - LSB
0x0A1	Transmit Valid Cell Count
0x0A2	Transmit Valid Cell Count - MSB
0x0A3-0x0AF	Reserved
0x0B0	Transmit System I/F Event Mask
0x0B1	Reserved
0x0B2	Transmit System I/F Control
0x0B3	Reserved
0x0B4	Transmit FIFO Low-watermark

Table 28. S1201 Register Map

Address	Register Name
0x0B5	Transmit FIFO High-watermark
0x0B6	Transmit System I/F Event
0x0B7	Reserved
0x0B8	PHY Address
0x0B9	Reserved
0x0BA	Transmit FIFO Error Count
0x0BB-0x0BF	Reserved
0x0C0	Transmit POS Error Event Mask
0x0C1	Reserved
0x0C2	Transmit POS Frame Abort Enable
0x0C3	Transmit POS Min Pkt Size
0x0C4	Transmit POS Max Pkt Size - LSB
0x0C5	Transmit POS Max Pkt Size - MSB
0x0C6	Transmit POS FIFO Fill Pattern
0x0C7	Reserved
0x0C8	Transmit POS Error Events
0x0C9	Reserved
0x0CA	Transmit POS Control
0x0CB	Reserved
0x0CC	Transmit POS FIFO Pkt Error Count
0x0CD	Transmit POS Link Pkt Error Count
0x0CE	Transmit POS Giant Pkt Count
0x0CF	Transmit POS Runt Pkt Count
0x0D0-0x0FF	Reserved
0x100	Receive LOH Monitor Delta
0x101	Receive SOH Monitor Delta
0x102	Receive TOH Monitor Second Event
0x103	Reserved
0x104	Receive LOH Monitor Masks
0x105	Receive SOH Monitor Masks
0x106	Receive TOH Monitor Sec. Event Mask
0x107	Reserved

Table 28. S1201 Register Map

Address	Register Name
0x108	Receive TOH Monitor Control 1
0x109	Receive TOH Monitor Control 2
0x10A	Receive Framer Position Control
0x10B	Reserved
0x10C	Receive LOH Status
0x10D	Receive SOH Status
0x10E	Reserved
0x10F	Reserved
0x110	Receive J0 - Byte 0
0x111	Receive J0 - Byte 1
0x112	Receive J0 - Byte 2
0x113	Receive J0 - Byte 3
0x114	Receive J0 - Byte 4
0x115	Receive J0 - Byte 5
0x116	Receive J0 - Byte 6
0x117	Receive J0 - Byte7
0x118	Receive J0 - Byte 8
0x119	Receive J0 - Byte 9
0x11A	Receive J0 - Byte 10
0x11B	Receive J0 - Byte 11
0x11C	Receive J0 - Byte 12
0x11D	Receive J0 - Byte 13
0x11E	Receive J0 - Byte 14
0x11F	Receive J0 - Byte 15
0x120	Reserved
0x121	Receive S1 Frame
0x122	Receive K2 Byte
0x123	Receive K1 Byte
0x124	Signal Fail Block Size
0x125	Reserved
0x126	Signal Fail Threshold Set
0x127	Signal Fail Group Set

Table 28. S1201 Register Map

Address	Register Name
0x128	Signal Fail Threshold Clear
0x129	Signal Fail Group Clear
0x12A	Signal Degrade Block Size - LSB
0x12B	Signal Degrade Block Size - MSB
0x12C	Signal Degrade Threshold Set
0x12D	Signal Degrade Group Set
0x12E	Signal Degrade Threshold Clear
0x12F	Signal Degrade Group Clear
0x130	Receive B1 Error Count - LSB
0x131	Receive B1 Error Count - MSB
0x132	Reserved
0x133	Reserved
0x134	Receive B2 Error Count - LSB
0x135	Receive B2 Error Count
0x136	Receive B2 Error Count - MSB
0x137	Reserved
0x138	Receive M1 Error Count - LSB
0x139	Receive M1 Error Count
0x13A	Receive M1 Error Count - MSB
0x13B-0x141	Reserved
0x142	Receive Pointer Interpreter Mask
0x143	Reserved
0x144	Receive Pointer Interpreter Control
0x145	Reserved
0x146	Receive Pointer Interpreter Delta
0x147	Reserved
0x148	Receive Pointer Tributary [1] Status
0x149	Reserved
0x14A	Receive Pointer Tributary [2] Status
0x14B	Reserved
0x14C	Receive Pointer Tributary [3] Status
0x14D	Receive Reserved

Table 28. S1201 Register Map

Address	Register Name
0x14E	Receive Pointer Tributary [4] Status
0x14F	Receive Reserved
0x150	Receive Pointer Tributary [5] Status
0x151	Reserved
0x152	Receive Pointer Tributary [6] Status
0x153	Reserved
0x154	Receive Pointer Tributary [7] Status
0x155	Reserved
0x156	Receive Pointer Tributary [8] Status
0x157	Reserved
0x158	Receive Pointer Tributary [9] Status
0x159	Reserved
0x15A	Receive Pointer Tributary [10] Status
0x15B	Reserved
0x15C	Receive Pointer Tributary [11] Status
0x15D	Reserved
0x15E	Receive Pointer Tributary [12] Status
0x15F	Reserved
0x160	Receive J1 Control
0x161	Receive RDI Monitor
0x162	Receive J1 Delta
0x163	Receive J1 Mask
0x164	Receive G1 Mask
0x165	Receive J1 OOF
0x166 - 0x1A5	Receive J1 - Bytes 1 - 64
0x1A6	Receive Path Delta
0x1A7	Reserved
0x1A8	Expected C2 Byte
0x1A9	Reserved
0x1AA	Receive POH Monitor
0x1AB	Receive C2 Byte
0x1AC	B3 Error Count - LSB

Table 28. S1201 Register Map

Address	Register Name
0x1AD	B3 Error Count - MSB
0x1AE	G1 Error Count - LSB
0x1AF	G1 Error Count - MSB
0x1B0-0x1BF	Reserved
0x1C0	Receive ATM Error Mask
0x1C1	Reserved
0x1C2	Reserved
0x1C3	Receive ATM LCD Time
0x1C4	Receive ATM Idle Header
0x1C5	Receive ATM Idle Cell Capture
0x1C6	Reserved
0x1C7	Reserved
0x1C8	Receive ATM Idle Data
0x1C9	Reserved
0x1CA	Receive ATM Error Events
0x1CB	Reserved
0x1CC	Receive ATM HEC Control
0x1CD	Receive ATM Status
0x1CE	Reserved
0x1CF	Reserved
0x1D0	Receive SBE Correct Count - LSB
0x1D1	Receive SBE Correct Count - MSB
0x1D2	Receive HEC Discards Count - LSB
0x1D3	Receive HEC Discards Count - MSB
0x1D4	Receive Cell Count - LSB
0x1D5	Receive Cell Count
0x1D6	Receive Cell Count - MSB
0x1D7-0x1DF	Reserved
0x1E0	Receive FIFO Overflow Mask
0x1E1	Reserved
0x1E2	Receive System I/F Control
0x1E3	Reserved

Table 28. S1201 Register Map

Address	Register Name
0x1E4	Receive FIFO Low-watermark
0x1E5	Receive FIFO High-watermark
0x1E6	Receive FIFO Overflow Event
0x1E7	Reserved
0x1E8	Receive FIFO Overflow Count
0x1E9-0x1EF	Reserved
0x1F0	Receive POS Error Mask
0x1F1	Receive POS Min Pkt Size
0x1F2	Receive POS Max Pkt Size - LSB
0x1F3	Receive POS Max Pkt Size - MSB
0x1F4	Receive POS FIFO Fill Pattern
0x1F5	Receive POS Error Event
0x1F6	Receive POS Control
0x1F7	Receive POS Addr/Ctrl Status
0x1F8	Receive POS Abort Packet Count
0x1F9	Reserved
0x1FA	Receive POS Giant Pkt Count
0x1FB	Receive POS Runt Pkt Count
0x1FC	Receive POS FCS Error Count - LSB
0x1FD	Receive POS FCS Error Count
0x1FE	Receive POS FCS Error Count - MSB
0x1FF	Device ID

10.2 Register Description

ADDR=0x000: Transmit Reset Control

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	Reserved	TEST	Reserved	TX_STATE_RESET	TX_PROV_RESET
R/W	X	X	X	X	R/W	X	R/W	R/W
Default	X	X	X	X	0	X	0	0

TEST *This bit is used for internal verification and should always be set to a 0.*

TX_STATE_RESET When set, all transmit state machines are reset to their default states. This bit must be cleared to resume normal operation.

TX_PROV_RESET When set, all transmit read/write registers (except the **TX_PROV_RESET** register itself) are reset. The transmit registers are held in their default state until **TX_PROV_RESET** is written to 0 or a hardware reset occurs.

ADDR=0x001: Receive Reset Control

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	Reserved	TEST	LATCH_CNT	RX_STATE_RESET	RX_PROV_RESET
R/W	x	x	x	x	R/W	R/W	R/W	R/W
Default	x	x	x	x	0	0	0	0

TEST *This bit is used for internal verification and should always be set to a 0.*

LATCH_CNT Used to transfer performance monitoring counter values to holding registers so that they can be read. When written from a 0 to a 1 (and **CNT_SEC_EN** = 0), all *_SECE register bits are set if their corresponding internal current second event monitoring bits are active.

RX_STATE_RESET When set, all receive state machines are reset to their default states. This bit must be cleared to resume normal operation.

RX_PROV_RESET When set, all receive read/write registers (except the **TX_PROV_RESET** register itself) are reset. The transmit registers are held in their default state until **TX_PROV_RESET** is written to 0 or a hardware reset occurs.

ADDR=0x002: Summary Interrupt Status

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RX_APS_INT	SUM_INT
R/W	x	x	x	x	x	x	R	R
Default	x	x	x	x	x	x	0	0

SUM_INT The microprocessor interface can be operated in either an interrupt driven or a polled mode. In both modes, the **SUM_INT** bit will be set if changes have occurred in the state of enabled monitoring registers in the S1201. The bit is cleared once the register which caused it to be set is read. See description of **SUM_INT_MASK** for further details.

RX_APS_INT Interrupt message for APS (K1 and K2).

ADDR=0x004: TX Summary Event

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LATCH_E	Reserved	Reserved	Reserved	TX_ATM_HEC_SUME	GPIO_SUMD	TX_POS_PKTERR_SECE_SUME	TX_FIFO_SUME
R/W	R	X	X	X	R	R	R	R
Default	0	X	X	X	0	0	0	0

TX_ATM_HEC_SUME Will be set if the **TX_ATM_HEC_ERR_E** bit is active and enabled (not masked).

GPIO_SUMD Will be set if any of the General Purpose I/O delta bits (**GPIO1_D**, **GPIO2_D**, ..., **GPIO8_D**) are active and enabled.

TX_POS_PKTERR_SECE_SUME Will be set if any of the transmit POS packet error event and second event monitors (**TX_POS_FIFOUNDR_E**, **TX_POS_FIFOUNDR_ERR_SECE**, **TX_POS_LLPKT_ERR_SECE**, **TX_POS_PMAX_ERR_SECE**, **TX_POS_PMIN_ERR_SECE**) are active and enabled.

TX_FIFO_SUME Will be set if any of the transmit FIFO event and second event monitors (**TX_PRTY_ERR_E**, **TX_FIFOERR_E**, **TX_FIFOERR_SECE**) are active and enabled.

LATCH_E is set to 1 whenever the CONGO updates the second event bits and the counters in all register maps, due to either the expiration of SEC_EVENT or the setting of **LATCH_CNT.**

ADDR=0x005: RX Summary Event

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	TOH_SUMD	TOH_SECE_SUM	PTR_INT_PAIS_SUMD	PATH_SUMD	ATM_SUMD	POS_SUME	RX_FIFO_SUME	RX_ATM_IDLE_CAP_E
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

TOH_SUMD Will be set if any of the TOH/SOH delta bits (**RX_LOS_D**, **RX_LOC_D**, **RX_OOF_D**, **RX_LOF_D**, **RX_J0_D**, **B2_ERR_SF_D**, **B2_ERR_SD_D**, **RX_LAIS_D**, **RX_LRDI_D**, **RX_K1_D**, **K1_UNSTAB_D**, **RX_K2_D**, **RX_S1_D**, **J0_OOF_D**) are active and enabled.

TOH_SECE_SUM Will be set if any of the TOH/SOH second event bits (**RX_OOF_SECE**, **RX_LOF_SECE**, **B1ERR_SECE**, **B2ERR_SECE**, **S1_FAIL_SECE**, **M1_ERR_SECE**) are active and enabled.

PTR_INT_PAIS_SUMD Will be set if any of the Pointer Interpreter delta bits (**RX_PAIS_D**, **RX_LOP_D**) are active and enabled.

PATH_SUMD Will be set if any of the Path Monitoring delta bits (**RX_PLM_D**, **RX_UNEQ_D**, **RX_G1_D**, **RX_J1_D**, **J1_CAP_E**, **J1_OOF_D**, **B3ERR_SECE**, **G1ERR_SECE**, **RX_C2_D**) are active and enabled.

ATM_SUMD Will be set if any of the ATM delta bits (**RX_ATM_OCD_D**, **RX_ATM_LCD_D**, **RX_ATM_OCD_SECE**, **RX_ATM_LCD_SECE**, **RX_ATM_HEC_CORR_SECE**, **RX_ATM_HEC_DROP_SECE**) are active and enabled.

POS_SUME Will be set if any of the POS delta and second bits (**RX_POS_ADRCTL_INVALID_D**, **RX_POS_PMIN_ERR_SECE**, **RX_POS_PMAX_ERR_SECE**, **RX_POS_PABORT_ERR_SECE**, **RX_POS_FCS_ERR_SECE**) are active and enabled.

RX_FIFO_SUME Will be set if any of the FIFO error indication event bits (**RX_FIFOOVER_E**, **RX_FIFOOVER_ERR_SECE**) are active and enabled.

RX_ATM_IDLE_CAP_E Will be set when the capture of an ATM idle cell is completed. After being set, **RX_ATM_IDLE_DATA[7:0]** will contain the results of the capture. The user will be notified that the capture has completed by the setting of **RX_ATM_IDLE_CAP_E**.

ADDR=0x006: Summary Interrupt Mask

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RX_APS_INT_MASK	SUM_INT_MASK
R/W	x	x	x	x	x	x	R/W	R/W
Default	x	x	x	x	x	x	1	1

SUM_INT_MASK Used to enable/disable the S1201 interrupt output pin INTB. The **SUM_INT_MASK** bit should be enabled to suppress all hardware interrupts and operate in polled mode. In this mode, the INTB output is held high (inactive). Note that the **SUM_INT_MASK** bit does not affect the state of the register bit **SUM_INT**. This bit can always be polled to determine if register interrogation is needed.

In an interrupt driven mode, the **SUM_INT_MASK** bit should be cleared. This allows INTB to become active should an interrupt occur. The microprocessor can first read the Summary Event/Delta status registers to determine the class of interrupt that is active, and then read the specific registers in that class to determine the exact cause of the interrupt.

RX_APS_INT_MASK Used to enable/disable the S1201 interrupt output pin APS_INTB. If **RX_APS_INT_MASK** is set to a logic “0” then the APS_INT is enabled. If a logic “1” then the **RX_APS_INT_MASK** suppresses all APS interrupts.

ADDR=0x008: TX Summary Event Mask

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LATCH_E_MASK	Reserved	Reserved	Reserved	TX_ATM_HEC_SUME_MASK	GPIO_SUMD_MASK	TX_POS_PKTERR_SECE_SUME_MASK	TX_FIFO_SUME_MASK
R/W	R/W	X	X	X	R/W	R/W	R/W	R/W
Default	1	X	X	X	1	1	1	1

The bits in the **Summary Event Mask** register are used to enable/disable status reporting of the corresponding bits in the Summary Event register. Setting the mask bit=0 enables status reporting of the corresponding bit in the event register, setting the mask bit=1 disables it.

ADDR=0x009: RX Summary Event Mask

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	TOH_SUMD_MASK	TOH_SECE_SUM_ MASK	PTR_INT_PAIS_ SUMD_MASK	PATH_SUMD_MASK	ATM_SUMD_MASK	POS_SUME_MASK	RX_FIFO_SUME_ MASK	RX_ATM_IDLE_ CAP_E_MASK
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	1	1	1	1

The bits in the **RX Summary Event Mask** register are used to enable/disable status reporting of the corresponding bits in the Summary Delta register. Setting the mask bit=0 enables status reporting of the corresponding bit in the event register, setting the mask bit=1 disables it.

ADDR=0x00A: Receive Configuration

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	RX_DSCR_INH	Reserved	RX_SIG_MODE	RX_DIRECT_MAP	RX_POS
R/W	x	x	x	R/W	x	R/W	R/W	R/W
Default	x	x	x	0	x	0	0	0

RX_DSCR_INH When clear, the receive payload descrambler (X^{43} + 1) is enabled. When set, operation of the receive descrambler is inhibited.

RX_SIG_MODE Determines the format and rate of the SONET/SDH input signal. If the bit is clear, the S1201's line-side input is configured for STS-3c/STM-1, byte-wide input at 19.44 MHz. If the bit is set, the S1201's line-side input is configured for STS-12c/STM-4, byte-wide input at 77.76 MHz

RX_DIRECT_MAP When set, the S1201's receive logic will not process ATM cells or PPP packets from the received data stream, and the SONET payload data is passed directly out to the System Interface with minimal processing. When clear, normal ATM cell or PPP packet processing operations will occur.

RX_POS When set, the S1201's receive logic is configured for Packet-Over-SONET mode, and will extract PPP packets from the SONET payload. When clear, the receive logic is configured for ATM mode, and will extract ATM cells within the SONET payload.

ADDR=0x00B: Transmit Configuration

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	TX_UNEQ	TX_SCR_INH	Reserved	TX_SIG_MODE	TX_DIRECT_MAP	TX_POS
R/W	X	X	R/W	R/W	X	R/W	R/W	R/W
Default	X	X	0	0	X	0	0	0

TX_UNEQ When set, the SONET/SDH output signal is generated with all-zeros in its SPE/VC bytes. This creates an unequipped SPE. When clear, the output signal assumes normal operation.

TX_SCR_INH When clear, the transmit payload scrambler ($X^{43} + 1$) is enabled. When set, operation of the transmit scrambler is inhibited.

TX_SIG_MODE Determines the format and rate of the SONET/SDH output signal. If the bit is clear, the S1201's line-side output is configured for STS-3c/STM-1, byte-wide output at 19.44 MHz. If the bit is set, the S1201's line-side output is configured for STS-12c/STM-4, byte-wide output at 77.76 MHz

TX_DIRECT_MAP When set, the S1201's transmit logic will map data received from the System Interface directly into the payload of the SONET/SDH Synchronous Payload Envelope (SPE) with no ATM cell processing or PPP packet processing. When clear, normal ATM cell or PPP packet processing operations will occur. In direct data mapping applications, the Link Layer device is responsible for insuring there is enough data in the S1201 to fill the SONET/SDH SPE.

TX_POS When set, the S1201's transmit logic is configured for Packet-Over-SONET mode, and will insert HDLC-encapsulated PPP packets received from the System Interface into the SONET payload. When clear, the transmit logic is configured for ATM mode, and will insert ATM cells into the SONET payload.

ADDR=0x00C: Loopback Control

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	CNT_SEC_EN	Reserved	Reserved	BIT_BLKCNT	SYS_T_TO_R_LOOP	SYS_R_TO_T_LOOP	SONET_T_TO_R_LOOP
R/W	X	R/W	X	X	R/W	R/W	R/W	R/W
Default	X	0	X	X	0	0	0	0

CNT_SEC_EN If the **CNT_SEC_EN** bit is set, the performance monitoring counters of the S1201 are latched every second. If clear, **LATCH_CNT** controls the latching of these counters.

BIT_BLKCNT The **BIT_BLKCNT** bit provisions performance monitoring counters to count bit errors or block errors. When **BIT_BLKCNT** is set, the B1, B2, B3, G1, and M1 monitors will count block errors. When clear, the monitors will count bit errors.

SYS_T_TO_R_LOOP When **SYS_T_TO_R_LOOP** is set, data transmitted to the S1201's transmit cell/packet FIFO is looped directly to the receive FIFO, and transmitted back to the receive side of the System Interface. When **SYS_T_TO_R_LOOP** is clear, normal operation occurs.

SYS_R_TO_T_LOOP When **SYS_R_TO_T_LOOP** is set, data received in the S1201's receive cell/packet FIFO is looped directly to the transmit FIFO, and transmitted to the output of the transmit FIFO. When **SYS_R_TO_T_LOOP** is clear, normal operation occurs.

SONET_T_TO_R_LOOP When **SONET_T_TO_R_LOOP** is set, data transmitted out of the S1201's SONET transmit framer generator is looped directly to the input of the receive framer. When **SONET_T_TO_R_LOOP** is clear, normal operation occurs.

ADDR=0x00D: GPIO Control

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	Reserved	GPIOCTL1	GPIOCTL2	GPIOCTL3	GPIOCTL4
R/W	x	x	x	x	R/W	R/W	R/W	R/W
Default	x	x	x	x	0	0	0	0

GPIOCTL1 When set, GPIO0 and GPIO1 are to be used as inputs. When clear GPIO0 and GPIO1 are outputs.

GPIOCTL2 When set, GPIO2 and GPIO3 are to be used as inputs. When clear GPIO2 and GPIO3 are outputs.

GPIOCTL3 When set, GPIO4 and GPIO5 are to be used as inputs. When clear GPIO4 and GPIO5 are outputs.

GPIOCTL4 When set, GPIO6 and GPIO7 are to be used as inputs. When clear GPIO6 and GPIO7 are outputs.

ADDR=0x00E: GPIO Delta

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	GPIO7_D	GPIO6_D	GPIO5_D	GPIO4_D	GPIO3_D	GPIO2_D	GPIO1_D	GPIO0_D
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

GPIOx_D Whenever there is a change in status of one of the GPIO bits, the corresponding GPIOx_D will be set. These bits are cleared by writing 1 to them.

ADDR=0x010: GPIO Mask

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	GPIO7_MASK	GPIO6_MASK	GPIO5_MASK	GPIO4_MASK	GPIO3_MASK	GPIO2_MASK	GPIO1_MASK	GPIO0_MASK
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	1	1	1	1

The bits in the **GPIO Mask** register are used to enable/disable status reporting of the corresponding bits in the GPIO Delta register. Setting the mask bit=0 enables status reporting of the corresponding bit in the event register, setting the mask bit=1 disables it.

ADDR=0x012: GPIO[3:0] Data

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	Reserved	GPIO3	GPIO2	GPIO1	GPIO0
R/W	x	x	x	x	R/W	R/W	R/W	R/W
Default	x	x	x	x	0	0	0	0

ADDR=0x014: GPIO[7:4] Data

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	Reserved	GPIO7	GPIO6	GPIO5	GPIO4
R/W	x	x	x	x	R/W	R/W	R/W	R/W
Default	x	x	x	x	0	0	0	0

The **GPIO[7:0]** bits contain data that the user has programmed as either input or output.

ADDR=0x020: Transmit Error Insert

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	A1A2_ERR	A1A2_ERR_NUM[2:0]			B1_INV	B2_INV	TX_M1_ERR	SCRINH
R/W	R/W	R/W			R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

A1A2_ERR For testing purposes, the A1 and A2 frame bytes pattern can be generated with errors. When **A1A2_ERR** is set, then *n* consecutive frames, where *n* is the binary equivalent of **A1A2_ERR_NUM[2:0]**, in each group of 8 frames, is generated with A1 and A2 exclusive-OR'ed with the contents of **A1A2_ERR_PAT[15:0]**. The most significant bit of A1 is XOR'ed with **A1A2_ERR_PAT[15]**, and the least significant bit of A2 is XORed with **A1A2_ERR_PAT[0]**. If **A1A2_ERR** is clear, no errors are inserted.

B1_INV When clear, the B1 Bit Interleaved Parity 8 (BIP-8) is transmitted as even parity (normal). When set, odd parity (incorrect) is generated.

B2_INV When clear, the B2 Bit Interleaved Parity 8 (BIP-8) is transmitted as even parity (normal). When set, odd parity (incorrect) is generated.

TX_M1_ERR When set, the user can force the transmission of Remote Error Indication (REI) errors. When clear, normal operation occurs.

SCRINH When set, the S1201's SONET scrambler is disabled. When clear, normal scrambler operation occurs.

ADDR=0x021: Transmit AIS, RDI, REI Control

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	TX_LAIS	TX_SDH_PG	Reserved	Reserved	Reserved	Reserved	LRDI_INH	LREI_INH
R/W	R/W	R/W	X	X	X	X	R/W	R/W
Default	0	0	X	X	X	X	0	0

TX_LAIS When set, the entire SONET/SDH signal is generated as all-ones, except for the first three rows of Section Overhead. When clear, normal operation occurs.

TX_SDH_PG When set, the S1201 pointer generator will operate in SDH mode (**SS bits** =10). When clear, the S1201 pointer generator will operate in SONET mode (**SS bits** = 00).

LRDI_INH When set, automatic generation of Line Remote Defect Indication (LRDI) is disabled. When clear, automatic generation of LRDI is enabled.

LREI_INH When set, automatic generation of Line Remote Error Indication (LREI) is disabled. When clear, automatic generation of LREI is enabled.

ADDR=0x022: Transmit A1A2 Error Pattern - LSB

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	A1A2_ERR_PAT[7:0]							
R/W	R/W							
Default	0	0	0	0	0	0	0	0

ADDR=0x023: Transmit A1A2 Error Pattern - MSB

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	A1A2_ERR_PAT[15:8]							
R/W	R/W							
Default	0	0	0	0	0	0	0	0

A1A2 Error Pattern See description in ADDR=0x020 Transmit Error Insert.

ADDR=0x024 - 0x033: Transmit J0 Bytes 1 - 16

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	TX_J0_[0]_[7:0] . . . TX_J0_[15]_[7:0]							
R/W	R/W							
Default	0	0	0	0	0	0	0	1

Transmit J0 (Section Trace) When enabled, the S1201 will continuously transmit in the J0 byte the 16-byte pattern contained in **TX_J0_[15:0]_[7:0]**. The bytes are transmitted in descending order starting with **TX_J0_[15]_[7:0]**.

ADDR=0x034: Transmit K2 Byte

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	TX_K2_[7:0]							
R/W	R/W							
Default	0	0	0	0	0	0	0	0

ADDR=0x035: Transmit K1 Byte

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	TX_K1_[7:0]							
R/W	R/W							
Default	0	0	0	0	0	0	0	0

TX_K1_[7:0] and **TX_ K2_[7:3]** are used for automatic protection switching (APS) signaling. The three LSBs of the K2 byte are used as an AIS or Remote Defect Indication (RDI) at the line/MS level in SDH. In SONET, the three LSBs of K2 are also used for APS signalling. The S1201 inserts **TX_K1_[7:0]** into the transmitted K1 byte stream, and **TX_K2_[7:3]** into the five MSBs transmitted K2 byte stream.

The three LSBs of K2 are controlled from three sources. In order of priority, these are:

- If **TX_LAIS** (ADDR=0x021) is set, they are transmitted as ‘111’.
- Else, if **LRDI_INH (ADDR=0x021)** is clear, and if any of (**RX_LOS** and not **RX_LOS_INH**), **RX_LOF**, **RX_LOC**, or **RX_LAIS** are set; they are transmitted as ‘110’ for a minimum of 20 frames.
- else **TX_K2_[2:0]** is transmitted.

ADDR=0x036: Transmit S1 Byte

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	TX_S1_[7:0]							
R/W	R/W							
Default	0	0	0	0	0	0	0	0

Transmit S1 (Synchronization Status Messages) The transmitted S1 byte out of the S1201 is set equal to **TX_S1_[7:0]**.

ADDR=0x037: Transmit Frame Position Control

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	TX_FOUT_BYTE_TYPE[1:0]		TX_FOUT_BYTE_NUMBER[3:0]			
R/W	X	X	R/W		R/W			
Default	X	X	0	0	0	0	0	0

TX_FOUT_BYTE_TYPE[1:0] and **TX_FOUT_BYTE_NUMBER[3:0]** Controls the relationship between the TX_FRAME_OUT clock pulse and the data bytes on the output bus TX_DATA[7:0]. Refer to the tables below for configuration of these registers. Note that only 2 LSB's of **TX_FIN_BYTE_NUMBER[3:0]** are used for STS-3/STM-1 mode.

Table 29. STS-3c/STM-1 configuration for TX_FOUT_BYTE_TYPE[1:0] and TX_FOUT_BYTE_NUMBER[3:0]

Data on *TX_DATA[7:0]* (when TX_FRAME_OUT =1)	TX_FOUT_BYTE_TYPE[1:0]	TX_FOUT_BYTE_NUMBER[3:0]
last byte of frame	00	00
first A1 byte	00	01
second A1 byte	00	10
third A1 byte	01	00
first A2 byte	01	01
second A2 byte	01	10
third A2 byte	10	00
J0 byte	10	01
first Z0 byte	10	10
last Z0 byte	11	00
first byte after last Z0 byte	11	01
second byte after last Z0 byte	11	10

Table 30. STS-12c/STM-4 configuration for TX_FOUT_BYTE_TYPE[1:0] and TX_FOUT_BYTE_NUMBER[3:0]

Data on *TX_DATA[7:0]* (when TX_FRAME_OUT =1)	TX_FOUT_BYTE_TYPE[1:0]	TX_FOUT_BYTE_NUMBER[3:0]
last byte of frame	00	0000
first A1 byte	00	0001
. . .	. . .	. . .
eleventh A1 byte	00	1011
last A1 byte	01	0000
first A2 byte	01	0001
. . .	. . .	. . .
last Z0 byte	11	0000
first byte after last Z0 byte	11	0001
. . .	. . .	. . .
eleventh byte after last Z0 byte	11	1011

ADDR=0x040: Transmit G1 Control

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	Reserved	Reserved	PREI_INH	PRDI_ENH	PRDI_AUTO
R/W	x	x	x	x	x	R/W	R/W	R/W
Default	x	x	x	x	x	0	0	0

PREI_INH If **PREI_INH** is set =1, G1 bits 1-4 are set to all zeros. If **PREI_INH** is set =0, G1 bits 1-4 are set to the binary value (0000 through 1000, indicating between 0 and 8) equal to the number of B3 errors most recently detected by the Receive Side POH monitoring block.

PRDI_ENH, PRDI_AUTO The values transmitted in bits 5, 6, and 7 of the G1 byte are taken either from the **TX_G1_[2:0]** registers (if **PRDI_AUTO** = 0), or the S1201 automatically generates an enhanced RDI signal (if **PRDI_AUTO** = 1 and **PRDI_ENH** = 1), or a one bit RDI signal (if **PRDI_AUTO** = 1 and **PRDI_ENH** = 0). The values transmitted in bits 5, 6, and 7 of G1 are shown in the table below.

Table 31. Path RDI Bit Values

<table>
<tr><th>PRDI_ AUTO</th><th>PRDI_ ENH</th><th>RX_PAIS || RX_LOP</th><th>RX_UNEQ</th><th>RX_PLM || RX_ATM_LCD</th><th>G1 Bits 5, 6, & 7</th></tr>
<tr><td>0</td><td>x</td><td>x</td><td>x</td><td>x</td><td>TX_G1_[2:0]</td></tr>
<tr><td rowspan="6">1</td><td rowspan="2">0</td><td>1</td><td>x</td><td>x</td><td>100</td></tr>
<tr><td>0</td><td>x</td><td>x</td><td>000</td></tr>
<tr><td rowspan="4">1</td><td>1</td><td>x</td><td>x</td><td>101</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>110</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>010</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>001</td></tr>
</table>

ADDR=0x042 - 0x081: Transmit J1 Bytes 1 - 64

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	TX_J1_[0]_[7:0] . . . TX_J1_[63]_[7:0]							
R/W	R/W							
Default	0	0	0	0	0	0	0	0

Transmit J1 (Path Trace) When enabled, the S1201 will continuously transmit in the J1 POH byte the 16 or 64 byte pattern contained in **TX_J1_[63:0]_[7:0]**. If **TX_SDH_J1** (ADDR=0x86) = 1, the J1 byte is transmitted repetitively as the 16-byte sequence in **TX_J1_[15]_[7:0]** descending down to **TX_J1_[0]_[7:0]**. If **TX_SDH_J1 = 0**, the J1 byte is transmitted repetitively as the 64-byte sequence in **TX_J1_[63]_[7:0]** descending down to **TX_J1_[0]_[7:0]**.

ADDR=0x084: POH Error Generation

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	FORCE_G1ERR	TX_G1_[2:0]			Reserved	Reserved	B3_INV	TX_PAIS
R/W	R/W	R/W			X	X	R/W	R/W
Default	0	0	0	0	X	X	0	0

FORCE_G1ERR If set=1, **G1** bits 1-4 will continuously be transmitted as 1000 (for testing purposes).

TX_G1_[2:0] The values transmitted in bits 5, 6, and 7 of G1 are taken from the **TX_G1_[2:0]** registers if **PRDI_AUTO** = 0. (See ADDR=0x040: Transmit G1 Control for further explanation.)

B3_INV If set=1, the **POH** Bit Interleaved Parity 8 (BIP-8) is transmitted with errors by generating odd parity. If B3_INV is set=0, even parity (normal) is generated.

TX_PAIS If **TX_PAIS** = 1, all rows of the TOH/SOH are generated normally, except for the pointer bytes in row 4. The H1, H2, and H3 bytes (as well as all SPE/VC bytes) are transmitted as all-ones bytes. If **TX_PAIS** = 0, normal payload fill will occur.

ADDR=0x085: Transmit C2 Byte

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	TX_C2_[7:0]							
R/W	R/W							
Default	0	0	0	0	0	0	0	0

Transmit C2 Byte The transmitted C2 byte out of the S1201 is set equal to **TX_C2_[7:0]**.

ADDR=0x086: Transmit J1 Control

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	TX_J1SEL
R/W	x	x	x	x	x	x	x	R/W
Default	x	x	x	x	x	x	x	1

If **TX_J1SEL** = 0, the J1 byte is transmitted repetitively as the 16-byte sequence in **TX_J1_[15]_[7:0]** down to **TX_J1_[0]_[7:0]**. Otherwise, the 64-byte sequence in **TX_J1_[63]_[7:0]** down to **TX_J1_[0]_[7:0]** is transmitted. (The 16-byte sequence is normally used in the SDH mode, and the 64-byte sequence in the SONET mode.)

ADDR=0x090: Transmit ATM HEC Error Mask

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	TX_ATM_HEC_ERR_E_MASK
R/W	x	x	x	x	x	x	x	R/W
Default	x	x	x	x	x	x	x	1

TX_ATM_HEC_ERR_EMASK Setting the **TX_ATM_HEC_ERR_EMASK**=0 enables status reporting of the **TX_ATM_HEC_ERR_E** event register, setting the mask bit=1 disables it.

ADDR=0x093: Transmit ATM HEC Control

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	Reserved	Reserved	TX_ATM_UTP_HEC_INH	TX_ATM_HEC_UDF	TX_ATM_HEC_ENH
R/W	X	X	X	X	X	R/W	R/W	R/W
Default	X	X	X	X	X	0	0	1

TX_ATM_UTP_HEC_INH If **TX_ATM_UTP_HEC_INH** is set=1, calculation of HEC errors in ATM cells received over the Utopia transmit system interface will be inhibited. If set=0, HEC error reporting will occur.

TX_ATM_HEC_UDF Register **TX_ATM_HEC_UDF** defines the location of the ATM HEC within the two user-defined bytes in the Utopia ATM data structure. If **TX_ATM_HEC_UDF** is set=0, the HEC is located in UDF1. If set=1, the HEC is located in UDF2.

TX_ATM_HEC_ENH Setting **TX_ATM_HEC_ENH** = 1 enables the modulo 2 addition of the alternating bit pattern (0x55) to the 8 bit HEC before being inserted into the last octet of the header. Setting **TX_ATM_HEC_ENH** = 0 disables this feature.

ADDR=0x094: Transmit Idle Cell Header

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	TX_ATM_IDLE_CLP	TX_ATM_IDLE_PTI[2:0]			TX_ATM_IDLE_GFC[3:0]			
R/W	R/W	R/W			R/W			
Default	1	0	0	0	0	0	0	0

ADDR=0x095: Transmit Idle Cell Data

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	TX_ATM_IDLE_DATA[7:0]							
R/W	R/W							
Default	0	1	1	0	1	0	1	0

TX_ATM_IDLE_CLP, TX_ATM_IDLE_PTI[2:0], and **TX_ATM_IDLE_GFC[3:0]** User programmable registers for the CLP, PTI, and GFC fields of the ATM header when the S1201 is sending idle cells.

TX_ATM_IDLE_DATA[7:0] User programmable register for the payload when sending idle cells. The value programmed will be repeated on all 48 bytes of the payload data.

ADDR=0x096: Transmit ATM HEC Error Event

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	TX_ATM_HEC_ ERR_E
R/W	x	x	x	x	x	x	x	R/W
Default	x	x	x	x	x	x	x	0

TX_ATM_HEC_ERR_E If **TX_ATM_HEC_ERR_E** is set=1, a HEC error is detected in any cell received from the ATM layer via the Utopia TX system interface. This event bit is cleared when written to a 1.

ADDR=0x099: Transmit ATM HEC Inhibit

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	TX_ATM_HEC_INH	Reserved	Reserved	Reserved	Reserved
R/W	x	x	x	R/W	x	x	x	x
Default	x	x	x	0	x	x	x	x

TX_ATM_HEC_INH When set =1, **TX_ATM_HEC_INH** will inhibit the S1201 from overwriting the HEC received from the ATM layer. In this mode the S1201 passes through the HEC byte received from the ATM layer. When set =0, the S1201 overwrites the HEC with a recalculated value.

ADDR=0x0A0: Transmit Valid Cell Count - LSB

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	TX_ATM_CELL_CNT_[7:0]							
R/W	R							
Default	0	0	0	0	0	0	0	0

ADDR=0x0A1: Transmit Valid Cell Count

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	TX_ATM_CELL_CNT_[15:8]							
R/W	R							
Default	0	0	0	0	0	0	0	0

ADDR=0x0A2: Transmit Valid Cell Count - MSB

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	Reserved	TX_ATM_CELL_CNT_[20:16]			
R/W	X	X	X	X	R			
Default	X	X	X	X	0	0	0	0

TX_ATM_CELL_CNT_[20:0] Registers 0xA0, 0xA1, and 0xA2 are the counters for valid transmitted ATM cells excluding idle cells. The counter is updated every second (if **CNT_SEC_EN** = 1) or when **LATCH_CNT** is written to a 1.

ADDR=0x0B0: Transmit System I/F Event Mask

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	Reserved	TX_FIFOERR_SECE_MASK	TX_FIFOERR_E_MASK	TX_PRTY_ERR_E_MASK	Reserved
R/W	x	x	x	x	R/W	R/W	R/W	x
Default	x	x	x	x	1	1	1	x

The bits in the **Transmit System I/F Event Mask** register are used to enable/disable status reporting of the corresponding bits in the Transmit System I/F Event register. Setting the mask bit=0 enables status reporting of the corresponding bit in the event register, setting the mask bit=1 disables it.

ADDR=0x0B2: Transmit System I/F Control

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	TX_SYSINT_8BIT	TX_SYSINT_POLL	TX_SYSINT_ GRPADD_INH	Reserved	TX_PRTY_MODE	Reserved	TX_CLAV_DSST
R/W	X	R/W	R/W	R/W	X	R/W	X	R/W
Default	X	0	1	1	X	0	x	0

TX_SYSINT_8BIT Controls whether the transmit system interface operates in 8 or 16 bit mode. Sixteen bit data bus operation is selected by setting **TX_SYSINT_8BIT** = 0. Eight bit data bus operation is selected by setting **TX_SYSINT_8BIT** = 1.

TX_SYSINT_POLL The S1201 supports multiplexed polled Utopia Level 2 operation by setting **TX_SYSINT_POLL** = 1. If the bit is set = 0, the S1201 operates in direct status mode.

TX_SYSINT_GRPADD If **TX_SYSINT_GRPADDR** is set = 0, whenever its' assigned polling group address is present on the address bus TX_ADR[4:2], the S1201 drives its TX_CLAV(PTPA) signal. TX_ADR[1:0] do not play a role in polling in this mode of operation. In this way, the Link Layer can poll multiple CLAV(PTPA) signals in a single clock cycle. If **TX_SYSINT_GRPADDR_INH** is set = 1, the S1201 drives TX_CLAV(PTPA) only when its' assigned full address is present on the address bus TX_ADR[4:0].

TX_PRTY_MODE When set=1, even parity will be used. When set=0, odd parity will be used.

TX_CLAV_DSST In the transmit direction, TX_CLAV is asserted when there is sufficient space available in the TX FIFO to accommodate an entire ATM cell. If **TX_CLAV_DSST** is set = 0, TX_CLAV is deasserted four clock cycles before the end of the cell transfer, if the TX FIFO cannot accommodate another cell. If **TX_CLAV_DSST** is set = 1, TX_CLAV is deasserted one clock cycle after the end of the cell transfer, if the TX FIFO cannot accommodate another cell.

ADDR=0x0B4: Transmit FIFO Low-watermark

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	TX_FIFOEMPTY_TPA[4:0]				
R/W	x	x	x	R/W				
Default	x	x	x	0	1	1	1	1

ADDR=0x0B5: Transmit FIFO High-watermark

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	TX_FIFOFULL_TPA[4:0]				
R/W	x	x	x	R/W				
Default	x	x	x	1	1	1	0	1

The S1201 allows the user to configure the low and high watermarks for the transmit FIFO by writing to the **TX_FIFOEMPTY_TPA** and **TX_FIFOFULL_TPA** registers. If the transmit FIFO falls below, or rises above these thresholds, the S1201 will notify the link layer via the TX_CLAV(PTPA) signal. To insure proper operation of this function, the **TX_FIFOFULL_TPA** setting must be greater than **TX_FIFOEMPTY_TPA**. The table below illustrates how the bits in these registers are interpreted.

TX_FIFOFULL/EMPTY_TPA setting	# of bytes for high/low watermark
00000	8
00001	16
: :	: :
11111	256

ADDR=0x0B6: Transmit System I/F Event

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	Reserved	TX_FIFOERR_SECE	TX_FIFOERR_E	TX_PRTY_ERR_E	Reserved
R/W	x	x	x	x	R/W	R/W	R/W	x
Default	x	x	x	x	0	0	0	x

TX_FIFOERR_SECE Indicates that a FIFO error event has occurred in the last second (if **CNT_SEC_EN**=1) or since **LATCH_CNT** was last written to a 1. The bit is cleared by writing a 1 to it.

TX_FIFOERR_E Indicates that a FIFO error has occurred. The bit is cleared by writing a 1 to it.

TX_PRTY_ERR_E Indicates that a parity error has been detected in the transmit data stream. The bit is cleared by writing a 1 to it .

ADDR=0x0B8: PHY Address

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	PHYADDR[4:0]				
R/W	x	x	x	R/W				
Default	x	x	x	1	1	1	1	1

PHYADDR[4:0] is the Utopia or POS-PHY^{TM} address associated with the device. Valid ranges for this register, when the CD012002 is active, are 0x00-1E, with 0x1F being reserved for the null-PHY address.

ADDR=0x0BA: Transmit FIFO Error Count

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	TX_FIFOERR_CNT[7:0]							
R/W	R							
Default	0	0	0	0	0	0	0	0

TX_FIFOERR_CNT[7:0] An 8-bit FIFO error counter that counts every cell/packet affected by a FIFO error event. The FIFO error counter is refreshed every second (if **CNT_SEC_EN**=1) or when **LATCH_CNT** is written to a 1.

ADDR=0x0C0: Transmit POS Error Event Mask

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	TX_POS_FIFOUNDR_ERR_SECE_MASK	TX_POS_PMIN_ER_SECE_MASK	TX_POS_PMAX_ER_SECE_MASK	TX_POS_LLPKT_ERR_SECE_MASK	TX_POS_FIFOUNDR_E_MASK
R/W	X	X	X	R/W	R/W	R/W	R/W	R/W
Default	X	X	X	1	1	1	1	1

The bits in the **Transmit POS Error Mask** register are used to enable/disable status reporting of the corresponding bits in the Transmit POS Error register. Setting the mask bit=0 enables status reporting of the corresponding bit in the event register, setting the mask bit=1 disables it.

ADDR=0x0C2: Transmit POS Frame Abort Enable

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	TX_POS_FCSABRT_ENB
R/W	x	x	x	x	x	x	x	R/W
Default	x	x	x	x	x	x	x	0

TX_POS_FCSABRT_ENB The S1201 cannot delete packets if the error condition is received or detected after transmission of the packet has begun. These packets are therefore aborted. The S1201 supports two options for aborting an errored packet. The default option is to abort a packet by inserting the abort sequence, 0x7D7E. Reception of this code at the far end will cause the receiver to discard this packet.

As an alternative, the S1201 can also abort an errored packet by simply inverting the FCS bytes. Setting **TX_POS_FCSABRT_ENB** = 1 enables the FCS inversion method, setting **TX_POS_FCSABRT_ENB** = 0 disables it.

ADDR=0x0C3: POS Min Packet Size

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	TX_POS_FCS_BIT_ORDR	TX_POS_PMIN[3:0]			
R/W	X	X	X	R/W	R/W			
Default	X	X	X	0	0	0	0	0

TX_POS_PMIN[3:0] A programmable value for the minimum transmitted PPP packet size. The packet size refer to the size of the PPP packet only, and do not include the bytes inserted by the S1201 (flag sequence, address, control, FIFO underflow, transparency or the FCS bytes).

TX_POS_FCS_BIT_ORDR If **TX_POS_FCS_BIT_ORDR** = 0 (the default), the packet data is written into the FCS shift register in big endian order (MSB fist). If **TX_POS_BIT_ORDR** = 1, the packet data is read into the shift register in little endian bit order.

ADDR=0x0C4: POS Max Packet Size - LSB

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	TX_POS_PMAX[7:0]							
R/W	R/W							
Default	1	1	1	0	0	0	0	0

ADDR=0x0C5: POS Max Packet Size - MSB

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	TX_POS_PMAX[15:8]							
R/W	R/W							
Default	0	0	0	0	0	1	0	1

TX_POS_PMAX[15:0] A programmable value for the maximum transmitted packet size. The default value is 0x05E0.

ADDR=0x0C6: POS FIFO Fill Pattern

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	TX_POS_FIFOUNDR_BYTE[7:0]							
R/W	R/W							
Default	1	0	1	0	0	0	0	0

TX_POS_FIFOUNDR_BYTE[7:0] Contains the byte pattern that may be inserted to the transmitted data stream during periods of Tx FIFO underflow. The pattern is inserted if **TX_POS_FIFOUNDR_MODE** (ADDR=0x0CA) is set =1.

ADDR=0x0C8: Transmit POS Error Events

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	TX_POS_FIFOUNDR_ERR_SECE	TX_POS_PMIN_ERR_SECE	TX_POS_PMAX_ERR_SECE	TX_POS_LLPKT_ERR_SECE	TX_POS_FIFOUNDR_E
R/W	X	X	X	R/W	R/W	R/W	R/W	R/W
Default	X	X	X	0	0	0	0	0

TX_POS_FIFOUNDR_ERR_SECE Indicates that the transmit FIFO has had at least one under-run condition in the last monitoring interval.

TX_POS_PMIN_ERR_SECE Indicates that there has been at least one minimum packet size violation in the last monitoring interval.

TX_POS_PMAX_ERR_SECE Indicates that there has been at least one maximum packet size violation in the last monitoring interval.

TX_POS_LLPKT_ERR_SECE Indicates that there has been at least one link-layer packet violation in the last monitoring interval.

TX_POS_FIFOUNDR_E Indicates a transmit FIFO under-run condition has occurred.

A monitoring interval is either 1 sec (if **CNT_SEC_EN** = 1) or between consecutive settings of **LATCH_CNT** =1.

These bits are cleared by writing a 1 to them.

ADDR=0x0CA: Transmit POS Control

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	TX_POS_FIFOUNDR_MODE	TX_POS_PMIN_ENB	TX_POS_PMAX_ENB	TX_POS_FCS_MODE	TX_POS_FCS_INH	TX_POS_EOP_FLAG	TX_POS_ADRCTL_INS
R/W	X	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	X	0	0	0	0	0	0	0

TX_POS_FCS_MODE When set=1, the S1201 is placed in FCS-16 mode, and provides FCS-16 functionality using the following generator polynomial: $1 + X^5 + X^{12} + X^{16}$. When set=0, the S1201 is placed in FCS-32 mode, and provides FCS-32 functionality using the following generator polynomial: $1 + X + X^2 + X^4 + X^5 + X^7 + X^8 + X^{10} + X^{11} + X^{12} + X^{16} + X^{22} + X^{23} + X^{26} + X^{32}$

TX_POS_FCS_INH When set = 0, the S1201 will calculate the FCS and insert it at the end of each frame. When set = 1, FCS insertion is inhibited.

TX_POS_FIFOUNDR_MODE When set =1, the S1201 will insert the FIFO byte-code contained in **TX_POS_FIFOUNDR_BYTE[7:0]** into the transmitted data stream during periods of FIFO underflow, and transparency byte stuffing for the FIFO byte code is enabled. If set = 0, the FIFO byte code is not inserted, and the byte stuffing of the FIFO byte code is not performed.

TX_POS_PMIN_ENB When set =1, packets below the minimum packet size threshold will be aborted. When set = 0, minimum size violations are ignored.

TX_POS_PMAX_ENB When set =1, packets above the minimum packet size threshold will be aborted. When set = 0, maximum size violations are ignored.

TX_POS_EOP_FLAG When set = 1, the S1201 inserts separate flags to indicate the end of one frame and the start of the following frame. If set = 0, only a single flag may be inserted.

TX_POS_ADRCTL When set = 1, the S1201 inserts Address and Control fields. When set = 0 does not insert them (default).

ADDR=0x0CC: POS FIFO Packet Error Count

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	TX_POS_FIFOUNDR_ERRCNT[7:0]							
R/W	R							
Default	0	0	0	0	0	0	0	0

TX_POS_FIFOUNDR_ERRCNT[7:0] Counts the number of packets corrupted due to FIFO underflow events.

ADDR=0x0CD: POS Link Layer Packet Error Count

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	TX_POS_LLPKT_ERRCNT[7:0]							
R/W	R							
Default	0	0	0	0	0	0	0	0

TX_POS_LLPKT_ERRCNT[7:0] counts the number of packets received from the Link Layer device that are marked as errored.

ADDR=0x0CE: POS Giant Packet Error Count

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	TX_POS_PMAX_ERRCNT[7:0]							
R/W	R							
Default	0	0	0	0	0	0	0	0

ADDR=0x0CF: POS Runt Packet Error Count

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	TX_POS_PMIN_ERRCNT[7:0]							
R/W	R							
Default	0	0	0	0	0	0	0	0

TX_POS_PMAX_ERRCNT[7:0] and **TX_POS_PMIN_ERRCNT[7:0]** count the number of packets received from the Link Layer device that violate minimum and maximum packet lengths.

ADDR=0x100: Receive LOH Monitor Delta

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B2_ERR_SF_D	B2_ERR_SD_D	RX_LAIS_D	RX_LRDI_D	RX_K1_D	K1_UNSTAB_D	RX_K2_D	RX_S1_D
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

ADDR=0x101: Receive SOH Monitor Delta

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	RX_LOS_D	RX_LOC_D	RX_OOF_D	RX_LOF_D	J0_OOF_D	RX_J0_D
R/W	X	X	R/W	R/W	R/W	R/W	R/W	R/W
Default	X	X	0	0	0	0	0	0

Receive Framer Delta Bits Will be set = 1 if there is a change in state of the corresponding event bit. These bits are cleared by writing a 1 to them.

ADDR=0x102: Receive TOH Monitor Second Event

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	RX_OOF_SECE	RX_LOF_SECE_	B1ERR_SECE	B2ERR_SECE	S1FAIL_SECE	M1ERR_SECE
R/W	X	X	R/W	R/W	R/W	R/W	R/W	R/W
Default	X	X	0	0	0	0	0	0

Receive TOH Monitor Event Bits Will be set at the end of each second that the corresponding error bits are in the active state at any time during the second. These bits are cleared by writing a 1 to them.

ADDR=0x104: Receive LOH Monitor Masks

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B2_ERR_SF_D_MASK	B2_ERR_SD_D_MASK	RX_LAIS_D_MASK	RX_LRDI_D_MASK	RX_K1_D_MASK	K1_UNSTAB_D_MASK	RX_K2_D_MASK	RX_S1_D_MASK
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	1	1	1	1

ADDR=0x105: Receive SOH Monitor Masks

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	RX_LOS_D_MASK	RX_LOC_D_MASK	RX_OOF_D_MASK	RX_LOF_D_MASK	J0_OOF_D_MASK	RX_J0_D_MASK
R/W	X	X	R/W	R/W	R/W	R/W	R/W	R/W
Default	X	X	1	1	1	1	1	1

ADDR=0x106: Receive TOH Monitor Second Event Masks

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	RX_OOF_SECE_MASK	RX_LOF_SECE_MASK	B1ERR_SECE_MASK	B2ERR_SECE_MASK	S1FAIL_SECE_MASK	M1_RR_SECE_MASK
R/W	X	X	R/W	R/W	R/W	R/W	R/W	R/W
Default	X	X	1	1	1	1	1	1

The bits in the above registers are used to enable/disable status reporting of the corresponding event bits. Setting the mask bit=0 enables status reporting of the corresponding bit in the event register, setting the mask bit=1 disables it.

ADDR=0x108: Receive TOH Monitor Control 1

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	K2_CONSEC[3:0]				Reserved	Reserved	RX_LOF_ALG	DSCRINH
R/W	R/W				X	X	R/W	R/W
Default	0	1	0	1	X	X	0	0

K2_CONSEC[3:0] The number of consecutive occurrences of LAIS and LRDI in order for the presence/absence of LAIS or LRDI to be detected and the monitors updated accordingly.

RX_LOF_ALG Determines which of 2 algorithms is used to clear the **RX_LOF** status bit. If **RX_LOF_ALG** is set = 1, **RX_LOF** will be cleared after **RX_OOF** is inactive for 24 consecutive frames. If **RX_LOF_ALG** is set = 0, **RX_LOF** will be cleared after **RX_OOF** is inactive for 8 consecutive frames.

DSCRINH For testing purposes, the descrambler can be disabled by setting **DSCRINH** = 1. Scrambler is enabled if set = 0.

ADDR=0x109: Receive TOH Monitor Control 2

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	RX_LOS_LEVEL	RX_LOS_INH	RX_FRMR_INH	Reserved	Reserved	RX_SDH_S1	RX_SDH_J0
R/W	X	R/W	R/W	R/W	X	X	R/W	R/W
Default	X	0	0	0	X	X	0	0

RX_LOS_LEVEL Programmable input level for the RX_LOS input (pin 196) to the S1201. If set = 1, the input is active low. If set = 0, the input is active high.

RX_LOS_INH Controls the LOS contribution to LRDI. If set = 1, the RX_LOS contribution to LRDI will be inhibited. If set = 0, the RX_LOS contribution to LRDI will be enabled.

RX_FRMR_INH If set = 0, the S1201 receive framer is enabled and the parallel input signal is not assumed to be byte aligned. If **RX_FRMR_INH** = 1, the framer circuitry in the S1201 is bypassed, and requires a frame start indication, RX_FRAME_IN, as well as data and clock.

RX_SDH_S1 The receive framer will monitor the S1 byte in SDH mode when **RX_SDH_S1** is set =1, and SONET mode when set =0. The S1201 will monitor S1 for consistent values for 3 consecutive frames (**RX_SDH_S1**=0) or 8 consecutive frames (**RX_SDH_S1** =1).

RX_SDH_J0 The receive framer will monitor the J0 bytes in SDH mode when **RX_SDH_S1** is set =1, and SONET mode when set =0. The S1201 will monitor the J0 byte for 3 consecutive single byte patterns (**RX_SDH_J0** =0) or 3 consecutive 16 byte patterns (**RX_SDH_J0** =1).

ADDR=0x10A: Receive Framer Position Control

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	RX_FIN_BYTE_TYPE[1:0]		RX_FIN_BYTE_NUMBER[3:0]			
R/W	x	x	R/W		R/W			
Default	x	x	0	0	0	0	0	0

RX_FIN_BYTE_TYPE[1:0] and RX_FIN_BYTE_NUMBER[3:0] Controls the relationship between the RX_FRAME_IN clock pulse and the data bytes on the input bus RX_DATA[7:0]. Refer to the tables below for configuration of these registers. Note that only 2 LSB's of **RX_FIN_BYTE_NUMBER[3:0]** are used for STS-3/STM-1 mode.

Table 32. STS-3c/STM-1 configuration for RX_FIN_BYTE_TYPE[1:0] and RX_FIN_BYTE_NUMBER[1:0]

Data on RX_DATA[7:0]	RX_FIN_BYTE_TYPE[1:0]	RX_FIN_BYTE_NUMBER[1:0]
last byte of frame	00	00
first A1 byte	00	01
second A1 byte	00	10
third A1 byte	01	00
first A2 byte	01	01
second A2 byte	01	10
third A2 byte	10	00
J0 byte	10	01
first Z0 byte	10	10
last Z0 byte	11	00
first byte after last Z0 byte	11	01
second byte after last Z0 byte	11	10

Table 33. STS-12c/STM-4 configuration for RX_FIN_BYTE_TYPE[1:0] and RX_FIN_BYTE_NUMBER[3:0]

Data on RX_DATA[7:0]	RX_FIN_BYTE_TYPE[1:0]	RX_FIN_BYTE_NUMBER[3:0]
last byte of frame	00	0000
first A1 byte	00	0001
. . .	. . .	. . .
eleventh A1 byte	00	1011
last A1 byte	01	0000
first A2 byte	01	0001
. . .	. . .	. . .
last Z0 byte	11	0000
first byte after last Z0 byte	11	0001
. . .	. . .	. . .
eleventh byte after last Z0 byte	11	1011

ADDR=0x10C: Receive LOH Status

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B2_ERR_SF	B2_ERR_SD	RX_LAIS	RX_LRDI	Reserved	K1_UNSTAB	Reserved	Reserved
R/W	R	R	R	R	X	R	X	X
Default	1	1	0	0	X	0	X	X

B2_ERR_SF If the B2 error rate is above the threshold specified in the **B2_THRESH_SET/CLR_SF** registers (ADDR 0x124), this bit will be set = 1.

B2_ERR_SD If the B2 error rate is above the threshold specified in the **B2_THRESH_SET/CLR_SD** registers (ADDR 0x12A), this bit will be set = 1.

RX_LAIS If the 3 LSB's of the received K2 byte are received as "111" for the number of consecutive frames specified in the **K2_CONSEC[3:0]** (ADDR 0x108) register, this bit will be set = 1. If the 3 LSB's of the received K2 byte are not received as "111" for the number of consecutive frames specified in the **K2_CONSEC[3:0]** register, this bit will be set = 0.

RX_LRDI If the 3 LSB's of the received K2 byte are received as "110" for the number of consecutive frames specified in the **K2_CONSEC[3:0]** (ADDR 0x108) register, this bit will be set = 1. If the 3 LSB's of the received K2 byte are not received as "110" for the number of consecutive frames specified in the **K2_CONSEC[3:0]** register, this bit will be set = 0.

K1_UNSTAB The K1 byte is checked for instability. If, for 12 successive frames, no 3 consecutive frames are received with identical K1 bytes, the **K1_UNSTAB** bit is set = 1. It is cleared when 3 consecutive identical K1 bytes are received.

ADDR=0x10D: Receive SOH Status

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	RX_LOS	RX_LOC	RX_OOF	RX_LOF	J0_OOF	Reserved
R/W	X	X	R	R	R	R	R	X
Default	X	X	0	0	0	1	1	1

RX_LOS Will be set = 1 when the S1201 receives Loss of Signal indication from the optical transceiver.

RX_LOC If no transitions are detected on *RX_SONETCLK* for 16 periods of *TX_CLK*, the **RX_LOC** bit is set = 1. It is cleared when transitions are detected.

RX_OOF If the receive framer receives 5 successive frames with at least 1 bit error in the A1-A1-A2-A2 framing pattern, **RX_OOF** is set = 1. When the framer finds 2 successive frames in which the A1-A1-A2-A2 framing bytes exactly match the framing pattern 0xF6F6-0x2828, it goes into frame and sets **RX_OOF** = 0.

RX_LOF If RX_OOF is active (= 1) continuously for 24 consecutive frames (3 ms), the **RX_LOF** bit is set = 1, indicating loss of frame. Once **RX_LOF** is set, it remains high until **RX_OOF** is inactive continuously for 3 ms.

J0_OOF The most significant bits(MSB's) of all J0 bytes are 0, except for the MSB of the frame start marker byte. The J0 monitor framer searches for 15 consecutive J0 bytes that have a 0 in their MSB, followed by a J0 byte with a 1 in its MSB. When this pattern is found, the framer goes into frame, and sets **J0_OOF** = 0. Once the J0 monitor framer is in-frame, it remains in-frame until 3 consecutive J0 bytes are received with at least 1 MSB bit error, at which point it sets **J0_OOF** = 1. If **RX_SDH_J0** is set = 0, the J0 frame indication is held in the in-frame state (**J0_OOF** = 0).

ADDR=0x110 - 0x11F: Receive J0 Bytes 0 - 15

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RX_J0_[0]_[7:0] . . . RX_J0_[15]_[7:0]							
R/W	R							
Default	0	0	0	0	0	0	0	0

Received J0 (Section Trace) The received 16 J0 bytes.

ADDR=0x121: Receive S1 LSBs

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	Reserved	RX_S1_[3:0]			
R/W	X	X	X	X	R			
Default	X	X	X	X	0	0	0	0

RX_S1_[3:0] (Synchronization Message) The received 4 LSB's of the S1 byte.

ADDR=0x122: Receive K2 Byte

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RX_K2_[7:0]							
R/W	R							
Default	0	0	0	0	0	0	0	0

RX_K2_[7:0] (APS Signalling) The received K2 byte.

ADDR=0x123: Receive K1 Byte

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RX_K1_[7:0]							
R/W	R							
Default	0	0	0	0	0	0	0	0

RX_K1_[7:0] (APS Signalling) The received K1 byte.

ADDR=0x124: Signal Fail Block Size

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B2_BLOCK_SF[7:0]							
R/W	R/W							
Default	0	0	0	0	0	0	0	1

ADDR=0x126: Signal Fail Threshold Set

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B2_THRESH_SET_SF[7:0]							
R/W	R/W							
Default	0	0	0	0	0	0	0	1

ADDR=0x127: Signal Fail Group Set

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	B2_GROUP_SET_SF[5:0]					
R/W	x	x	R/W					
Default	x	x	0	0	0	0	0	1

ADDR=0x128: Signal Fail Threshold Clear

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B2_THRESH_CLR_SF[7:0]							
R/W	R/W							
Default	0	0	0	0	0	0	0	1

ADDR=0x129: Signal Fail Group Clear

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	B2_GROUP_CLR_SF[5:0]					
R/W	x	x	R/W					
Default	x	x	0	0	0	0	0	1

ADDR=0x12A: Signal Degrade Block Size - LSB

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B2_BLOCK_SD[7:0]							
R/W	R/W							
Default	0	0	0	0	0	0	0	1

ADDR=0x12B: Signal Degrade Block Size - MSB

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B2_BLOCK_SD[15:8]							
R/W	R/W							
Default	0	0	0	0	0	0	0	0

ADDR=0x12C: Signal Degrade Threshold Set

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	B2_THRESH_SET_SD[5:0]					
R/W	x	x	R/W					
Default	x	x	0	0	0	0	0	1

ADDR=0x12D: Signal Degrade Group Set

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	B2_GROUP_SET_SD[5:0]					
R/W	x	x	R/W					
Default	x	x	0	0	0	0	0	1

ADDR=0x12E: Signal Degrade Threshold Clear

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	B2_THRESH_CLR_SD[5:0]					
R/W	x	x	R/W					
Default	x	x	0	0	0	0	0	1

ADDR=0x12F: Signal Degrade Group Clear

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	B2_GROUP_CLR_SD[5:0]					
R/W	x	x	R/W					
Default	x	x	0	0	0	0	0	1

For the purpose of determining whether or not the bit error rate of the received signal is above or below two different provisionable thresholds (the Signal Fail and the Signal Degrade conditions), the S1201 provides two B2 error rate threshold blocks. If the Signal Fail block or the Signal Degrade block determines that the error rate is above the threshold, it sets **B2_ERR_SF** or **B2_ERR_SD** (ADDR 0x10C). For each error rate threshold block, the user may provision a block register and 2 pairs of threshold and group registers. The 2 pairs of registers allow hysteresis in setting and clearing the state bits.

The values that should be programmed in these registers are a function of the desired BER at which Signal Fail and Signal Degrade should be set and cleared. These values are shown in the tables below. For a desired BER, the same values should be used for both the Signal Fail and the Signal Degrade registers.

Table 34. STS-3c/STM-1 Signal Fail and the Signal Degrade Values for given BER

BER	BLOCK	THRESH_SET	THRESH_CLR	GROUP_SET	GROUP_CLR
10^{-3}	3	28	7	4	5
10^{-4}	16	23	4	4	5
10^{-5}	160	28	4	2	5
10^{-6}	1600	28	4	2	5
10^{-7}	16,000	28	4	2	5

Table 34. STS-3c/STM-1 Signal Fail and the Signal Degrade Values for given BER

BER	BLOCK	THRESH_SET	THRESH_CLR	GROUP_SET	GROUP_CLR
10^{-8}	40,000	7	1	3	5
10^{-9}	65,000	2	1	4	28

Table 35. STS-12c/STM-4 Signal Fail and the Signal Degrade Values for given BER

BER	BLOCK	THRESH_SET	THRESH_CLR	GROUP_SET	GROUP_CLR
10^{-3}	1	39	8	4	5
10^{-4}	6	37	7	4	5
10^{-5}	40	28	4	2	5
10^{-6}	400	28	4	2	5
10^{-7}	4000	28	4	2	2
10^{-8}	20,000	15	2	2	4
10^{-9}	60,000	5	1	3	6

ADDR=0x130: Receive B1 Error Count - LSB

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B1_ERRCNT[7:0]							
R/W	R							
Default	0	0	0	0	0	0	0	0

ADDR=0x131: Receive B1 Error Count - MSB

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B1_ERRCNT[15:8]							
R/W	R							
Default	0	0	0	0	0	0	0	0

B1_ERRCNT[15:0] A 16-bit B1 error counter that either counts every B1 bit error (if **BIT_BLKCNT**, ADDR 0x00C is set = 0) or every frame with at least one B1 bit error (if **BIT_BLKCNT** is set = 1).

ADDR=0x134: Receive B2 Error Count - LSB

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B2_ERRCNT[7:0]							
R/W	R							
Default	0	0	0	0	0	0	0	0

ADDR=0x135: Receive B2 Error Count

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B2_ERRCNT[15:8]							
R/W	R							
Default	0	0	0	0	0	0	0	0

ADDR=0x136: Receive B2 Error Count - MSB

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	Reserved	B2_ERRCNT[19:16]			
R/W	X	X	X	X	R			
Default	X	X	X	X	0	0	0	0

B2_ERRCNT[19:0] A 20-bit B2 error counter that either counts every B2 bit error (if **BIT_BLKCNT**, ADDR 0x00C is set = 0) or every frame with at least one B2 bit error (if **BIT_BLKCNT** is set = 1).

ADDR=0x138: Receive M1 Error Count - LSB

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	M1_ERRCNT[7:0]							
R/W	R							
Default	0	0	0	0	0	0	0	0

ADDR=0x139: Receive M1 Error Count

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	M1_ERRCNT[15:8]							
R/W	R							
Default	0	0	0	0	0	0	0	0

ADDR=0x13A: Receive M1 Error Count - MSB

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	Reserved	M1_ERRCNT[19:16]			
R/W	X	X	X	X	R			
Default	X	X	X	X	0	0	0	0

M1_ERRCNT[19:0] Indicates the number of B2 errors that were detected by the remote terminal in its received signal. The S1201 contains a 20-bit M1 error counter that either counts every error indicated by M1 (if **BIT_BLKCNT**, ADDR 0x00C is set = 0) or every frame received with M1 not equal to 0 errors (if **BIT_BLKCNT** is set = 1). When configured for STS-3 mode, the valid range of values for M1 is 0 to 24; any other value is interpreted as 0 errors. When configured for STS-12 mode, the valid range of values for M1 is 0 to 96; any other value is interpreted as 0 errors. These values assume that **BIT_BLKCNT** is set = 0.

ADDR=0x142: Receive Pointer Interpreter Mask

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RX_LOP_D_MASK	RX_PAIS_D_MASK
R/W	x	x	x	x	x	x	R/W	R/W
Default	x	x	x	x	x	x	1	1

The bits in the **Receive Pointer Interpreter Mask** register are used to enable/disable status reporting of the corresponding event bits. Setting the mask bit=0 enables status reporting of the corresponding bit in the event register, setting the mask bit=1 disables it.

ADDR=0x144: Receive Pointer Interpreter Control

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RX_SDH_PI	RX_SS_EN
R/W	x	x	x	x	x	x	R/W	R/W
Default	x	x	x	x	x	x	0	0

RX_SDH_PI Determines whether the S1201 receive framer performs SONET or SDH pointer interpretation. If set = 1, SDH pointer interpretation is performed. If set = 0, SONET pointer interpretation is performed.

RX_SS_EN Determines whether or not the SS-bits are used in the Pointer Interpreter algorithms. If this bit is set = 1, **SS-bits** are used in the Pointer Interpreter algorithm, if clear, they are not.

ADDR=0x146: Receive Pointer Interpreter Delta

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RX_LOP_D	RX_PAIS_D
R/W	x	x	x	x	x	x	R/W	R/W
Default	x	x	x	x	x	x	0	0

RX_LOP_D/RX_PAIS_D Will be set = 1 if there is a change in state of the corresponding event bit. These bits are cleared by writing a 1 to them.

ADDR=0x148: Receive Pointer Tributary [1] Status

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	Reserved	PTR_STATE_[1]_[1:0]		RX_LOP	RX_PAIS
R/W	x	x	x	x	R		R	R
Default	x	x	x	x	0	0	0	0

PTR_STATE_[1]_[1:0] Monitors the first pair of H1/H2 pointer bytes in the received SONET/SDH frame, and indicates the current state of the S1201's pointer interpreter. A '00' indicates a normal pointer, a '01' indicates Alarm Indication Signal, and '10' indicates Loss of Pointer.

RX_LOP Receive Loss of Pointer indication.

RX_PAIS Receive Path Alarm Indication Signal.

ADDR=0x14A - 0x15E: Receive Pointer Tributary [2-12] Status

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	Reserved	PTR_STATE_[2]_[1:0] . . . PTR_STATE_[12]_[1:0]		Reserved	Reserved
R/W	x	x	x	x	R		x	x
Default	x	x	x	x	0	0	x	x

PTR_STATE_[2:12]_[1:0] Monitors the second through twelfth pair of H1/H2 pointer bytes (second and third if in STS-3 mode) for the correct concatenation indications, and indicates the current state of the S1201's pointer interpreter. A '11' indicates a correct concatenated pointer.

ADDR=0x160: Receive J1 Mode Control

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	J1_CRLF	J1_CAP	Reserved	RX_SDH_J1	Reserved	Reserved	Reserved	Reserved
R/W	R/W	R/W	X	R/W	X	X	X	X
Default	0	0	X	0	X	X	X	X

J1_CRLF If set = 1, the S1201 captures the first 64 byte string it receives in the J1 byte position that ends with {0D, 0A}. If set = 0, the S1201 captures the next 64 J1 bytes without regard to their content.

J1_CAP When J1_CAP transitions from 0 to 1, the S1201 captures 64 consecutive J1 bytes from the specified tributary and writes them to **RX_J1_[63:0]_[7:0]**.

RX_SDH_J1 If set =1 (normally used in SDH mode), the J1 bytes are expected to contain a repeating 16-byte path trace frame that includes the PAPI. In this mode, the **J1_CAP, J1_CRLF**, and **J1_CAP_E** bits are not used. For SONET mode, **RX_SDH_J1** should be set = 0.

ADDR=0x161: Receive RDI Monitor

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	G1_CONSEC[3:0]				Reserved	Reserved	Reserved	RX_PRDI5
R/W	R/W				X	X	X	R/W
Default	0	1	0	1	X	X	X	0

G1_CONSEC[3:0] Specifies the number of consecutive received G1 bytes which will be monitored to determine if a Path RDI indication is present.

RX_PRDI5 Is used to determine which bits of the G1 byte will be monitored for Path RDI indication. If set = 1, the S1201 will use only bit 5 of the received G1 byte. If set = 0, bits 5,6, and 7 of the received G1 byte will be used.

ADDR=0x162: Receive J1 Delta

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	Reserved	Reserved	J1_CAP_E	RX_J1_D	J1_OOF_D
R/W	x	x	x	x	x	R/W	R/W	R/W
Default	x	x	x	x	x	0	0	0

J1_CAP_E On completion of the capture of J1 bytes, **J1_CAP_E** will be set = 1.

RX_J1_D When a new value is stored in **RX_J1_[15:0]_[7:0]**, the **TX_J1_D** delta bit is set = 1.

J1_OOF_D The **J1_OOF_D** delta bit is set = 1 when **J1_OOF** changes state.

These bits are cleared by writing a 1 to them.

ADDR=0x163: Receive J1 Mask

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	Reserved	Reserved	J1_CAP_E_MASK	RX_J1_D_MASK	J1_OOF_D_MASK
R/W	x	x	x	x	x	R/W	R/W	R/W
Default	x	x	x	x	x	1	1	1

The bits in the **Receive J1 Mask** register are used to enable/disable status reporting of the corresponding event bits. Setting the mask bit=0 enables status reporting of the corresponding bit in the event register, setting the mask bit=1 disables it.

ADDR=0x164: Receive POH Mask

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	G1ERR_SECE_ MASK	B3ERR_SECE_ MASK	Reserved	RX_C2_D_ MASK	RX_G1_D_ MASK	RX_UNEQ_D _MASK	RX_PLM_D_ MASK	Reserved
R/W	R/W	R/W	X	R/W	R/W	R/W	R/W	X
Default	1	1	X	1	1	1	1	X

The bits in the **Receive G1 Mask** register are used to enable/disable status reporting of the corresponding event bits. Setting the mask bit=0 enables status reporting of the corresponding bit in the event register, setting the mask bit=1 disables it.

ADDR=0x165: Receive J1 OOF

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	J1_OOF
R/W	x	x	x	x	x	x	x	R
Default	x	x	x	x	x	x	x	1

J1_OOF The J1 monitor framer searches for 15 consecutive J1 bytes that have a 0 in their MSB, followed by a J1 byte with a 1 in its MSB. When this pattern is found, the framer goes into frame, and sets **J1_OOF** = 0. When this pattern match is lost (3 consecutive J1 bytes with MSB error), **J1_OOF** =1.

ADDR=0x166 - 0x1A5: Receive J1 Bytes 1 - 64

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RX_J1_[0]_[7:0] . . . RX_J1_[63]_[7:0]							
R/W	R							
Default	0	0	0	0	0	0	0	0

In SONET mode, the **RX_J1_[63:0]_[7:0]** registers hold the last captured path trace frame. In SDH mode, the last accepted path trace frame is held in the **RX_J1_[15:0]_[7:0].**

ADDR=0x1A6: Receive Path Delta

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	G1ERR_SECE	B3ERR_SECE	Reserved	RX_C2_D	RX_G1_D	RX_UNEQ_D	RX_PLM_D	Reserved
R/W	R/W	R/W	X	R/W	R/W	R/W	R/W	X
Default	0	0	X	0	0	0	0	X

G1ERR_SECE/B3ERR_SECE Will be set = 1 at the end of each second that the corresponding error status bits are in the active state at any time during the second.

RX_C2_D When a new C2 value is accepted, the **RX_C2_D** delta bit is set = 1.

RX_G1_D When a new value is stored in **RX_G1[2:0]**, the **RX_G1_D** delta bit is set =1.

RX_UNEQ_D When **RX_UNEQ** changes state, the **RX_UNEQ_D** delta bit is set =1.

RX_PLM_D When **RX_PLM** changes state, the **RX_PLM_D** delta bit is set =1.

These bits are cleared by writing 1 to them.

ADDR=0x1A8: Expected C2 Byte

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	EXP_C2_[7:0]							
R/W	R/W							
Default	0	0	0	0	0	0	0	1

The received C2 bytes are monitored so that reception of the correct type of payload can be verified. When a consistent C2 value is received for 5 consecutive frames, it is written to **RX_C2[7:0]**, and the **RX_C2_D** delta bit is set. The expected value of the received C2 bytes is provisioned in **EXP_C2[7:0]**. If the received value does not match the expected value, and it is NOT:

- the all zeros unequipped label
- the 0x01 equipped, non-specific label
- the 0xFC payload defect label
- the 0xFF reserved label

then the Payload Label Mismatch register bit, **RX_PLM**, is set = 1.

If the current accepted value is the all zeros Unequipped label, and **EXP_C2[7:0]** = 00, then the Unequipped register bit, **RX_UNEQ**, is set = 1.

ADDR=0x1AA: Receive POH UNEQ Monitor

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	RX_G1_[2:0]			TX_UNEQ	RX_PLM	Reserved
R/W	X	X	R			R	R	X
Default	X	X	0	0	0	0	0	X

RX_G1[2:0] When a consistent G1 monitor is received, bits 5, 6 and 7 of G1 are written to **RX_G1[2:0]**.

RX_UNEQ/RX_PLM RX_PLM and RX_UNEQ signals contribute to the insertion of Path RDI. See ADDR 0x1A8 for further explanation.

ADDR=0x1AB: Receive C2 Byte

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RX_C2_[7:0]							
R/W	R							
Default	0	0	0	0	0	0	0	1

When a consistent C2 value is received for 5 consecutive frames, the accepted value is written to **RX_C2[7:0]**.

ADDR=0x1AC: B3 Error Count - LSB

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B3_ERRCNT_[7:0]							
R/W	R							
Default	0	0	0	0	0	0	0	0

ADDR=0x1AD: B3 Error Count - MSB

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	B3_ERRCNT_[15:8]							
R/W	R							
Default	0	0	0	0	0	0	0	0

B3_ERRCNT[15:0] A 16-bit counter that either counts every BIP-8 (B3) error (if **BIT_BLKCNT**=0) or every frame with at least one B3 bit error (if **BIT_BLKCNT**=1)..

ADDR=0x1AE: G1 Error Count - LSB

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	G1_ERRCNT_[7:0]							
R/W	R							
Default	0	0	0	0	0	0	0	0

ADDR=0x1AF: G1 Error Count - MSB

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	G1_ERRCNT_[15:8]							
R/W	R							
Default	0	0	0	0	0	0	0	0

G1_ERRCNT[15:0] The S1201 contains a 16-bit G1 error counter that either counts every error indicated by G1 (if **BIT_BLKCNT**, ADDR 0x00C is set = 0) or every frame received with the first 4 bits of G1 not equal to 0 (if **BIT_BLKCNT** is set = 1).

ADDR=0x1C0: Receive ATM Error Mask

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	RX_ATM_HEC_DROP_SECE_MASK	RX_ATM_HEC_CORR_SECE_MASK	RX_ATM_LCD_SECE_MASK	RX_ATM_OCD_SECE_MASK	RX_ATM_LCD_D_MASK	RX_ATM_OCD_D_MASK	Reserved
R/W	X	R/W	R/W	R/W	R/W	R/W	R/W	X
Default	X	1	1	1	1	1	1	X

The bits in the **Receive ATM Error Mask** register are used to enable/disable status reporting of the corresponding event bits. Setting the mask bit=0 enables status reporting of the corresponding bit in the event register, setting the mask bit=1 disables it.

ADDR=0x1C3: Receive ATM LCD Time

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RX_ATM_LCD_TIME[5:0]						RX_ATM_ HEC_UDF	RX_ATM_ HEC_ENH
R/W	R/W						R/W	R/W
Default	1	0	0	0	0	0	0	1

RX_ATM_LCD_TIME Specifies the time interval used in the determination of ATM Loss of Cell Delineation. Each bit of the register represents 125 µs. Thus **RX_ATM_LCD_TIME** = 000000 corresponds to 0 ms., **RX_ATM_LCD_TIME** = 100000 corresponds to 4 ms.

RX_ATM_HEC_UDF Controls the location of the HEC byte within the two Utopia UDF bytes. If set = 0, the HEC is located in UDF1. If set = 1, the HEC is located in UDF2.

RX_ATM_HEC_ENH Enables or disables MOD2 addition of alternating 01010101 pattern to HEC calculation. A value of 1 enables the feature, a value of 0 disables it.

ADDR=0x1C4: Receive ATM Idle Cell Header Control

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RX_ATM_ IDLE_CLP	RX_ATM_IDLE_PTI_[2:0]			RX_ATM_IDLE_GFC[3:0]			
R/W	R/W	R/W			R/W			
Default	1	0	0	0	0	0	0	0

ADDR=0x1C5: Receive ATM Idle Cell Capture

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RX_ATM_ IDLE_CAP	Reserved	Reserved	RX_ATM_IDLE_BYTE[5:0]				
R/W	R/W	X	X	R/W				
Default	0	X	X	0	0	0	0	0

ADDR=0x1C8: Receive ATM Idle Cell Data

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RX_ATM_IDLE_DATA[7:0]							
R/W	R							
Default	0	0	0	0	0	0	0	0

RX_ATM_IDLE_CLP, RX_ATM_IDLE_PTI[2:0], RX_ATM_IDLE_GFC[3:0] Provisionable fields that allow the user to define an idle ATM cell header within the incoming data stream.

The S1201 provides the capability for the user to monitor the data bytes of idle cells. **RX_ATM_IDLE_BYTE[5:0]** indicates which byte of the ATM idle cell payload is monitored. This register is interpreted as directly identifying the byte position in the idle cell payload; values 1 through 48 indicate the first through 48th byte of the idle payload, other values are undefined. When **RX_ATM_IDLE_CAP** is written from 0 to 1, the S1201 captures the next ATM idle cell it detects in the indicated payload byte position, and stores it in **RX_ATM_IDLE_DATA[7:0]**.

ADDR=0x1CA: Receive ATM Error Events

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	RX_ATM_HEC_DROP_SECE	RX_ATM_HEC_CORR_SECE	RX_ATM_LCD_SECE	RX_ATM_OCD_SECE	RX_ATM_LCD_D	RX_ATM_OCD_D	Reserved
R/W	X	R/W	R/W	R/W	R/W	R/W	R/W	X
Default	X	0	0	0	0	0	0	X

RX_ATM_HEC_DROP_SECE, RX_ATM_HEC_CORR_SECE, RX_ATM_LCD_SECE, RX_ATM_OCD_SECE Will be set = 1 at the end of each second or monitoring interval that the corresponding error status bits are in the active state at any time during the second.

RX_ATM_LCD_D When **RX_ATM_LCD** changes state, the **RX_ATM_LCD_D** delta bit is set =1.

RX_ATM_OCD_D When **RX_ATM_OCD** changes state, the **RX_ATM_OCD_D** delta bit is set =1.

These bits are cleared by writing a 1 to them.

ADDR=0x1CC: Receive ATM HEC Control

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RX_ATM_HEC_INH
R/W	x	x	x	x	x	x	x	R/W
Default	x	x	x	x	x	x	x	0

RX_ATM_HEC_INH If set = 1, the S1201 operates in HEC detection only mode, where single error correction is disabled and all cells with errored headers are discarded.

ADDR=0x1CD: Receive ATM Status

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	Reserved	Reserved	RX_ATM_LCD	RX_ATM_OCD	Reserved
R/W	x	x	x	x	x	R	R	x
Default	x	x	x	x	x	1	1	x

RX_ATM_LCD If an LCD error occurs, **RX_ATM_LCD** will be set = 1. This bit is cleared when the LCD condition terminates.

RX_ATM_OCD If an OCD error occurs, **RX_ATM_OCD** will be set = 1. This bit is cleared when the OCD condition terminates.

ADDR=0x1D0: Receive SBE Correct Count - LSB

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RX_ATM_HEC_CORR_[7:0]							
R/W	R							
Default	0	0	0	0	0	0	0	0

ADDR=0x1D1: Receive SBE Correct Count - MSB

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RX_ATM_HEC_CORR_[15:8]							
R/W	R							
Default	0	0	0	0	0	0	0	0

RX_ATM_HEC_CORR_[15:0] A 16-bit register that contains the number of single-bit errors that are corrected by the HEC processor.

ADDR=0x1D2: Receive HEC Discards Count - LSB

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RX_ATM_HEC_DROP_[7:0]							
R/W	R							
Default	0	0	0	0	0	0	0	0

ADDR=0x1D3: Receive HEC Discards Count - MSB

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RX_ATM_HEC_DROP_[15:8]							
R/W	R							
Default	0	0	0	0	0	0	0	0

RX_ATM_HEC_DROP_[15:0] A 16-bit register that contains the number of cells that are discarded due errored cell headers.

ADDR=0x1D4: Receive Cell Count - LSB

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RX_ATM_CELL_CNT_[7:0]							
R/W	R							
Default	0	0	0	0	0	0	0	0

ADDR=0x1D5: Receive Cell Count

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RX_ATM_CELL_CNT_[15:8]							
R/W	R							
Default	0	0	0	0	0	0	0	0

ADDR=0x1D6: Receive Cell Count - MSB

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	RX_ATM_CELL_CNT_[20:16]				
R/W	X	X	X	R				
Default	X	X	X	0	0	0	0	0

RX_ATM_CELL_CNT_[20:16] Counter for valid received ATM cells, excluding idle cells. The counter is updated at the end of a monitoring interval. The monitoring interval can be one second (if **CNT_SEC_EN**), or can be set by the user, by writing **LATCH_CNT** with a 1. The counter freezes when it reaches its maximum value. It does not reset to 0.

ADDR=0x1E0: Receive FIFO Overflow Mask

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	Reserved	RX_FIFOOVER_ SECE_MASK	RX_FIFOOVER_E_ MASK	Reserved	Reserved
R/W	X	X	X	X	R/W	R/W	X	X
Default	X	X	X	X	1	1	X	X

The bits in the **Receive FIFO Overflow Mask** register are used to enable/disable status reporting of the corresponding event bits. Setting the mask bit=0 enables status reporting of the corresponding bit in the event register, setting the mask bit=1 disables it.

ADDR=0x1E2: Receive System I/F Control

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	RX_SYSINT_8BIT	RX_SYSINT_POLL	RX_SYSINT_ GRPADD_INH	Reserved	RX_PRTY_MODE	Reserved	RX_CLAV_DSST
R/W	X	R/W	R/W	R/W	X	R/W	X	R/W
Default	X	0	1	1	X	0	X	0

RX_SYSINT_8BIT Controls whether the receive system interface operates in 8 or 16 bit mode. Sixteen bit data bus operation is selected by setting **RX_SYSINT_8BIT** = 0. Eight bit data bus operation is selected by setting **RX_SYSINT_8BIT** = 1.

RX_SYSINT_POLL The S1201 supports multiplexed polled Utopia Level 2 operation by setting **RX_SYSINT_POLL** = 1. If the bit is set = 0, the S1201 operates in direct status mode.

RX_SYSINT_GRPADD If **RX_SYSINT_GRPADDR_INH** is set = 0, whenever its assigned polling group address is present on the address bus RX_ADR[4:2], the S1201 drives its' RX_PRPA signal. RX_ADR[1:0] do not play a role in polling in this mode of operation. In this way, the Link Layer can poll multiple CLAV(PRPA) signals in a single clock cycle. If **RX_SYSINT_GRPADDR_INH** is set = 1, the S1201 drives RX_PRPA only when its assigned full address is present on the address bus RX_ADR[4:0]. In both modes, whenever the PHYADDR does not correspond to the address (Polling Group or full) last presented on RX_ADR, RX_CLAV(PRPA) is tristated.

RX_PRTY_MODE When set=1, even parity will be used. When set=0, odd parity will be used.

RX_CLAV_DSST In the receive direction, RX_CLAV is asserted when there is sufficient space available in the RX FIFO to accommodate an entire ATM cell. If **RX_CLAV_DSST** is set = 0, RX_CLAV is deasserted four clock cycles before the end of the cell transfer, if the TR FIFO cannot accommodate another cell. If **RX_CLAV_DSST** is set = 1, RX_CLAV is deasserted one clock cycle after the end of the cell transfer, if the RX FIFO cannot accommodate another cell.

ADDR=0x1E4: Receive FIFO Low-watermark

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	RX_FIFOEMPTY_RPA[4:0]				
R/W	x	x	x	R/W				
Default	x	x	x	0	1	1	1	1

ADDR=0x1E5: Receive FIFO High-watermark

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	RX_FIFOFULL_RPA[4:0]				
R/W	x	x	x	R/W				
Default	x	x	x	1	1	1	0	1

The S1201 allows the user to configure the low and high watermarks for the receive FIFO by writing to the **RX_FIFOEMPTY_RPA** and **RX_FIFOFULL_RPA** registers. If the receive FIFO falls below, or rises above these thresholds, the S1201 will notify the link layer via the RX_CLAV(PRPA) signal. To insure proper operation of this function, the **RX_FIFOFULL_RPA** setting must be greater than **RX_FIFOEMPTY_RPA**. The table below illustrates how the bits in these registers are interpreted.

RX_FIFOFULL/EMPTY_RPA setting	# of bytes for high/low watermark
00000	8
00001	16
: :	: :
11111	256

ADDR=0x1E6: Receive FIFO Overflow Events

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	Reserved	RX_FIFOOVER_ SECE	RX_FIFOOVER_E	Reserved	Reserved
R/W	X	X	X	X	R/W	R/W	X	X
Default	X	X	X	X	0	0	X	X

RX_FIFOOVER_SECE Will be set = 1 at the end of each monitoring interval in which the **RX_FIFOOVER_E** event bit is in the active state at any time during the second.

RX_FIFOOVER_E Will be set = 1 if a receive FIFO overflow has occurred.

These bits are cleared by writing 1 to them.

ADDR=0x1E8: Receive FIFO Overflow Count

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RX_FIFOOVER_ERRCNT_[7:0]							
R/W	R							
Default	0	0	0	0	0	0	0	0

RX_FIFOOVER_ERRCNT[7:0] An 8-bit counter that counts every cell/packet affected by a receive FIFO overflow event.

ADDR=0x1F0: Receive POS Error Mask

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	RX_POS_FCS_ERR_ SECE_MASK	RX_POS_PMIN_ER R_SECE_MASK	RX_POS_PMAX_ ERR_SECE_MASK	RX_POS_PABORT_ ERR_SECE_MASK	RX_POS_ADRCTL_ INVALID_D_MASK
R/W	x	x	x	R/W	R/W	R/W	R/W	R/W
Default	x	x	x	1	1	1	1	1

The bits in the **Receive POS Error Mask** register are used to enable/disable status reporting of the corresponding event bits. Setting the mask bit=0 enables status reporting of the corresponding bit in the event register, setting the mask bit=1 disables it.

ADDR=0x1F1: Receive POS Min Pkt Size

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	RX_POS_FCS_BIT_ORDR	RX_POS_PMIN[3:0]			
R/W	x	x	x	R/W	R/W			
Default	x	x	x	0	0	0	0	0

RX_POS_FCS_BIT_ORDR If set = 1, received data is read into the shift register in little endian bit order (LSB first). If set = 0, the received data is read into the shift register in big endian bit order (MSB first).

RX_POS_PMIN[3:0] A programmable value for the minimum received PPP packet size. The packet size refer to the size of the PPP packet only, and do not include the bytes inserted by the S1201 (flag sequence, address, control, FIFO underflow, transparency or the FCS bytes).

ADDR=0x1F2: Receive POS Max Pkt Size - LSB

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RX_POS_PMAX[7:0]							
R/W	R/W							
Default	1	1	1	0	0	0	0	0

ADDR=0x1F3: Receive POS Max Pkt Size - MSB

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RX_POS_PMAX[15:8]							
R/W	R/W							
Default	0	0	0	0	0	1	0	1

RX_POS_PMAX[15:0] A programmable value for the maximum received PPP packet size. The default value is 0x05E0.

ADDR=0x1F4: Receive POS FIFO Fill Pattern

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RX_POS_FIFOUNDR_BYTE[7:0]							
R/W	R/W							
Default	1	0	1	0	0	0	0	0

RX_POS_FIFOUNDR_BYTE[7:0] Contains the byte pattern that may be inserted to the received data stream during periods of Rx FIFO underflow. The pattern is inserted if **RX_POS_FIFOUNDR_MODE** (ADDR=0x1F6) is set =1.

ADDR=0x1F5: Receive POS Error

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	RX_POS_FCS_ERR_SECE	RX_POS_PMIN_ERR_SECE	RX_POS_PMAX_ERR_SECE	RX_POS_PABORT_ERR_SECE	RX_POS_ADRCTL_INVALID_D
R/W	x	x	x	R/W	R/W	R/W	R/W	R/W
Default	x	x	x	0	0	0	0	0

RX_POS_FCS_ERR_SECE,RX_POS_PMIN_ER_SECE, RX_POS_PMAX_ERR_SECE, RX_POS_PABORT_ERR_SECE Will be set = 1 at the end of each monitoring interval in which the corresponding error occurred at any time during the interval.

RX_POS_ADRCTL_INVALID_D When **RX_POS_ADRCTL_INVALID** changes state, the **RX_POS_ADRCTL_INVALID_D** delta bit is set =1.

These bits are cleared by writing a 1 to them.

ADDR=0x1F6: Receive POS Control

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	RX_POS_FIFOUNDR_MODE	RX_POS_PMIN_ENB	RX_POS_PMAX_ENB	Reserved	RX_POS_FCS_INH	RX_POS_FCS_MODE	RX_POS_ADRCTL_DROP_INH
R/W	X	R/W	R/W	R/W	X	R/W	R/W	R/W
Default	X	0	0	0	X	0	0	0

RX_POS_FIFOUNDR_MODE If set = 1, the **RX_POS_FIFOUNDR_BYTE[7:0]** was inserted into the bit stream by the transmit end during periods of FIFO underflow. The receiver will then search for this pattern, prior to transparency processing, and delete it.

RX_POS_PMIN_ENB When set = 1, any packet received which is below the packet size threshold specified in the **RX_POS_PMIN[3:0]** register is marked as errored.

RX_POS_PMAX_ENB When set = 1, any packet received which is above the packet size threshold specified in the **RX_POS_PMAX[15:0]** register is marked as errored.

RX_POS_FCS_INH In POS mode, a FCS is calculated and checked against the FCS bytes at the end of each frame if **RX_POS_FCS_INH** is set = 0. Setting **RX_POS_FCS_INH** = 1 disables FCS checking.

RX_POS_FCS_MODE When set=1, the S1201 is placed in FCS-16 mode, and provides FCS-16 functionality using the following generator polynomial: $1 + X^5 + X^{12} + X^{16}$. When set=0, the S1201 is placed in FCS-32 mode, and provides FCS-32 functionality using the following generator polynomial: $1 + X + X^2 + X^4 + X^5 + X^7 + X^8 + X^{10} + X^{11} + X^{12} + X^{16} + X^{22} + X^{23} + X^{26} + X^{32}$.

RX_POS_ADRCTL_DROP_INH If set = 0, the S1201 examines the address and control bytes (the first two bytes of the HDLC frame following the Flag Sequence) and if valid, does not pass them on to the Rx FIFO. If set = 1, the automatic drop feature is inhibited.

ADDR=0x1F7: Receive POS Addr/Ctrl Status

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RX_POS_ADRCTL_ INVALID
R/W	x	x	x	x	x	x	x	R
Default	x	x	x	x	x	x	x	0

RX_POS_ADRCTL_INVALID Indicates whether the received POS Address and Control bytes are valid. If set = 0 the bytes are valid, if set = 1 the bytes are invalid.

ADDR=0x1F8: Receive POS Aborts

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RX_POS_PABORT_ERRCNT[7:0]							
R/W	R							
Default	0	0	0	0	0	0	0	0

RX_POS_PABORT_ERRCNT An 8-bit error counter that counts every packet in which the abort sequence is detected.

ADDR=0x1FA: Receive POS Giant Pkt Count

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RX_POS_PMAX_ERRCNT[7:0]							
R/W	R							
Default	0	0	0	0	0	0	0	0

ADDR=0x1FB: Receive POS Runt Pkt Count

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RX_POS_PMIN_ERRCNT[7:0]							
R/W	R							
Default	0	0	0	0	0	0	0	0

RX_POS_PMAX_ERRCNT[7:0] and **RX_POS_PMIN_ERRCNT[7:0]** count the number of packets received from the line side that violate minimum and maximum packet lengths.

ADDR=0x1FC: Receive POS FCS Error Count - LSB

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RX_POS_FCS_ERRCNT[7:0]							
R/W	R							
Default	0	0	0	0	0	0	0	0

ADDR=0x1FD: Receive POS FCS Error Count

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RX_POS_FCS_ERRCNT[15:8]							
R/W	R							
Default	0	0	0	0	0	0	0	0

ADDR=0x1FE: Receive POS FCS Error Count - MSB

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	Reserved	Reserved	Reserved	RX_POS_FCS_ERRCNT[19:16]			
R/W	X	X	X	X	R			
Default	X	X	X	X	0	0	0	0

RX_POS_FCS_ERRCNT[19:0] A 20-bit FCS error counter that counts every FCS CRC violation in the received packets.

ADDR=0x1FF: Device Identification Code - Addr - 0x1FF

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	DEV_ID[7:0]							
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	1

This register holds a device identification number for the CONGO. **DEV_ID[7:0] =** 0x01

11.0 Summary Register Map Tables

Table 36. Common Configuration and Summary Status Map

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset Control (Read/Write)									
000	0x00					TX_CNT_LOAD		TX_STATE_RESET	TX_PROV_RESET
001	0x00					RX_CNT_LOAD	LATCH_CNT	RX_STATE_RESET	RX_PROV_RESET
Transmit Side Summary Interrupt and Summary Delta/Event (Read Only)									
002	0x00							RX_APS_INT	SUM_INT
003	0x00	DEV_VER[7:0]							
004	0x00	LATCH_E				TX_ATM_HEC_SUME	GPIO_SUMD	TX_POS_PKTERR_SECE_SUME	TX_FIFO_SUME
005	0x00	TOH_SUMD	TOH_SECE_SUM	PTR_INT_PAIS_SUMD	PATH_SUMD	ATM_SUMD	POS_SUME	RX_FIFO_SUME	RX_ATM_IDLE_CAP_E
Summary Masks (Read/Write)									
006	0x03							RX_APS_INT_MASK	SUM_INT_MASK
007									
008	0x0F	LATCH_E_MASK				TX_ATM_HEC_SUME_MASK	GPIO_SUMD_MASK	TX_POS_PKTERR_SECE_SUME_MASK	TX_FIFO_SUME_MASK
009	0xFF	TOH_SUMD_MASK	TOH_SECE_SUM_MASK	PTR_INT_PAIS_SUMD_MASK	PATH_SUMD_MASK	ATM_SUMD_MASK	POS_SUME_MASK	RX_FIFO_SUME_MASK	RX_ATM_IDLE_CAP_E_MASK
Configuration, Loopback and GPIO Provisioning (Read/Write)									
00A	0x00				RX_DSCR_INH		RX_SIG_MODE	RX_DIRECT_MAP	RX_POS
00B	0x00			TX_UNEQ	TX_SCR_INH		TX_SIG_MODE	TX_DIRECT_MAP	TX_POS
00C	0x00		CNT_SEC_EN			BIT_BLKCNT	SYS_T_TO_R_LOOP	SYS_R_TO_T_LOOP	SONET_T_TO_R_LOOP
00D	0x00					GPIOCTL1	GPIOCTL2	GPIOCTL3	GPIOCTL4
General Purpose Inputs/Outputs Delta (Read Only)									
00E	0x00	GPIO7_D	GPIO6_D	GPIO5_D	GPIO4_D	GPIO3_D	GPIO2_D	GPIO1_D	GPIO0_D
00F									
General Purpose Inputs/Outputs Mask Bits (Read/Write)									
010	0xFF	GPIO7_MASK	GPIO6_MASK	GPIO5_MASK	GPIO4_MASK	GPIO3_MASK	GPIO2_MASK	GPIO1_MASK	GPIO0_MASK
011									
General Purpose Inputs/Outputs									
012	0x00					GPIO3	GPIO2	GPIO1	GPIO0

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
013									
014	0x00					GPIO7	GPIO6	GPIO5	GPIO4

Table 37. Transmit Side Register Address Map for SONET/SDH TOH/SOH Provisioning and Scrambler Inhibit

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SONET/SDH Line/MS AIS Generation Control, Scrambler Inhibit, and TOH/SOH Provisioning (Read/Write)									
020	0x00	A1A2_ERR	A1A2_ERR_NUM[2:0]			B1_INV	B2_INV	TX_M1_ERR	SCRINH
021	0x00	TX_LAIS	TX_SDH_PG					LRDI_INH	LREI_INH
022	0x00	A1A2_ERR_PAT[7:0]							
023	0x00	A1A2_ERR_PAT[15:8]							
024	0x01	TX_J0_[0]_[7:0]							
025	0x01	TX_J0_[1]_[7:0]							
026	0x01	TX_J0_[2]_[7:0]							
027	0x01	TX_J0_[3]_[7:0]							
028	0x01	TX_J0_[4]_[7:0]							
029	0x01	TX_J0_[5]_[7:0]							
02A	0x01	TX_J0_[6]_[7:0]							
02B	0x01	TX_J0_[7]_[7:0]							
02C	0x01	TX_J0_[8]_[7:0]							
02D	0x01	TX_J0_[9]_[7:0]							
02E	0x01	TX_J0_[10]_[7:0]							
02F	0x01	TX_J0_[11]_[7:0]							
030	0x01	TX_J0_[12]_[7:0]							
031	0x01	TX_J0_[13]_[7:0]							
032	0x01	TX_J0_[14]_[7:0]							
033	0x01	TX_J0_[15]_[7:0]							
034	0x00	TX_K2_[7:0]							
035	0x00	TX_K1_[7:0]							
036	0x00	TX_S1_[7:0]							
037	0x00			TX_FOUT_BYTE_TYPE[1:0]		TX_FOUT_BYTE_NUMBER[3:0]			

Table 38. Transmit Side Register Address Map for Path/AU AIS Generation and Path Overhead Provisioning

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Path Overhead Provisioning (Read/Write)									
040	0x00						PREI_INH	PRDI_ENH	PRDI_AUTO
041									
J1 Path Trace Messages (Read/Write)									
042	0x00	TX_J1_[0]_[7:0]							
043	0x00	TX_J1_[1]_[7:0]							
044 to 07F	0x00	: : :							
080	0x00	TX_J1_[62]_[7:0]							
081	0x00	TX_J1_[63]_[7:0]							
SONET/SDH Path/AU AIS Generation Control and Path Overhead Provisioning (Read/Write)									

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
084	0x00	FORCE_ G1ERR	TX_G1_[2:0]					B3_INV	TX_PAIS
085	0x00	TX_C2_[7:0]							
086	0x01								TX_J1SEL

Table 39. Transmit Side Register Address Map for ATM Provisioning

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Utopia Level 2 and ATM Summary Masks (Read/Write)									
090	0x01								TX_ATM_HEC_ ERR_E_ MASK
091									
Utopia Level 2 and ATM Provisioning(Read/Write)									
092									
093	0x01						TX_ATM_ UTP_HEC_ INH	TX_ATM_ HEC_UDF	TX_ATM_HEC_ ENH
094	0x80	TX_ATM_ IDLE_ CLP	TX_ATM_IDLE_PTI[2:0]			TX_ATM_IDLE_GFC[3:0]			
095	0x6A	TX_ATM_IDLE_DATA[7:0]							
Event Bits (Read Only, cleared by uP)									
096	0x00								TX_ATM_HEC_ ERR_E
097									
Provisioning (Read/Write)									
098									
099	0x00				TX_ATM_ HEC_INH				
ATM Valid Cell and Idle Cell Counters (Read Only)									
0A0	0x00	TX_ATM_CELL_CNT_[7:0]							
0A1	0x00	TX_ATM_CELL_CNT_[15:8]							
0A2	0x00				TX_ATM_CELL_CNT_[20:16]				

Table 40. Transmit Side Register Address Map for System Interface Provisioning (Addr 0xB0)

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
System Interface Summary Masks (Read/Write)									
0B0	0x0E					TX_FIFOERR_ SECE_ MASK	TX_FIFOERR_ E_MASK	TX_PRTY_ ERR_E_ MASK	
0B1									
System Interface Provisioning(Read/Write)									
0B2	0x30		TX_SYSINT_ 8BIT	TX_SYSINT_ POLL	TX_SYSINT_ GRPADD_INH		TX_PRTY_ MODE		TX_CLAV_ DSST

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0B3									
0B4	0x0F				TX_FIFOEMPTY_TPA[4:0]				
0B5	0x1D				TX_FIFOFULL_TPA[4:0]				
System Interface Event Bits (Read Only, cleared by uP)									
0B6	0x00					TX_FIFOERR_SECE	TX_FIFOERR_E	TX_PRTY_ERR_E	
0B7									
System Interface PHY Address Provisioning (Read/Write)									
0B8	0x1F				PHYADDR[4:0]				
0B9									
System Interface FIFO Error Counter (Read Only)									
0BA	0x00	TX_FIFOERR_CNT[7:0]							
0BB									

Table 41. Transmit Side Register Address Map for POS Provisioning

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POS Summary Mask Bits (Read/Write)									
0C0	0x1F				TX_POS_FIFOUNDR_ERR_SECE_MASK	TX_POS_PMIN_ERR_SECE_MASK	TX_POS_PMAX_ERR_SECE_MASK	TX_POS_LLPKT_ERR_SECE_MASK	TX_POS_FIFOUNDR_E_MASK
0C1									
POS Provisioning(Read/Write)									
0C2	0x00								TX_POS_FCSABRT_ENB
0C3	0x00				TX_POS_FCS_BIT_ORDR	TX_POS_PMIN[3:0]			
0C4	0xE0	TX_POS_PMAX[7:0]							
0C5	0x05	TX_POS_PMAX[15:8]							
0C6	0x50	TX_POS_FIFOUNDER_BYTE[7:0]							
POS Event and Second Event Bits (Read Only, Cleared by microprocessor)									
0C8	0x00				TX_POS_FIFOUNDR_ERR_SECE	TX_POS_PMIN_ERR_SECE	TX_POS_PMAX_ERR_SECE	TX_POS_LLPKT_ERR_SECE	TX_POS_FIFOUNDR_E
0C9									
POS Provisioning(Read/Write)									
0CA	0x00		TX_POS_FIFOUNDR_MODE	TX_POS_PMIN_ENB	TX_POS_PMAX_ENB	TX_POS_FCS_MODE	TX_POS_FCS_INH	TX_POS_EOP_FLAG	TX_POS_ADRCTL_INS
0CB									
POS Errored Packet Counters (Read Only)									
0CC	0x00	TX_POS_FIFOUNDR_ERRCNT[7:0]							
0CD	0x00	TX_POS_LLPKT_ERRCNT[7:0]							
0CE	0x00	TX_POS_PMAX_ERRCNT[7:0]							
0CF	0x00	TX_POS_PMIN_ERRCNT[7:0]							

Table 42. Receive Side Register Address Map for SONET/SDH TOH/SOH Monitoring

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TOH/SOH Delta and Second Event Bits (Read Only, Cleared by microprocessor)									
100	0x00	B2_ERR_SF_D	B2_ERR_SD_D	RX_LAIS_D	RX_LRDI_D	RX_K1_D	K1_UNSTAB_D	RX_K2_D	RX_S1_D
101	0x00			RX_LOS_D	RX_LOC_D	RX_OOF_D	RX_LOF_D	J0_OOF_D	RX_J0_D
102	0x00			RX_OOF_SECE	RX_LOF_SECE_	B1_ERR_SECE	B2_ERR_SECE	S1_FAIL_SECE	M1_ERR_SECE
103									
TOH/SOH Masks and Provisioning Bits (Read/Write)									
104	0xFF	B2_ERR_SF_D_MASK	B2_ERR_SD_D_MASK	RX_LAIS_D_MASK	RX_LRDI_D_MASK	RX_K1_D_MASK	K1_UNSTAB_D_MASK	RX_K2_D_MASK	RX_S1_D_MASK
105	0x3F			RX_LOS_D_MASK	RX_LOC_D_MASK	RX_OOF_D_MASK	RX_LOF_D_MASK	J0_OOF_D_MASK	RX_J0_D_MASK
106	0x3F			RX_OOF_SECE_MASK	RX_LOF_SECE_MASK	B1_ERR_SECE_MASK	B2_ERR_SECE_MASK	S1_FAIL_SECE_MASK	M1_ERR_SECE_MASK
107									
108	0x50	K2_CONSEC[3:0]						RX_LOF_ALG	DSCRINH
109	0x00		RX_LOS_LEVEL	RX_LOS_INH	RX_FRMR_INH			RX_SDH_S1	RX_SDH_J0
10A	0x00			RX_FIN_BYTE_TYPE[1:0]		RX_FIN_BYTE_NUMBER[3:0]			
10B									
TOH/SOH Status (Read Only)									
10C	0xC0	B2_ERR_SF	B2_ERR_SD	RX_LAIS	RX_LRDI		K1_UNSTAB		
10D	0x0E			RX_LOS	RX_LOC	RX_OOF	RX_LOF	J0_OOF	
110	0x00	RX_J0_[0]_[7:0]							
111	0x00	RX_J0_[1]_[7:0]							
112	0x00	RX_J0_[2]_[7:0]							
113 to 11D	0x00	: : :							
11E	0x00	RX_J0_[14]_[7:0]							
11F	0x00	RX_J0_[15]_[7:0]							
120									
121	0x00					RX_S1_[3:0]			
122	0x00	RX_K2_[7:0]							
123	0x00	RX_K1_[7:0]							
Signal Fail & Signal Degrade Parameters (Read/Write)									
124	0x01	B2_BLOCK_SF[7:0]							
125									
126	0x01	B2_THRESH_SET_SF[7:0]							
127	0x01			B2_GROUP_SET_SF[5:0]					
128	0x01	B2_THRESH_CLR_SF[7:0]							

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
129	0x01			B2_GROUP_CLR_SF[5:0]					
12A	0x01	B2_BLOCK_SD[7:0]							
12B	0x00	B2_BLOCK_SD[15:8]							
12C	0x01			B2_THRESH_SET_SD[5:0]					
12D	0x01			B2_GROUP_SET_SD[5:0]					
12E	0x01			B2_THRESH_CLR_SD[5:0]					
12F	0x01			B2_GROUP_CLR_SD[5:0]					
Performance Monitoring Counters (Read Only)									
130	0x00	B1_ERRCNT[7:0]							
131	0x00	B1_ERRCNT[15:8]							
132									
133									
134	0x00	B2_ERRCNT[7:0]							
135	0x00	B2_ERRCNT[15:8]							
136	0x00					B2_ERRCNT[19:16]			
137									
138	0x00	M1_ERRCNT[7:0]							
139	0x00	M1_ERRCNT[15:8]							
13A	0x00					M1_ERRCNT[19:16]			

Table 43. Receive Side Register Address Map for SONET/SDH Pointer Interpreter

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Pointer Interpreter Delta bits (Read Only, Cleared by microprocessor)									
140									
141									
Pointer Interpreter Summary Mask Bits (Read/Write)									
142	0x03							RX_LOP_D MASK	RX_PAIS_D_ MASK
143									
Pointer Interpreter Provisioning (Read/Write)									
144	0x00							RX_SDH_ PI	RX_SS_EN
145									
Pointer Interpreter Delta Bits (Read Only, cleared by microprocessor)									
146	0x00							RX_LOP_D	RX_PAIS_D
147									
Tributary [1] Pointer Interpreter Status (Read Only)									
148	0x00					PTR_STATE_[1]_[1:0]		RX_LOP	RX_PAIS
149									
Tributary [2] Pointer Interpreter Status (Read Only)									
14A	0x00					PTR_STATE_[2]_[1:0]			
14B									
Tributary [3] Pointer Interpreter Status (Read Only)									
14C	0x00					PTR_STATE_[3]_[1:0]			
14D									

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
14E to 15B						: : :			
Tributary [11] Pointer Interpreter Status (Read Only)									
15C	0x00					PTR_STATE_[11]_[1:0]			
15D									
Tributary [12] Pointer Interpreter Status (Read Only)									
15E	0x00					PTR_STATE_[12]_[1:0]			
15F									

Table 44. Receive Side Register Address Map for SONET/SDH Path Monitoring

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Path Provisioning (Read/Write)									
160	0x00	J1_CRLF	J1_CAP		RX_SDH_ J1				
161	0x50	G1_CONSEC[3:0]							RX_PRDI5
Path J1 Monitoring Interrupt and Delta Bit (Read Only, Cleared by microprocessor)									
162	0x00						J1_CAP_E	RX_J1_D	J1_OOF_D
Path Summary Mask Bits (Read/Write)									
163	0x07						J1_CAP_E_ MASK	RX_J1_D_ MASK	J1_OOF_D_ MASK
164	0xDE	G1ERR_ SECE_MASK	B3ERR_ SECE_MASK		RX_C2_D_ MASK	RX_G1_D_ MASK	RX_UNEQ_D _MASK	RX_PLM_D_ MASK	
J1 Monitoring (Read Only)									
165	0x01								J1_OOF
166	0x00	RX_J1_[0]_[7:0]							
167	0x00	RX_J1_[1]_[7:0]							
168 to 1A3	0x00					: : :			
1A4	0x00	RX_J1_[62]_[7:0]							
1A5	0x00	RX_J1_[63]_[7:0]							
Path Delta and Second Event Bits (Read Only, Cleared by microprocessor)									
1A6	0x00	G1ERR_SECE	B3ERR_SECE		RX_C2_D	RX_G1_D	RX_UNEQ_D	RX_PLM_D	
1A7									
Path Provisioning									
1A8	0x01	EXP_C2_[7:0]							
1A9									
Path Status (Read Only)									
1AA	0x00			RX_G1_[2:0]			RX_UNEQ	RX_PLM	
1AB	0x00	RX_C2_[7:0]							
1AC	0x00	B3_ERRCNT_[7:0]							
1AD	0x00	B3_ERRCNT_[15:8]							
1AE	0x00	G1_ERRCNT_[7:0]							
1AF	0x00	G1_ERRCNT_[15:8]							

Table 45. Receive Side Register Address Map for ATM Provisioning and Monitoring

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FIFO and ATM Summary Masks (Read/Write)									
1C0	0x7E		RX_ATM_HEC_DROP_SECE_MASK	RX_ATM_HEC_CORR_SECE_MASK	RX_ATM_LCD_SECE_MASK	RX_ATM_OCD_SECE_MASK	RX_ATM_LCD_D_MASK	RX_ATM_OCD_D_MASK	
1C1									
ATM and Utopia Level 2 Provisioning									
1C2									
1C3	0x81	RX_ATM_LCD_TIME[5:0]						RX_ATM_HEC_UDF	RX_ATM_HEC_ENH
1C4	0x80	RX_ATM_IDLE_CLP	RX_ATM_IDLE_PTI_[2:0]			RX_ATM_IDLE_GFC[3:0]			
1C5	0x00	RX_ATM_IDLE_CAP			RX_ATM_IDLE_BYTE[5:0]				
1C6									
1C7									
Idle Cell Data Status (Read Only)									
1C8	0x00	RX_ATM_IDLE_DATA[7:0]							
1C9									
FIFO and ATM Delta, Event and Second Events (Read Only, Cleared by microprocessor)									
1CA	0x00		RX_ATM_HEC_DROP_SECE	RX_ATM_HEC_CORR_SECE	RX_ATM_LCD_SECE	RX_ATM_OCD_SECE	RX_ATM_LCD_D	RX_ATM_OCD_D	
1CB									
ATM Provisioning (Read/Write)									
1CC	0x00								RX_ATM_HEC_INH
ATM Status Bits (Read Only)									
1CD	0x06						RX_ATM_LCD	RX_ATM_OCD	
ATM Counters (Read Only)									
1D0	0x00	RX_ATM_HEC_CORR_[7:0]							
1D1	0x00	RX_ATM_HEC_CORR_[15:8]							
1D2	0x00	RX_ATM_HEC_DROP_[7:0]							
1D3	0x00	RX_ATM_HEC_DROP_[15:8]							
1D4	0x00	RX_ATM_CELL_CNT_[7:0]							
1D5	0x00	RX_ATM_CELL_CNT_[15:8]							
1D6	0x00				RX_ATM_CELL_CNT_[20:16]				

Table 46. Receive Side Register Address Map for FIFO Provisioning and Monitoring

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
System Interface Summary Masks (Read/Write)									
1E0	0x0C					RX_FIFOOVER_SECE_MASK	RX_FIFOOVER_E_MASK		
1E1									
System Interface Provisioning(Read/Write)									
1E2	0x30		RX_SYSINT_8BIT	RX_SYSINT_POLL	RX_SYSINT_GRPADD_INH		RX_PRTY_MODE		RX_CLAV_DSST
1E3									
1E4	0x0F				RX_FIFOEMPTY_RPA[4:0]				

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1E5	0x1D				RX_FIFOFULL_RPA[4:0]				
System Interface Event Bits (Read Only, cleared by uP)									
1E6	0x00					RX_FIFOOVER_SECE	RX_FIFOOVER_E		
1E7									
System Interface FIFO Error Counter (Read Only)									
1E8	0x00	RX_FIFOOVER_ERRCNT[7:0]							
1E9									

Table 47. Receive Side Register Address Map for POS Provisioning and Monitoring

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POS Summary Mask Bits (Read/Write)									
1F0	0x1F				RX_POS_FCS_ERR_SECE_MASK	RX_POS_PMIN_ERR_SECE_MASK	RX_POS_PMAX_ERR_SECE_MASK	RX_POS_PABORT_ERR_SECE_MASK	RX_POS_ADRCTL_INVALID_D_MASK
POS Provisioning(Read/Write)									
1F1	0x00				RX_POS_FCS_BIT_ORDR	RX_POS_PMIN[3:0]			
1F2	0xE0	RX_POS_PMAX[7:0]							
1F3	0x05	RX_POS_PMAX[15:8]							
1F4	0x50	RX_POS_FIFOUNDER_BYTE[7:0]							
POS Event and Second Event Bits (Read Only, Cleared by microprocessor)									
1F5	0x00				RX_POS_FCS_ERR_SECE	RX_POS_PMIN_ERR_SECE	RX_POS_PMAX_ERR_SECE	RX_POS_PABORT_ERR_SECE	RX_POS_ADRCTL_INVALID_D
POS Provisioning(Read/Write)									
1F6	0x00		RX_POS_FIFOUNDR_MODE	RX_POS_PMIN_ENB	RX_POS_PMAX_ENB		RX_POS_FCS_INH	RX_POS_FCS_MODE	RX_POS_ADRCTL_DROP_INH
POS Status (Read Only)									
1F7	0x00								RX_POS_ADRCTL_INVALID
POS Errored Packet Counters (Read Only)									
1F8	0x00	RX_POS_PABORT_ERRCNT[7:0]							
1F9									
1FA	0x00	RX_POS_PMAX_ERRCNT[7:0]							
1FB	0x00	RX_POS_PMIN_ERRCNT[7:0]							
1FC	0x00	RX_POS_FCS_ERRCNT[7:0]							
1FD	0x00	RX_POS_FCS_ERRCNT[15:8]							
1FE	0x00					RX_POS_FCS_ERRCNT[19:16]			

Table 48. .Device Identification Code

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Device Identification Code (Read Only)									
1FF	0x01	DEV_ID[7:0]							

12.0 Absolute Maximum Ratings

Table 49. Absolute Maximum Ratings

Description	Performance
Power Supply Voltage (V_{DD})	-0.3V to +3.9V
3.3V Input Voltage	-1.0V to V_{DD}+0.3V
5V Input Voltage	-0.5V to 6.0V
Lead Temperature	+300° C
Junction Temperature	+150° C
Power Dissipation	1.1W (Max) / 0.8W (Typ)
Storage Temperature	-55° to 135° C
Operating Temperature	-40° to 85° C

13.0 DC Electrical Characteristics

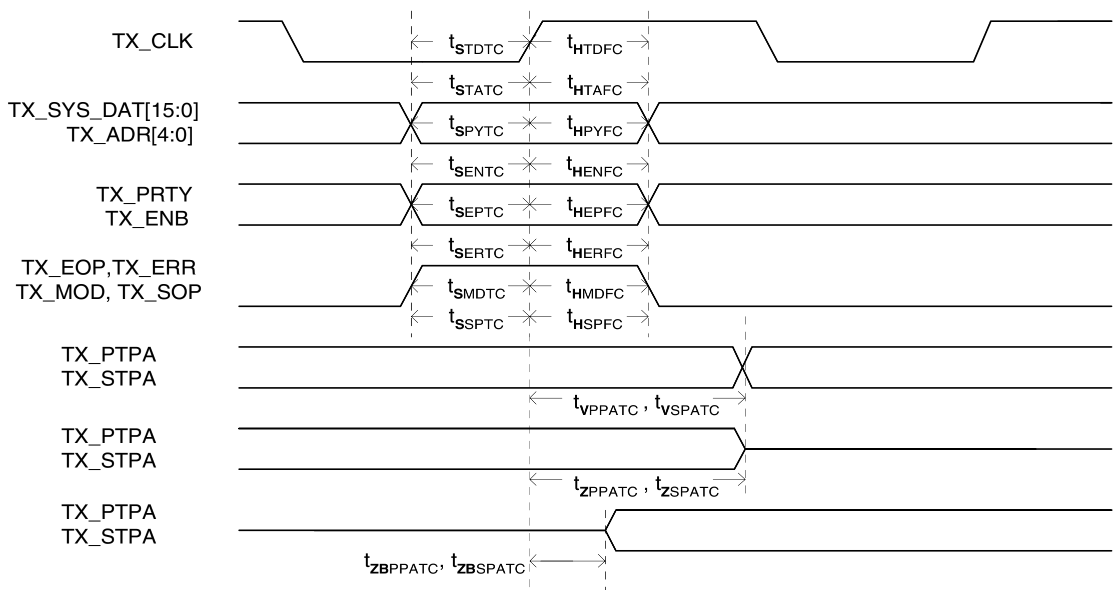
Typical Conditions: T_C = 25C, V_{DD} = 3.3V

Table 50. 3.3V DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Conditions
V_{IH}	Input High Voltage	V_{DD}-1.2V			Guaranteed Input High Voltage
V_{IL}	Input Low Voltage			V_{DD}-1.4V	Guaranteed Input Low Voltage
I_{IH}	Input High Current	-10uA	0	+10uA	$V_{IH} = V_{DD}$
I_{IL}	Input Low Current	-10uA	0	+10uA	V_{IL} = GND
V_{OH}	Output Voltage High	V_{DD}-1.0V			
V_{OL}	Output Voltage Low			V_{DD}-1.6V	

14.0 AC Electrical Characteristics

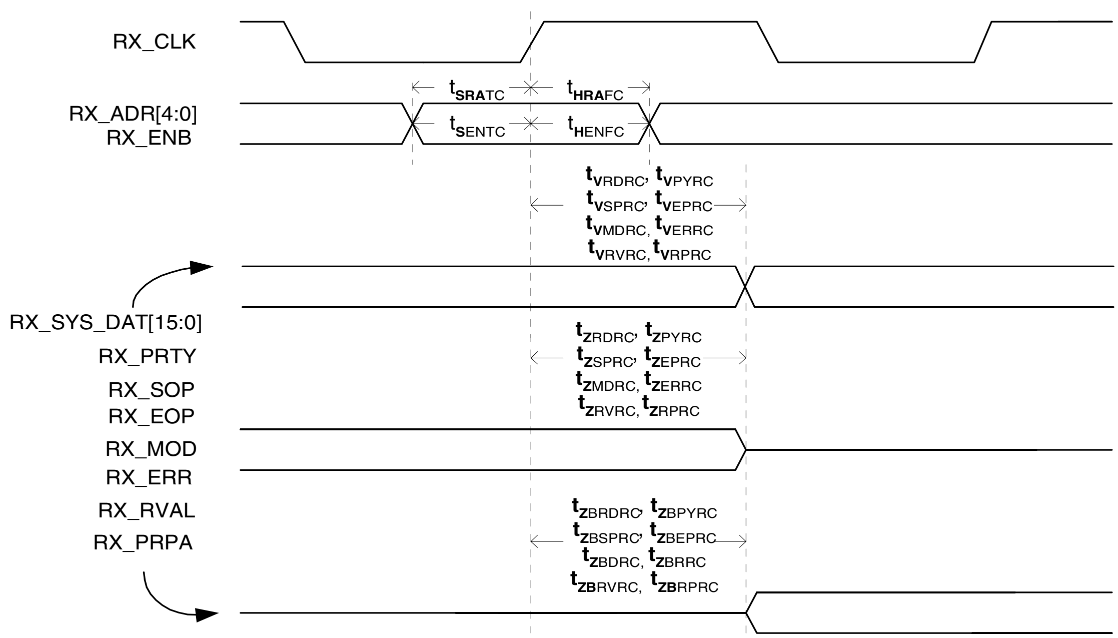
14.1 Transmit Timing (POS Mode)



Label	Parameter	Min	Max	Units
TX_CLK	TX_CLK frequency		50	MHz
t_{STDTC}	Setup TX_SYS_DAT to TX_CLK high	3		ns
t_{HTDFC}	Hold TX_SYS_DAT from TX_CLK high	0		ns
t_{STATC}	Setup TX_ADR to TX_CLK high	3		ns
t_{HTAFC}	Hold TX_ADR from TX_CLK high	0		ns
t_{SPYTC}	Setup TX_PRTY to TX_CLK high	3		ns
t_{HPYFC}	Hold TX_PRTY from TX_CLK high	0		ns
t_{SENTC}	Setup TX_ENB to TX_CLK high	3		ns
t_{HENFC}	Hold TX_ENB from TX_CLK high	0		ns
t_{SEPTC}	Setup TX_EOP to TX_CLK high	3		ns
t_{HEPFC}	Hold TX_EOP from TX_CLK high	0		ns
t_{SERTC}	Setup TX_ERR to TX_CLK high	3		ns
t_{HERFC}	Hold TX_ERR from TX_CLK high	0		ns
t_{SMDTC}	Setup TX_MOD to TX_CLK high	3		ns
t_{HMDFC}	Hold TX_MOD from TX_CLK high	0		ns
t_{SSPTC}	Setup TX_SOP to TX_CLK high	3		ns
t_{HSPFC}	Hold TX_SOP from TX_CLK high	0		ns

Label	Parameter	Min	Max	Units
t_{VPPATC},t_{VSPATC}	TX_PTPA, TX_STPA valid from TX_CLK high	1	12	ns
t_{ZPPATC},t_{ZSPATC}	TX_PTPA, TX_STPA tri-state from TX_CLK high	1	10	ns
t_{ZBPPAT},$t_{ZBSPATC}$	TX_PTPA, TX_STPA driven from TX_CLK high	0	3	ns

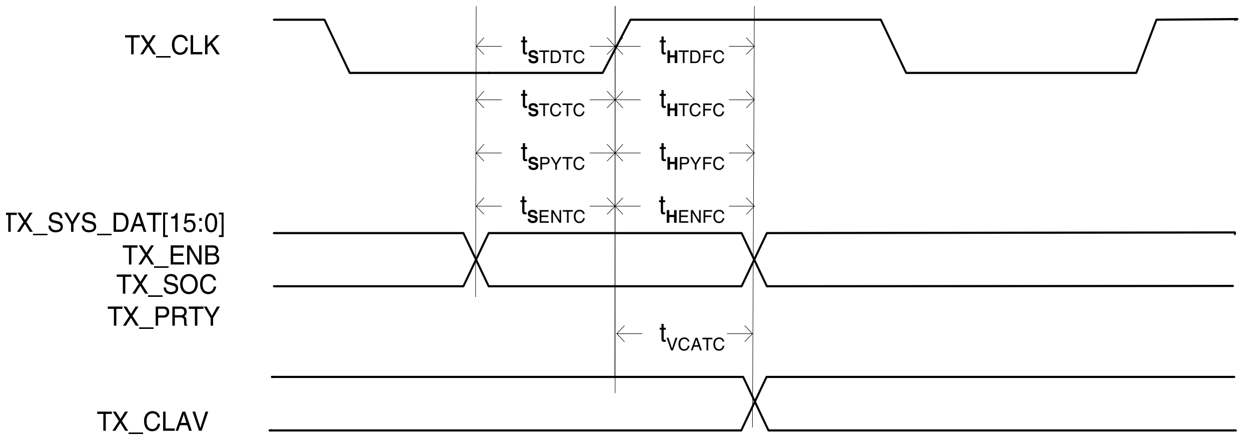
14.2 Receive Timing (POS Mode)



Label	Parameter	Min	Max	Units
RX_CLK	RX_CLK frequency		50	MHz
t_{SRATC}	Setup RX_ADR to RX_CLK high	3		ns
t_{HRAFC}	Hold RX_ADR from RX_CLK high	0		ns
t_{SENTC}	Setup RX_ENB to RX_CLK high	3		ns
t_{HENFC}	Hold RX_ENB from RX_CLK high	0		ns
t_{VRDRC}	RX_SYS_DAT valid from RX_CLK high	1	12	ns
t_{ZRDRC}	RX_SYS_DAT tri-state from RX_CLK high	1	10	ns
t_{ZBRDRC}	RX_SYS_DAT driven from RX_CLK high	0	3	ns
t_{VPYRC}	RX_PRTY valid from RX_CLK high	1	12	ns
t_{ZPYRC}	RX_PRTY tri-state from RX_CLK high	1	10	ns
t_{ZBPYRC}	RX_PRTY driven from RX_CLK high	0	3	ns
t_{VSPRC}	RX_SOP valid from RX_CLK high	1	12	ns
t_{ZSPRC}	RX_SOP tri-state from RX_CLK high	1	10	ns

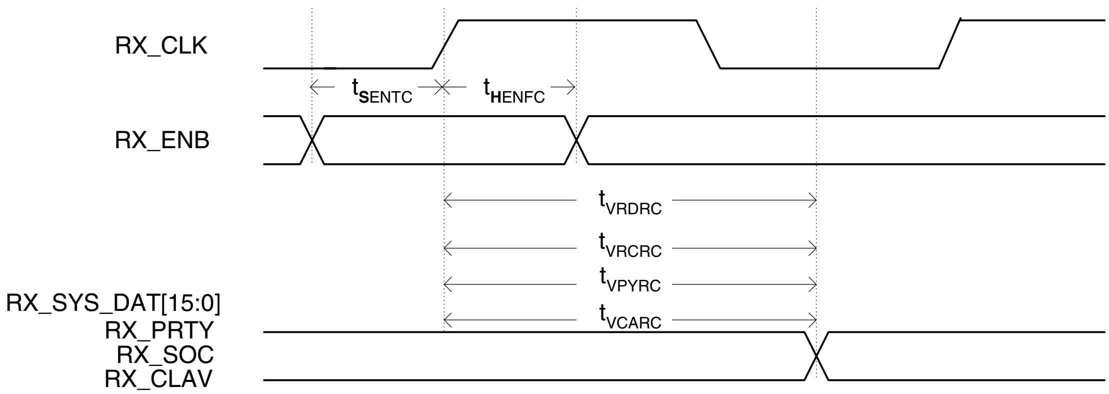
Label	Parameter	Min	Max	Units
t_{ZBSPRC}	RX_SOP driven from RX_CLK high	0	3	ns
t_{VEPRC}	RX_EOP valid from RX_CLK high	1	12	ns
t_{ZEPRC}	RX_EOP tri-state from RX_CLK high	1	10	ns
t_{ZBEPRC}	RX_EOP driven from RX_CLK high	0	3	ns
t_{VMDRC}	RX_MOD valid from RX_CLK high	1	12	ns
t_{ZMDRC}	RX_MOD tri-state from RX_CLK high	1	10	ns
t_{ZBMDRC}	RX_MOD driven from RX_CLK high	0	3	ns
t_{VERRC}	RX_ERR valid from RX_CLK high	1	12	ns
t_{ZERRC}	RX_ERR tri-state from RX_CLK high	1	10	ns
t_{ZBERRC}	RX_ERR driven from RX_CLK high	0	3	ns
t_{VRVRC}	RX_RVAL valid from RX_CLK high	1	12	ns
t_{ZRVRC}	RX_RVAL tri-state from RX_CLK high	1	10	ns
t_{ZBRVRC}	RX_RVAL driven from RX_CLK high	0	3	ns
t_{VRPRC}	RX_PRPA valid from RX_CLK high	1	12	ns
t_{ZRPRC}	RX_PRPA tri-state from RX_CLK high	1	10	ns
t_{ZBRPRC}	RX_PRPA driven from RX_CLK high	0	3	ns

14.3 Transmit Timing (UTOPIA Mode, single-PHY)



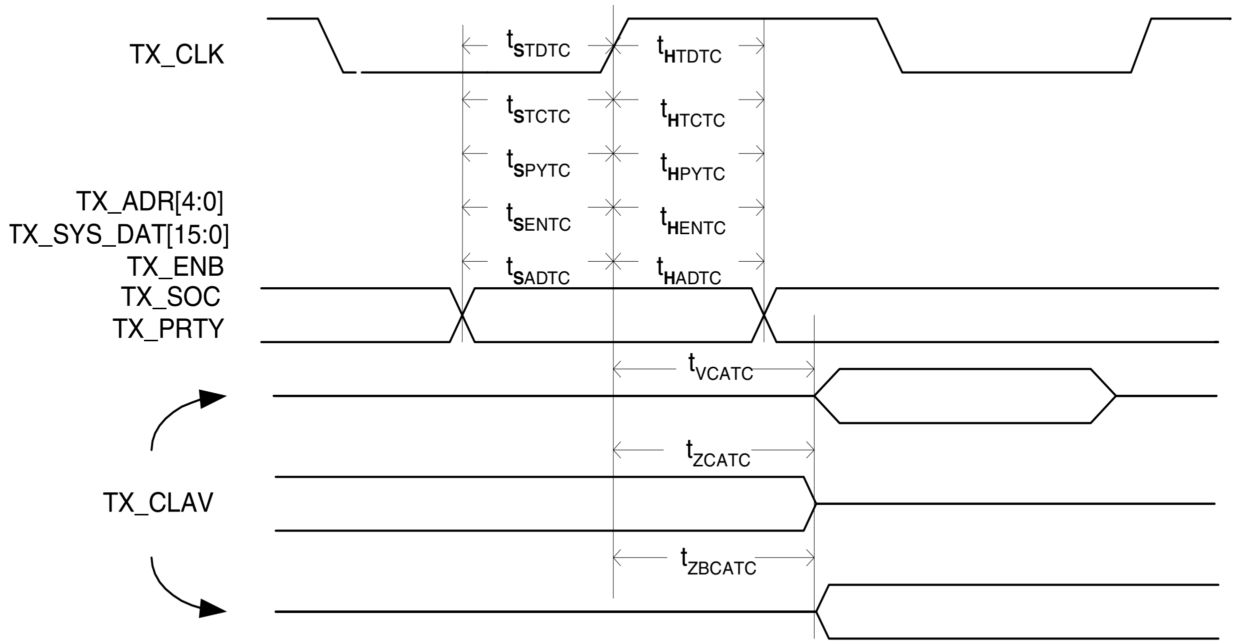
Label	Parameter	Min	Max	Units
TX_CLK	TX_CLK frequency		50	MHz
t_{STDTC}	Setup TX_SYS_DAT to TX_CLK high	3		ns
t_{HTDTC}	Hold TX_SYS_DAT from TX_CLK high	0		ns
t_{SPYTC}	Setup TX_PRTY to TX_CLK high	3		ns
t_{HPYTC}	Hold TX_PRTY from TX_CLK high	0		ns
t_{SENTC}	Setup TX_ENB to TX_CLK high	3		ns
t_{HENTC}	Hold TX_ENB from TX_CLK high	0		ns
t_{STCTC}	Setup TX_SOC to TX_CLK high	3		ns
t_{HTCTC}	Hold TX_SOC from TX_CLK high	0		ns
t_{SCAFC}	TX_CLAV valid from TX_CLK high	1	12	ns

14.4 Receive Timing (UTOPIA Mode, single-PHY)



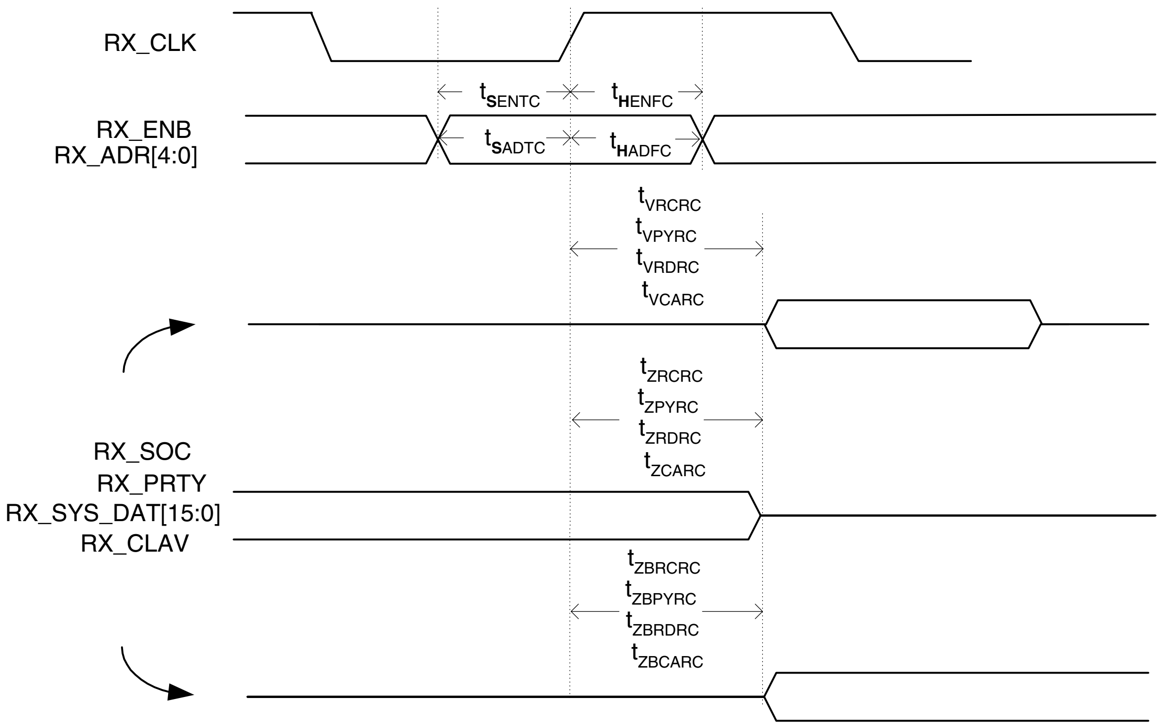
Label	Parameter	Min	Max	Units
RX_CLK	RX_CLK frequency		50	MHz
t_{SENRC}	Setup RX_ENB to RX_CLK high	3		ns
t_{HENRC}	Hold RX_ENB from RX_CLK high	0		ns
t_{VRDRC}	RX_SYS_DAT valid from RX_CLK high	1	12	ns
t_{VRCRC}	RX_SOC valid from RX_CLK high	1	12	ns
t_{VPYRC}	RX_PRTY valid from RX_CLK high	1	12	ns
t_{VCARC}	RX_CLAV valid from RX_CLK high	1	12	ns

14.5 Transmit Timing (UTOPIA Mode, multi-PHY)



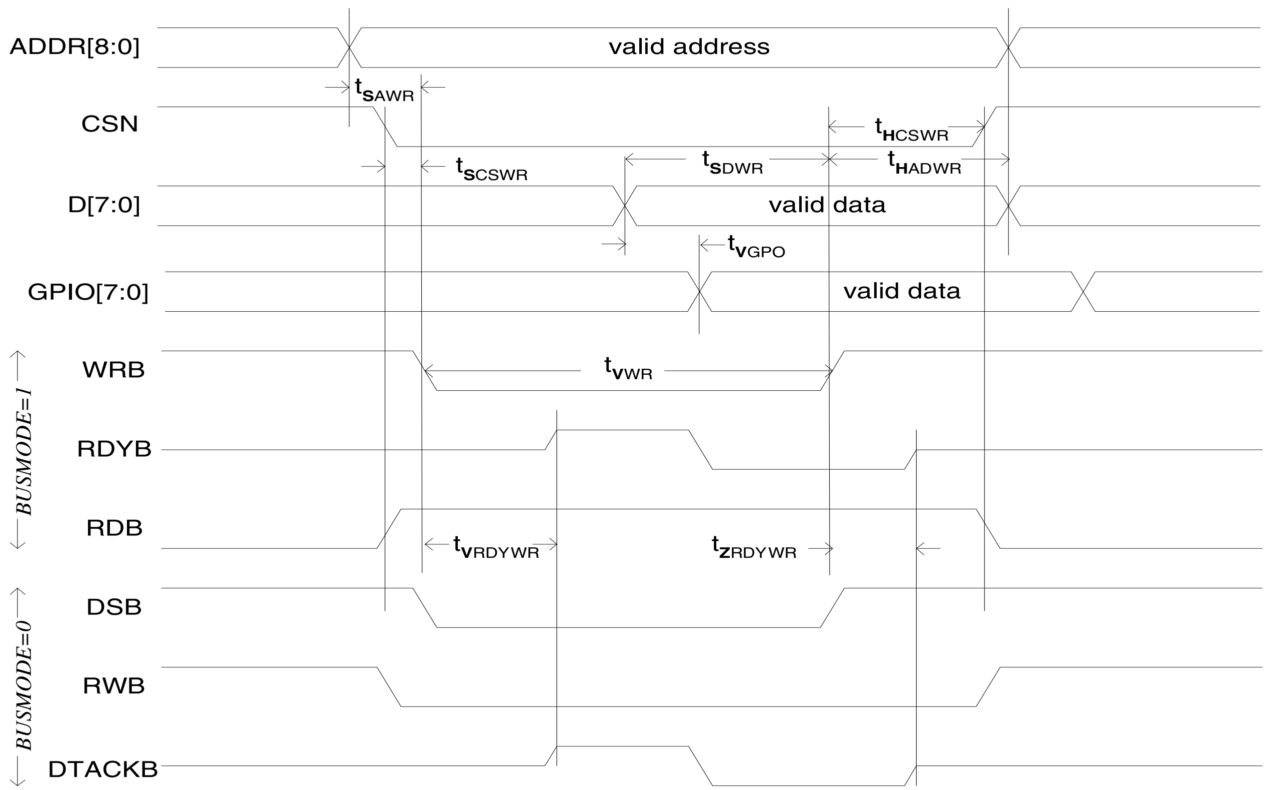
Label	Parameter	Min	Max	Units
TX_CLK	TX_CLK frequency		50	MHz
t_{STDTC}	Setup TX_SYS_DAT to TX_CLK high	3		ns
t_{HTDTC}	Hold TX_SYS_DAT from TX_CLK high	0		ns
t_{SPYTC}	Setup TX_PRTY to TX_CLK high	3		ns
t_{HPYTC}	Hold TX_PRTY from TX_CLK high	0		ns
t_{SENTC}	Setup TX_ENB to TX_CLK high	3		ns
t_{HENTC}	Hold TX_ENB from TX_CLK high	0		ns
t_{STCTC}	Setup TX_SOC to TX_CLK high	3		ns
t_{HTCTC}	Hold TX_SOC from TX_CLK high	0		ns
t_{SADTC}	Setup TX_ADR to TX_CLK high	3		ns
t_{HADTC}	Hold TX_ADR from TX_CLK high	0		ns
t_{ZCATC}	TX_CLAV valid from TX_CLK high	1	12	ns
t_{ZCATC}	TX_CLAV tri-state from TX_CLK high	1	12	ns
t_{ZBCATC}	TX_CLAV driven from TX_CLK high	0	3	ns

14.6 Receive Timing (UTOPIA Mode, multi-PHY)



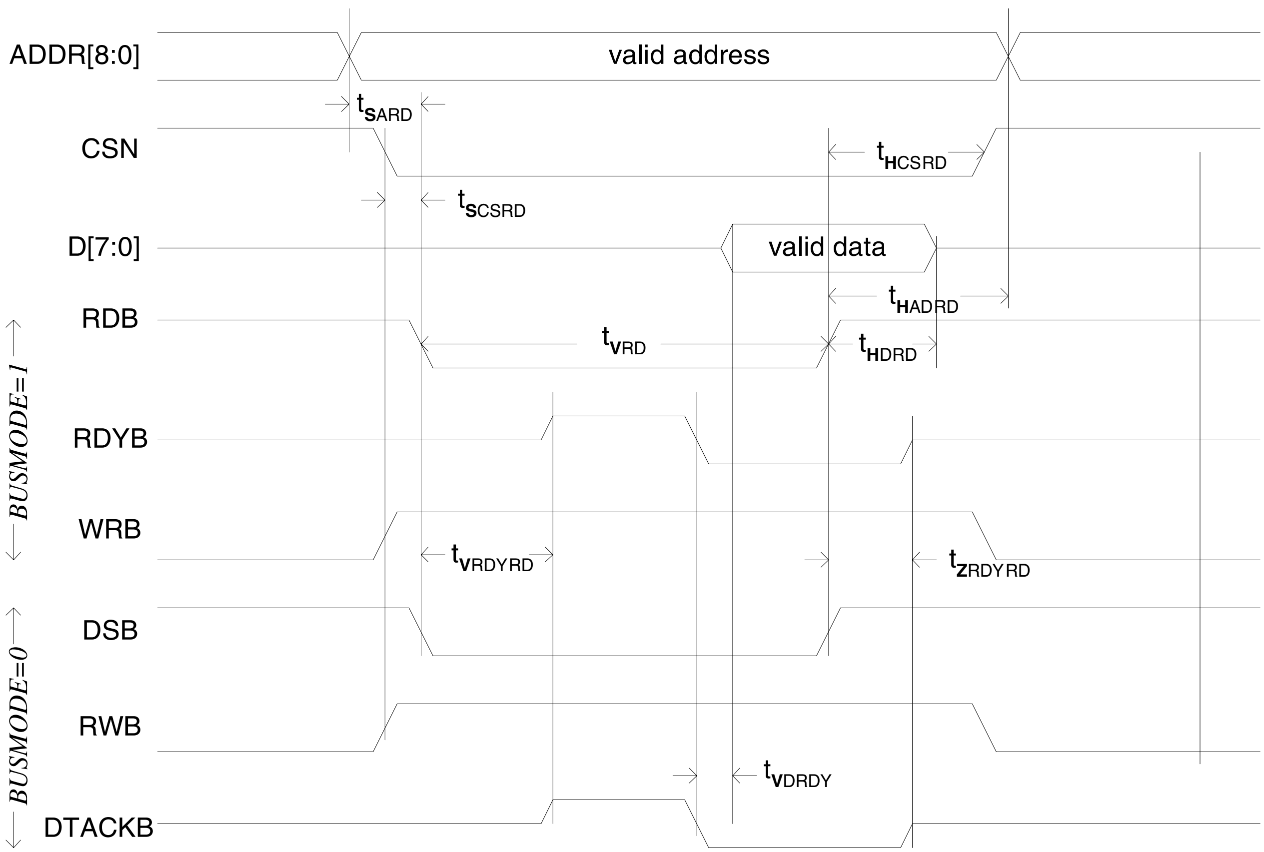
Label	Parameter	Min	Max	Units
RX_CLK	RX_CLK frequency		50	MHz
t_{SENRC}	Setup RX_ENB to RX_CLK high	3		ns
t_{HENRC}	Hold RX_ENB from RX_CLK high	0		ns
t_{SADRC}	Setup RX_ADR to RX_CLK high	3		ns
t_{HADRC}	Hold RX_ADR from RX_CLK high	0		ns
t_{VRDRC}	RX_SYS_DAT valid from RX_CLK high	1	12	ns
t_{ZRDRC}	RX_SYS_DAT tri-state from RX_CLK high	1	12	ns
t_{ZBRDRC}	RX_SYS_DAT driven from RX_CLK high	1	12	ns
t_{VPYRC}	RX_PRTY valid from RX_CLK high	1	12	ns
t_{ZPYRC}	RX_PRTY tri-state from RX_CLK high	1	12	ns
t_{ZBPYRC}	RX_PRTY driven from RX_CLK high	1	12	ns
t_{VRCRC}	RX_SOC valid from RX_CLK high	1	12	ns
t_{ZRCRC}	RX_SOC tri-state from RX_CLK high	1	12	ns
t_{ZBRCRC}	RX_SOC driven from RX_CLK high	1	12	ns
t_{VCARC}	RX_CLAV valid from RX_CLK high	1	12	ns
t_{ZCARC}	RX_CLAV tri-state from RX_CLK high	1	12	ns
t_{ZBCARC}	RX_CLAV driven from RX_CLK high	0	3	ns

14.7 Microprocessor Interface Write Timing



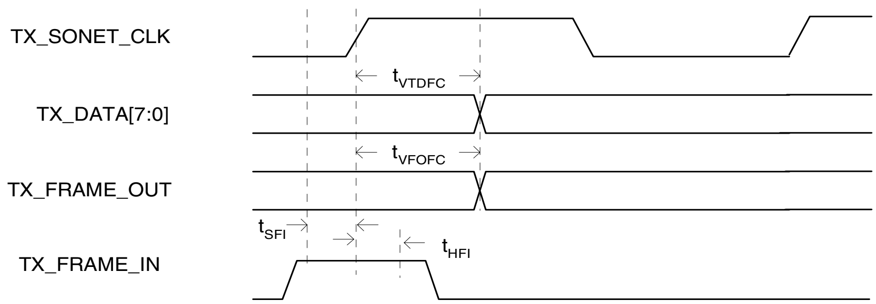
Label	Parameter	Min	Max	Units
t_{SAWR}	Setup addr to write (WRB,DSB) assert	10		ns
t_{SCSWR}	Setup chip select (CSN,RWB) to write (WRB,DSB) assert	5		ns
t_{VWR}	Valid write (WRB,DSB) pulse width	50		ns
t_{SDWR}	Setup data to write (WRB,DSB) deassert	15		ns
t_{HADWR}	Hold addr/data from write (WRB,DSB) deassert	4		ns
t_{VRDYWR}	Valid RDYB,DTACKB from write (WRB,DSB) assert	0	15	ns
t_{ZRDYWR}	Tri-state RDYB,DTACKB from write (WRB,DSB) deassert	0	10	ns
t_{HCSWR}	Hold chip select (CSB,RWB) from write (WRB,DSB) deassert	0		ns
t_{VGPO}	GPIO output valid after D[7:0] written	0	8	ns

14.8 Microprocessor Interface Read Timing



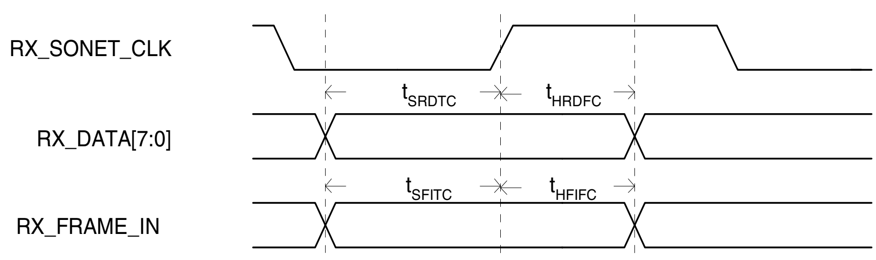
Label	Parameter	Min	Max	Units
t_{SARD}	Setup addr to read (RDB,DSB) assert	10		ns
t_{SCSRD}	Setup chip select (CSN,RWB) to read (RDB,DSB) assert	5		ns
t_{VRD}	Valid read (RDB,DSB) pulse width	50		ns
t_{VDRDY}	Valid data from RDYB/DTACKB assert		10	ns
t_{HADRD}	Hold addr from read (RDB,DSB) deassert	4		ns
t_{VRDYRD}	Valid RDYB,DTACKB from read (RDB,DSB) assert		15	ns
t_{ZRDYRD}	Tri-state RDYB,DTACKB from read (RDB,DSB) deassert	10		ns
t_{HDRD}	Hold data from read (RDB,DSB) deassert	15		ns

14.9 Line Interface Transmit Timing



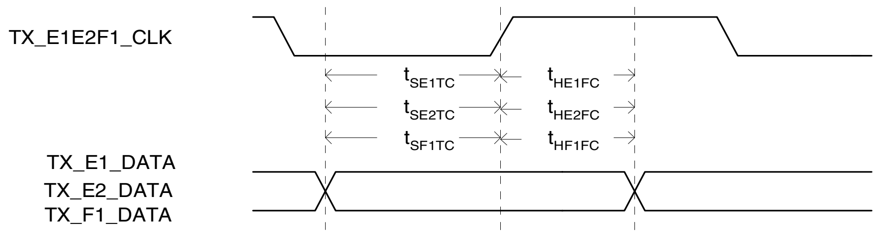
Label	Parameter	Min	Max	Units
TX_SONETCLK	TX_SONETCLK frequency		77.76	MHz
t_{VTDFC}	TX_DATA valid from TX_CLK high	1	5	ns
t_{VFOFC}	TX_FRAME_OUT valid from TX_CLK high	1	5	ns
t_{SFI}	Setup TX_FRAME_IN to TX_SONETCLK high	3		ns
t_{HFI}	Hold TX_FRAME_IN from TX_SONETCLK high	1		ns

14.10 Line Interface Receive Timing



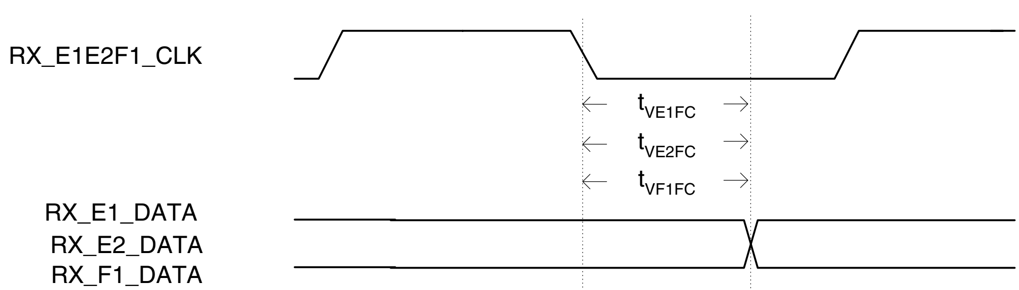
Label	Parameter	Min	Max	Units
RX_SONETCLK	RX_SONETCLK frequency		77.76	MHz
t_{SRDTC}	Setup RX_DATA to RX_CLK high	3		ns
t_{HRDFC}	Hold RX_DATA from RX_CLK high	0		ns
t_{SFITC}	Setup RX_FRAME_IN to RX_CLK high	3		ns
t_{HFIFC}	Hold RX_FRAME_IN from RX_CLK high	0		ns

14.11 TOH Interface E1/E2/E3 Transmit Timing



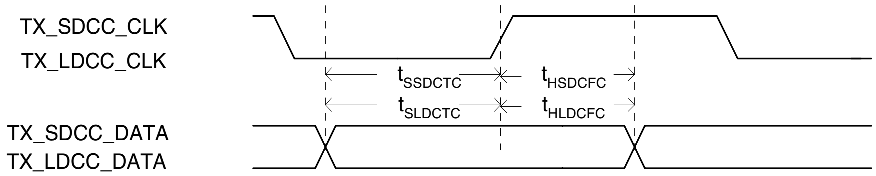
Label	Parameter	Min	Max	Units
TX_E1E2F1_CLK	TX_E1E2F1_CLK frequency		64	kHz
t_{SE1TC}	Setup TX_E1_DATA to TX_E1E2F1_CLK high	100		ns
t_{HE1FC}	Hold TX_E1_DATA from TX_E1E2F1_CLK high	100		ns
t_{SE2TC}	Setup TX_E2_DATA to TX_E1E2F1_CLK high	100		ns
t_{HE2FC}	Hold TX_E2_DATA from TX_E1E2F1_CLK high	100		ns
t_{SF1TC}	Setup TX_F1_DATA to TX_E1E2F1_CLK high	100		ns
t_{HF1FC}	Hold TX_F1_DATA from TX_E1E2F1_CLK high	100		ns

14.12 TOH Interface E1/E2/E3 Receive Timing



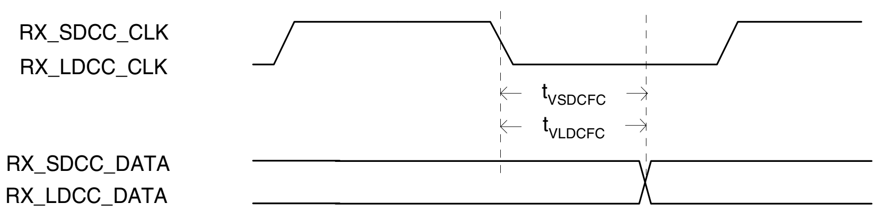
Label	Parameter	Min	Max	Units
TX_E1E2F1_CLK	TX_E1E2F1_CLK frequency		64	kHz
t_{VE1FC}	Valid RX_E1_DATA from RX_E1E2F1_CLK low	-5	25	ns
t_{HE2FC}	Valid RX_E2_DATA from RX_E1E2F1_CLK low	-5	25	ns
t_{HF1FC}	Valid RX_F1_DATA from RX_E1E2F1_CLK low	-5	25	ns

14.13 DCC Interface Transmit Timing



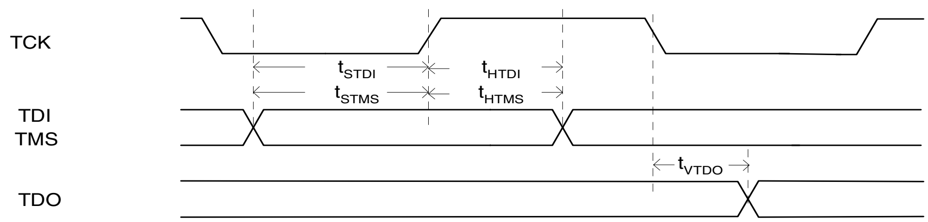
Label	Parameter	Min	Max	Units
TX_SDCC_CLK	TX_SDCC_CLK frequency		192	kHz
t_{SSDCTC}	Setup TX_SDCC_DATA to TX_SDCC_CLK high	100		ns
t_{HSDFC}	Hold TX_SDCC_DATA from TX_SDCC_CLK high	100		ns
TX_LDCC_CLK	TX_LDCC_CLK frequency		576	kHz
t_{SLDCTC}	Setup TX_LDCC_DATA to TX_LDCC_CLK high	100		ns
t_{HLDFC}	Hold TX_LDCC_DATA from TX_LDCC_CLK high	100		ns

14.14 DCC Interface Transmit Timing



Label	Parameter	Min	Max	Units
RX_SDCC_CLK	RX_SDCC_CLK frequency		192	kHz
t_{VSDCFC}	Valid RX_SDCC_DATA from RX_SDCC_CLK low	-5	25	ns
RX_LDCC_CLK	RX_LDCC_CLK frequency		576	kHz
t_{SLDCTC}	Valid RX_LDCC_DATA from RX_LDCC_CLK low	-5	25	ns

14.15 JTAG Interface Timing



Label	Parameter	Min	Max	Units
TCK	TCK frequency		1	MHz
t_{STDI}	Setup TDI to TCK high	50		ns
t_{HTDI}	Hold TDI from TCK high	50		ns
t_{STMS}	Setup TMS to TCK high	50		ns
t_{HTMS}	Hold TMS from TCK high	50		ns
t_{HTDO}	TDO valid from TCK low	2	50	ns

15.0 Index of Registers

KEY:

In this index, primary entries are registers that appear in text and include a definition of the register. Secondary (indented) registers in this index refer to registers in the Memory Map tables.

A

B

C

D

E

F

G

J

K

L

S

T

The information contained in this document is *Device Specification Information* and is about a product in its fully tested and characterized phase. All features described herein are supported. Contact AMCC for updates to this document and the latest product status.

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