
DECchip 21050 Specifications

This chapter describes the mechanical and electrical specifications of the 21050.

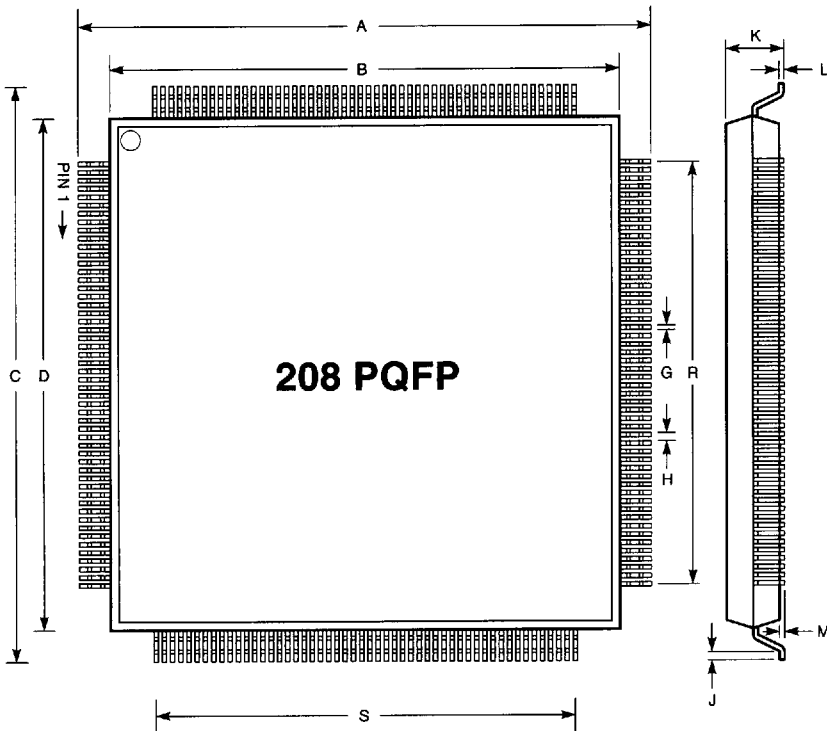
7.1 Mechanical Specifications

The following sections describe the mechanical specifications of the 21050.

7.1.1 DECchip 21050 Package

The DECchip 21050 PCI chip is packaged in a 208-pin PQFP. Figure 7-1 shows the DECchip 21050 package dimensions.

Figure 7-1 Package Dimensions



DIM	Millimeters	
	MIN	MAX
A	30.6 BSC	
B	28.0 BSC	
C	30.6 BSC	
D	28.0 BSC	
G	0.17	0.27
H	0.5 BSC	
J	0.45	0.75
K	--	4.2
L	0.12	0.20
M	0.25	--
R	26.75 BSC	
S	26.75 BSC	

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7.1.2 Absolute Maximum Ratings

This section lists the absolute maximum ratings.

V_{DD}	5.0 V $\pm 5\%$
T_J	100°C
T_A	40°C
P_{WC}	1.7W
Storage temperature	-55°C to 125°C

7.2 Electrical Specifications

The following sections describe the electrical specifications of the 21050.

7.2.1 Interface Signal DC Electrical Specifications

Table 7-1 defines the dc parameters met by all 21050 signals.

Table 7-1 DC Specifications

Symbol	Parameter	Condition	Minimum	Maximum	Units
V_{ih}	Input high voltage	—	2.0	$V_{DD} + 0.5$ V	V
V_{il}	Input low voltage	—	-0.5	0.8	V
I_{ih}	Input high leakage current ¹	$V_{in} = 2.7$ V	—	70	μ A
I_{il}	Input low leakage current ¹	$V_{in} = 0.5$ V	—	-70	μ A
V_{oh}	Output high voltage	$I_{out} = -2$ mA	2.4	—	V
V_{ol}	Output low voltage ²	$I_{out} = 3$ mA, 6 mA	—	0.55	V
C_{in}	Input pin capacitance	—	—	10	pF
C_{IDSEL}	p_idsel pin capacitance	—	—	8	pF
C_{clk}	p_clk, s_clk pin capacitance	—	5	12	pF

Footnotes:

1. Input high leakage current and input low leakage current include I_{ozl} or I_{ozh} leakage current for bidirectional signals.

2. Most output low voltage signals have 3 mA current. The following output low voltage signals have 6 mA low output current:

p_frame_l	p_trdy_l	p_irdy_l	p_devsel_l
p_stop_l	p_serr_l	p_perr_l	p_lock_l
s_frame_l	s_trdy_l	s_irdy	s_devsel_l
s_stop_l	s_perr_l	s_lock_l	

7.3 Interface Signal AC Electrical Specifications

Table 7–2 Shared Signal Output Parameters

Symbol	Parameter	Condition	Min.	Max.	Units
I_{oh} (AC)	Switching current high ¹	$0 < V_{out} \leq 1.4$	-44	–	μA
		$1.4 < V_{out} \leq 2.4$	2	3	μA
	Test point	$V_{out} = 3.1 \text{ V}$	–	-142	μA
I_{ol} (AC)	Switching current low ¹	$V_{out} \geq 2.2$	95	–	μA
		$2.2 > V_{out} > 0.55$	$V_{out} / 0.023$	4	μA
	Test point	$V_{out} = 0.71 \text{ V}$	–	206	μA
I_{cl}	Low clamp current	$-5 < V_{in} \leq -1$	5	–	μA
t_r	Unloaded output rise time	0.4 V to 2.4 V	1	–	V/ns
t_f	Unloaded output fall time	0.4 V to 2.4 V	1	–	V/ns

Footnotes:

1. See V/I curves in the *PCI Specification*.
2. $-44 + (V_{out} - 1.4)/0.024$

3. $11.9 * (V_{out} - 5.25) * (V_{out} + 2.45)$ for $V_{DD} > V_{out} > 3.1$ V
4. $78.5 * (V_{out} * (4.4 - V_{out}))$ for 0 V $< V_{out} < 0.71$ V
5. $-25 + (V_{in} + 1) / 0.015$

7.3.1 Interface Signal AC Timing Specifications

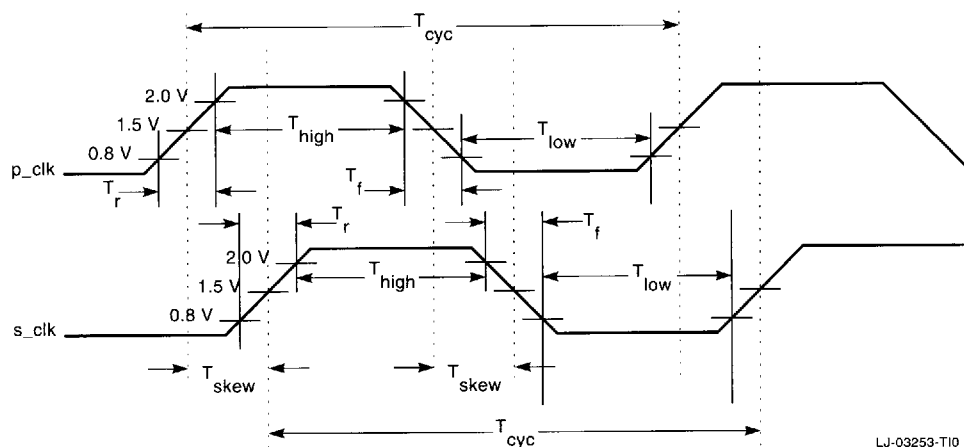
Table 7–3 and Figure 7–2 show the **p_clk** and **s_clk** ac timing.

Table 7–3 p_clk and s_clk AC Timing

Symbol	Parameter	Minimum	Maximum	Units	Notes
T_{cyc}	xclk cycle time	30	–	ns	–
T_{high}	xclk high time	12	–	ns	@1.5 V and @1 V/ns
T_{low}	xclk low time	12	–	ns	@1.5 V and @1 V/ns
	Slew rate	1	4	V/ns	0.4 to 2.4 V
T_{skew}	Delay from p_clk to s_clk	0	7	ns	@ 1.5 V
T_{sclk_r}	p_clk rising to s_clk_ o<6:0> rising	0	5	ns	@1.5 V ¹
T_{sclk_f}	p_clk falling to s_clk_ o<6:0> falling	0	5	ns	@1.5 V ¹

¹Measured with 30 pF lumped load.

Figure 7–2 p_clk and s_clk AC Timing



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7.3.2 Input Signal AC Timing Specifications

Table 7–4 and Figure 7–3 show the input signal ac timings.

Table 7–4 Input Signal AC Timings

Symbol	Parameter	Minimum	Maximum	Units
T_{val}	xclk -to- xsignal valid delay— bused signals ^{1, 2, 3}	2	11	ns
T_{val} (ptp)	xclk - to- xsignal valid delay— point-to-point ^{1, 2, 3}	2	12	ns
T_{on}	Float-to-active delay ¹	2	—	ns
T_{off}	Active-to-float delay ¹	—	28	ns

¹All primary interface signals are used by **p_clk** and all secondary interface signals are used by **s_clk**.

²Minimum times measured with 0-pF equivalent load. Maximum times measured with 50-pF equivalent load.

³Point-to-point signals are **p_req_l**, **s_req_l**<7:0>, **p_gnt_l**, **s_gnt_l**<7:0>, **s_dispst_l**, **s_bufne_l**, and **s_cfn_l**.

All other PCI signals are shared.

All **xgnt_l** signals, **s_dispst_l**, and **s_cfn_l** have a setup time of 10 ns.

xreq_l has a setup time of 12 ns.

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Table 7–4 (Cont.) Input Signal AC Timings

Symbol	Parameter	Minimum	Maximum	Units
T_{su}	Input setup time to $xclk$ — based signals ^{1, 3}	7	—	ns
T_{su} (ptp)	Input setup time to $xclk$ — point-to-point ^{1, 3}	10, 12	—	ns
T_h	Input signal hold time from $xclk$ ¹	0	—	ns

¹All primary interface signals are used by p_clk and all secondary interface signals are used by s_clk .

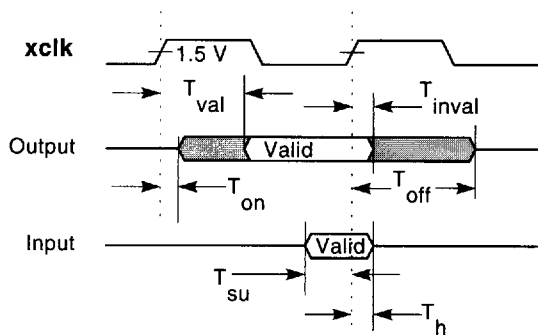
³Point-to-point signals are p_req_l , $s_req_l<7:0>$, p_gnt_l , $s_gnt_l<7:0>$, s_dispst_l , s_bufne_l , and s_cfn_l .

All other PCI signals are shared.

All $xgnt_l$ signals, s_dispst_l , and s_cfn_l have a setup time of 10 ns.

$xreq_l$ has a setup time of 12 ns.

Figure 7–3 AC Timing Waveforms



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Table 7–5 shows the timing specifications for **xrst_l**.

Table 7–5 xrst_l Timing Specifications

Symbol	Parameter	Minimum	Maximum	Units
T_{prst}	p_rst_l active time after power stable	1	–	μS
$T_{prst-clk}$	p_rst_l active time after p_clk stable	100	–	μS
$T_{prst-off}$	p_rst_l active to output float delay	–	40	ns
T_{rst}	s_rst_l active after p_rst_l assertion	–	40	ns
T_{rst-on}	s_rst_l active time after s_clk stable	100	–	μS
$T_{rst-off}$	s_rst_l active to secondary output float delay	–	40	ns