TMC2311
CMOS Fast Cosine Transform Processor
12 Bits, 15 Million Pixels Per Second

Description

The TMC2311, a high-speed algorithm specific processor, computes the one or two dimensional forward discrete cosine transform (DCT) of an 8 or 8x8 point array of contiguous 9-bit data or the inverse DCT of 12-bit data. Output precision in all cases in 12 bits. It complies with the CCITT Specialists' Group on Visual Telephony (SG XV) accuracy specification for inverse DCT. With its internal coefficient TOM, data transpose RAM, address generators, and sequencer, the TMC2311 accepts high level instructions from a host processor and raw 8x8 blocked data from an external memory and returns transformed data to a second external memory. The TMC2311 also includes a defeatable adder-subtractor for linear predictive coding and differential pulse code modulation. The pipelined TMC2311 can transform continuous 8x8 pixel data blocks at a rate of one per 4.48 µs.

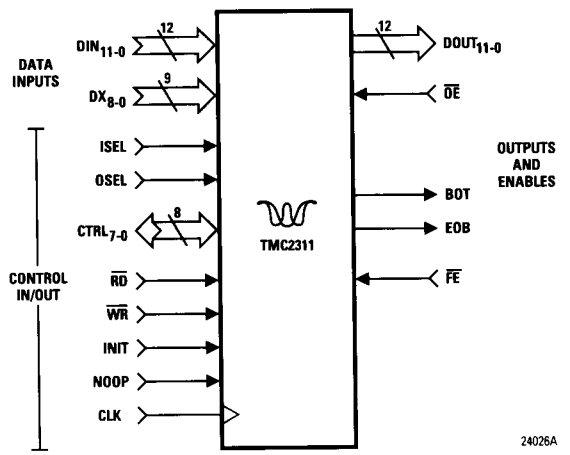
Operating under a system clock of up to 30 MHz, the TMC2311 accepts each incoming data block in row-major ("line-by-line") format at two clock cycles per pixel. Output data are written in column-major format, i.e., down the left-most column of the block, then down the next column to the right, etc., also at two clock cycles per pixel. In the inverse DCT mode, the chip accepts column-major data and returns row-major data. Thus, a pair of TMC2311 chips can transform an image and return it to its original spatial domain, with or without any intervening operation, such as compression, transmission and re-expansion.

Built with a one-micron double level metal OMICRON-C™ low-power CMOS process, the TMC2311 is available in a 68-lead plastic chip carrier.

Features

- Stand alone execution of 8-point forward or inverse cosine transform
- Continuous 8x8-point 2-D DCTs every 4.48 µs including memory transpose and data loading/ unloading
- On-chip cosine coefficient ROM
- On-chip data transpose memory with direct transpose mode
- Auxiliary adder with optional clipped outputs for linear predictive coding and differential pulse code modulation
- Two's complement 12-bit data I/O format
- Two's complement 9-bit add/subtract input
- Full CCITT SGXV compatibility
- All inputs and outputs TTL compatible
- 68 pin Plastic Chip Carrier

Logic Symbol



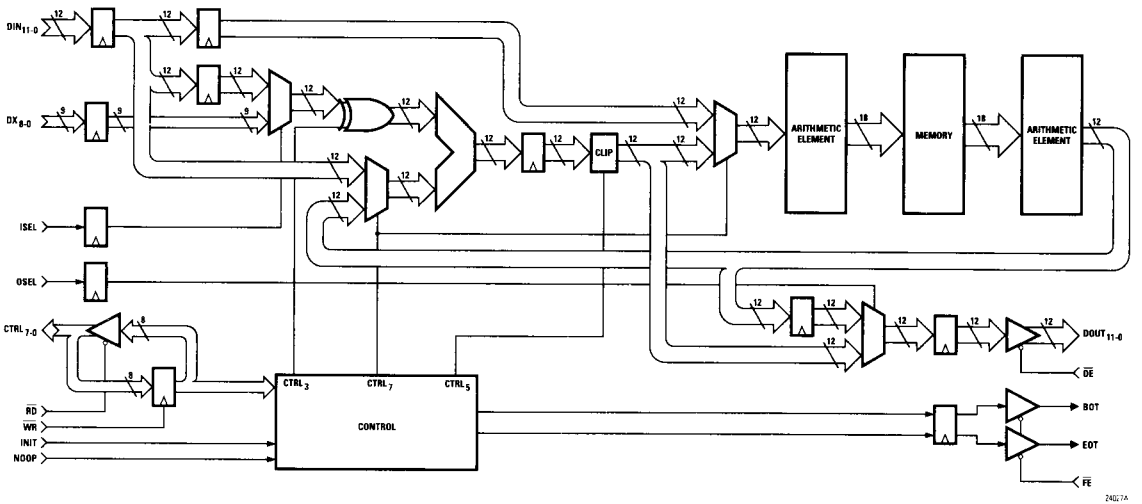
Applications

- Image Processing, Graphics
- Pulse And Image Compression
- Video Teleconferencing
- Linear Predictive Coding
- Differential Pulse Code Modulation
- Electronic Publishing
- Medical Imaging And Archiving

Associated Products

- TMC2220 — 4x32 Correlator
- TMC2250 — 2-D 3x3 FIR Filter
- TMC2272 — Colorspace Converter

Figure 1. Functional Block Diagram



Functional Description

The TMC2311 comprises five internal blocks: a controller, two arithmetic elements, a data transpose memory and an auxiliary adder circuit (*Figure 1*). Each arithmetic element (AE) can compute an 8-point 1-dimensional DCT in 16 clock cycles. When the device is configured to perform 2-dimensional transforms, the first AE computes the DCT of each consecutive row of 8 pixels. The results of each 8x1 DCT are written into the intermediate memory. After eight 1-dimensional transforms are computed, the device computes the DCT of each consecutive 8-pixel column, while (if so instructed) computing the DCTs of the rows of the next block of data. The auxiliary adder/subtractor can be used with a forward and inverse transform in linear predictive coding applications. The adder can also be used alone to perform differential pulse code modulation without the cosine transform. In all modes and configurations the device operates on continuous data at a rate of up to 15 Megapels/second and can perform a complete 8x8 DCT every 128 clock cycles.

Control

The control block includes the chip's preprogrammed controller, sequencer, and microcode generator. The host system needs only to load a single 8-bit control word on C_{7-0} and then strobe the INIT pin. The chip will proceed automatically through the chosen operation without further supervision.

Arithmetic Element #1

Comprising a multiplier and two adder/subtractors, bypassable processor AE1 performs a series of one-dimensional 8-point forward or inverse DCTs on the incoming data, writing its 8-point transform results into the transpose memory.

Data Transpose Memory

This two-port 64-word RAM collects each group of eight consecutive 8-point transformed data sets from AE1 and then passes them to AE2 while collecting the next group, thereby acting as a large pipeline buffer. When enabled, the DTM accepts each 64-point data block in row-major sequence and returns the same data in column-major order, effecting a "corner turn." Bypassing this block leaves the data sequence unchanged.

Arithmetic Element #2

Identical to AE1, bypassable data processor AE2 performs eight 8- point one-dimensional transforms on each 64-point block of data. Each transform pulls one data point from each of the eight transforms done by AE1, completing the 8x8 two-dimensional transform. For one-dimensional transforms, either AE can be bypassed.

Auxiliary Adder

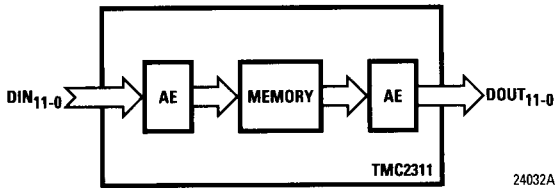
The remaining circuitry in ***Figure 1*** can be employed as either a presubtractor or a post-adder. (See ***Applications Discussions*** of ***Linear Predictive Coding, Differential Pulse Code Modulation,*** and ***Interframe Coding.***) As instructed by $CTRL_3$ (INVERT), $CTRL_7$ (XSEL), ISEL, and OSEL, this adder combines the 9-bit two's complement data entering on port DX_{8-0} with either the incoming or emerging data stream.

Operating Modes

The TMC2311's five operating modes are selected by control pins $CTRL_{2-0}$. The device can be configured in the following ways:

The device will perform a two-dimensional transform if $CTRL_{2-0}$ = 000 or 001. AE1 performs a one-dimensional DCT (IDCT if $CTRL_3$ = 1) on each of eight 8-pixel rows of data supplied row-by-row to DIN_{11-0}. Results from each block of eight transforms are fed via the Transpose Memory to AE2, which performs a one-dimensional DCT (IDCT) on each of the eight 8-pixel columns of data, in turn (***Figure 2***).

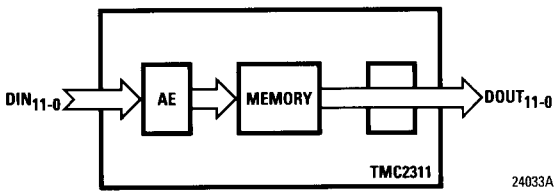
Figure 2. 2-D Transform (With Transpose)



The device can also perform one-dimensional DCTs (IDCTs) with or without memory transpose.

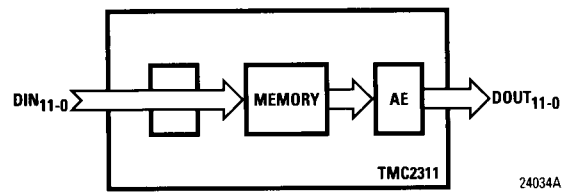
When $CTRL_{2-0}$ = 010, the chip will transform eight 8-point rows of incoming data, then transpose the results without transforming the columns (***Figure 3***).

Figure 3. 1-D Transform With 8x8 Transpose



When $CTRL_{2-0}$ = 011, the device accepts eight 8-point rows of data and transposes them before AE2 performs one-dimensional DCTs (IDCTs) of the columns (***Figure 4***).

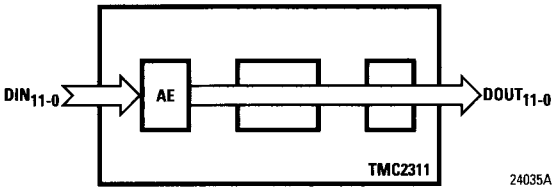
Figure 4. 8x8 Transpose With 1-D Transform



The device can also perform one-dimensional transforms without transposes. When $CTRL_{2-0}$ = 100 or 101, AE1 performs a one-dimensional DCT or IDCT on each incoming 8-point row of data (***Figure 5***).

Transforms

Figure 5. 1-D Transform (Without Transpose)



Finally, the device will perform the memory transpose with no DCT when $CTRL_{2-0}$ = 110 or 111 (*Figure 6*).

Figure 6. Memory Transpose (Without Transform)

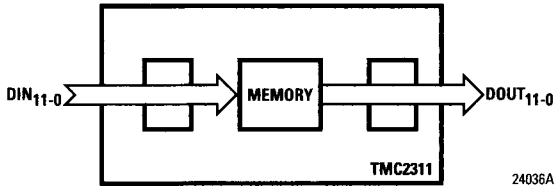


Table 1 summarizes the operation of controls $CTRL_7$, $CTRL_3$, ISEL, and OSEL, which "fine tune" the mode selection by programming the presubtractor/postadder and the transform direction. (Where a full two- dimensional FCT or IFCT is needed, $CTRL_{2-0}$ must be set to 011. $CTRL_7$=1 then enables presubtraction and OSEL=1 enables postaddition, as desired by the user.)

Table 1. Operating Mode Configurations

Application	Function	Device Configuration			
		$CTRL_7$	$CTRL_3$	ISEL	OSEL
2D DCT	2D FCT	0	0	X	0
2D IDCT	2D IFCT	0	1	X	0
Interframe Compress	2D FCT, Presubtract	1	0	0	0
Interframe Decompress	2D IFCT, Post Add	0	1	0	1
LPC	2D FCT, Presubtract	1	0	0	0
ILPC	2D IFCT, Post Add	0	1	0	1
LPC Directly Out	DOUT=DIN-DX	1	0	0	1
ILPC Directly Out	DOUT=DIN+DX	1	1	0	1
DPCM Directly Out	DOUT(k)=DIN(k)-DIN(k-1)	1	0	1	1
IDPCM Directly Out	DOUT(k)=DIN(k)+DIN(k-1)	1	1	1	1
DPCM w/ Transpose	DOUT(k)=DIN(k)-DIN(k-1)	1	0	1	0
IDPCM w/ Transpose	DOUT(k)=DIN(k)+DIN(k-1)	1	1	1	0

Notes: LPC/ILPC Linear Predictive Coding (Forward/Inverse)
DPCM/IDPCM Differential Pulse Code Modulation (Forward/Inverse)

Signal Definitions

Control

INIT — Single pass "start" command. INIT=0 resets the internal logic and output flags and updates the $CTRL_{7-0}$ parameters. INIT is registered and must be LOW for at least 3 clock cycles. INIT returning HIGH starts the transform. The first data point is loaded two cycles later.

NOOP — Input clock disable. NOOP=1 freezes operation of the device on the next CLK rising edge. Operation commences from where it stopped one cycle after NOOP returns LOW.

$\overline{WR}$ — Control word preload command. $\overline{WR}$=0 loads CTRL7-0 parameters into the device's preload register. The next INIT rising edge transfers the preloaded parameters into the chip's working registers.

$\overline{RD}$ — Control word (READ) command. $\overline{RD}$=0 allows the preloaded parameters $CTRL_{7-0}$ to be read.

$CTRL_{2-0}$ — MODE Control. Defines the internal configuration (mode) of the device, selecting either 2-dimensional or 1-dimensional transforms and/or the access to the internal Transpose Memory (***Figures 2*** through ***6***.)

$CTRL_{2-0}$	Operation
000	2–D Transform
001	2–D Transform
010	1–D Transform, Transpose
011	Transpose, 1–D Transform
100	1–D Transform
101	1–D Transform
110	Transpose
111	Transpose

$CTRL_3$ — Inverse Transform Enable (INV). INV=0 selects a forward DCT. If INV=1, the device will compute the Inverse DCT. INV also inverts the data to one side of the auxiliary adder. When and only when INV=0, data from the multiplexer which selects the DX port or delayed DIN port will be inverted.

$CTRL_4$ — Automatic Reinitialization (AUTOINIT). AI=0 allows continuous operation of device. When AI=1, the device will halt at the end of the specified transform.

$CTRL_5$ — Arithmetic Limit (CLIP). CLIP=1 saturates data outputs to 9 bits. CLIP is useful when presubtraction or postaddition is used with the DCT or IDCT.

$CTRL_6$ — Flag Control (FC). FC determines when the output flags, BOT and EOB, appear. When FC=0, both flags are output with the corresponding data result. When FC=1, the flags appear two clock cycles earlier.

$CTRL_7$ — Auxiliary Adder Select (XSEL). XSEL controls two multiplexers within the auxiliary adder circuitry. The first mux feeds the non-inverted input to the adder either the DIN port (XSEL=1) or outputs from the core of the device (XSEL=0). The second mux selects the data entering the core of the device from either the input port (XSEL=0) or adder output (XSEL=1). See ***Applications, Operating Mode Configurations***.

ISEL — Input Data Select. ISEL=0 connects the inverted (optional) input of the auxiliary adder to the DX port. When ISEL=1, the DIN port is connected, via a one data cycle delay. Output from this mux to the adder is inverted when INV=0. See ***Applications, Operating Mode Configurations***.

OSEL — Output Data Select. When OSEL=0, data results from the device core pass to the final output register. When OSEL=1, results from the adder pass to the final output register. See ***Applications, Operating Mode Configurations***.

$\overline{OE}$ — Asynchronous active LOW OUTPUT ENABLE for data output port, $DOUT_{11-0}$. When $\overline{OE}$=1, every output is forced into a high-impedance state.

$\overline{FE}$ — Active LOW asynchronous output FLAG ENABLE. When $\overline{FE}$=1, BOT and EOB are forced into a high-impedance state.

Data Inputs

DIN_{11-0} Data INput Port (12-bit two's complement format). DIN is the input port for both FORWARD and INVERSE transforms. DIN11 is the MSB. For two dimensional forward transforms, data precision is limited to 9 bits, DIN_{8-0}, and must be sign-extended into the remaining MSBs. Data exceeding the lower 9-bit range may cause an internal overflow. For INVERSE transforms, the entire 12-bit input port may used without risk of overflow.

DX_{8-0} Auxiliary Data Input Port (9-bit two's complement format). Feeds one side of auxiliary adder. DX_8 is the MSB. Auxiliary inputs can be provided to the device for linear predictive coding (LPC) where pixel differences are transformed. In the FORWARD direction, inputs supplied to the DX port (and selected via ISEL) will be subtracted from pixel values input simultaneously on the DIN port. In the INVERSE direction, DX inputs will be added to outputs following the desired tranform operation. The DX inputs must be delayed so that they appear at the adder simultaneously with the corresponding pixel outputs.

Data Outputs

$DOUT_{11-0}$ Data OUTput Port (12-bit, two's complement format). DOUT is the output port for both FORWARD and INVERSE transforms. $DOUT_{11}$ is the MSB. When CLIP=1, all data outputs are clipped to 9 bits, $DOUT_{8-0}$, with sign extension into the remaining MSBs. DOUT is forced into a high-impedance state when $\overline{OE}$=1.

Output Flags

BOT Beginning Of Transform. Toggles LOW to denote the first result of each one-dimensional 8-point transform or the first result of each 8-point row or column of a two-dimensional transform. When FC=0, BOT will appear simultaneously with the corresponding result. When FC=1, BOT will appear one data I/O cycle earlier.

EOB End Of Block. Toggles LOW to signal the last result of the entire (8 or 64 point) transform field. When FC=0, EOB appears simultaneously with the last data result. When FC=1, EOB appears two cycles earlier.

Clock

CLK Data Path Clock. The device operates with a clock of 0 to 30MHz. All internal operations are referenced to the rising edges of CLK; I/O operations except $CTRL_{7-0}$ read and write, to alternate rising edges of CLK.

Power

V_{DD}, GND The TMC2311 operates from a single +5 Volt supply. All V_{DD} and GND pins must be connected.

Table 2. Data Formats and Bit Weighting

	11	10	9	8	7	6	5	4	3	2	1	0
Input Data Format – Forward Transforms												
DIN	S	S	S	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
Input Data Format – Inverse Transforms												
DX:	-2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
				-2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	-2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
Output Data Format – Forward Transforms												
DOUT:	-2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
Output Data Format – Inverse Transforms												
	S	S	S	-2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Notes: S = Sign Extension.
In forward transforms, system should feed two's complement sign bit to DIN_{11-8} for 9-bit data size.
In inverse transforms, chip will output two's complement sign bit into pins $DOUT_{11-8}$.

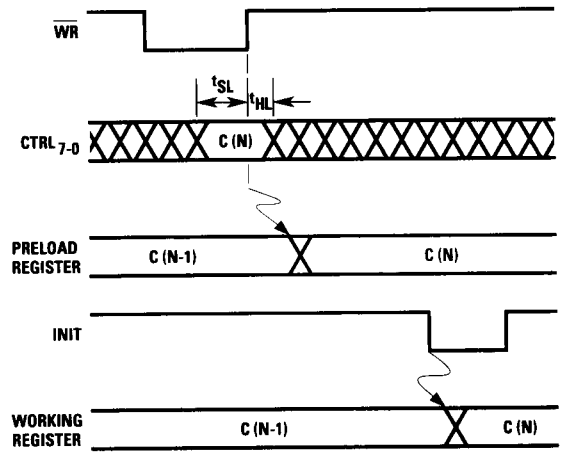
Operation and Timing

Initialization

Control Word Preload Timing

The self-sequencing TMC2311 requires no cycle-to-cycle supervision by the host system. On the rising edge of $\overline{WR}$, the user loads an 8-bit control word ($CTRL_{7-0}$) which sets 5 device parameters: mode and direction of the transform, continuous (or non-continuous) device operation, format of output data and timing of the output flags. The control parameters preloaded via $CTRL_{7-0}$ are registered internally and updated by the INIT signal. Control load timing is displayed in *Figure 7*.

Figure 7. Control Preload Timing



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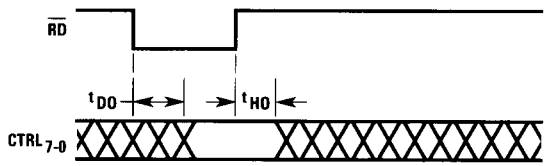
Control Word Read Timing

The TMC2311 also permits the user to read the preloaded control word value back through $CTRL_{7-0}$, a bidirectional port. When $\overline{RD}$=0, the $CTRL_{7-0}$ port outputs the control information stored in the device (*Figure 8*).

Figure 8. Control Read Timing



Data Input Timing

After the TMC2311 is initialized, data are input to DIN_{11-0} and DX_{8-0} on alternate rising edges of the device system clock. When the device is set for forward DCTs with transpose, data inputs are accepted in row-major format, i.e., line-by-line through the 8x8 transform window. When the device performs inverse DCTs, inputs are accepted in column-major format. Following the rising edge of INIT command, data inputs can be continuously loaded into the device on alternate rising edges of the system clock (*Figure 9*).

Data Output Timing

Results are output at half the system clock rate. The initial result latency and the number of results depends on the device operation specified by $CTRL_{2-0}$. Once the first result reaches the output port, remaining results will appear continuously. When the TMC2311 is set to perform forward DCTs with transpose, output data are written in column-major format. In the inverse direction, data results are returned row-by-row (*Figure 10*).

Figure 9. Data Input Timing

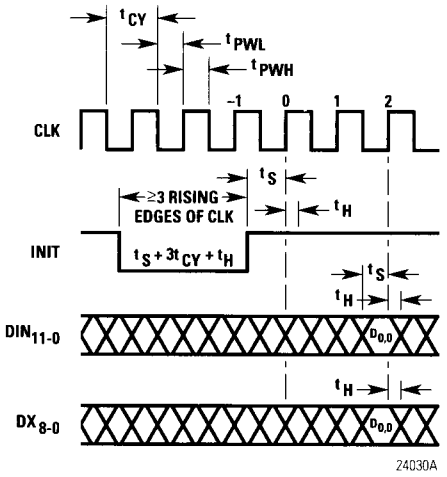
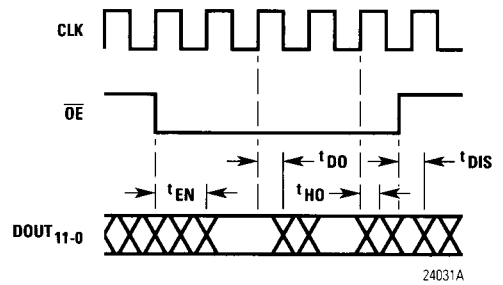


Figure 10. Data Output Timing



Overall Timing

The TMC2311 will expect data in groups of 8 or 64 points at regular intervals based on the mode of operation defined by $CTRL_{2-0}$. Results will be returned by the TMC2311 in similar groups following a predetermined initial latency. For applications that use the auxiliary adder ahead of the core of the device, corresponding DX and DIN inputs should be presented simultaneously to the device. Applications that use the adder after the DCT/memory core must account for the device's internal latency (*Table 3*). Each DX port input must be timed to appear at the adder one data cycle ahead of its corresponding output.

Table 3. Data Output Latency

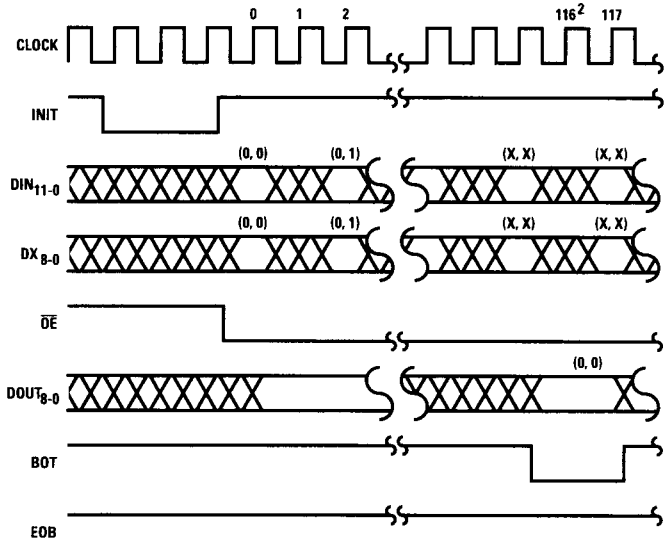
$CTRL_{2-0}$	Operation	Latency*
000	2-D Transform	232 clocks
001	2-D Transform	232
010	1-D Transform, Transpose	200
011	Transpose, 1-D Transform	200
100	1-D Transform	56
101	1-D Transform	56
110	Transpose	168
111	Transpose	168

*cycles after INIT goes high

If AUTOINIT ($CTRL_4$)=0, the device will operate continuously with no interruption between transforms. Otherwise the device will halt after the specified number of data points have been processed. When AUTOINIT=1, device operation will resume with the next INIT signal.

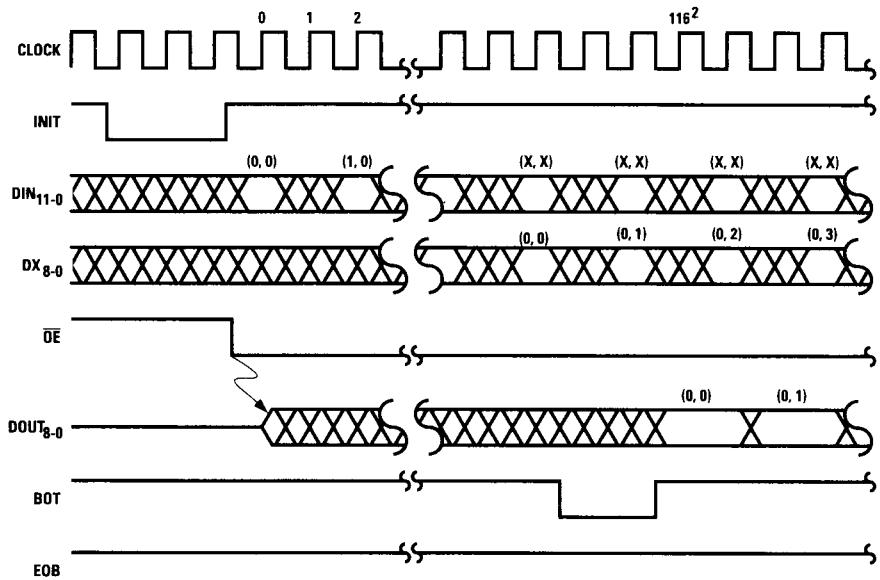
The TMC2311 also provides two output flags to differentiate between the rows/columns of the transform window and between individual transform blocks. The Beginning Of Transform (BOT) flag goes LOW with the first data result of each 8x1 transform row or column. A second flag, End Of Block, EOB, delineates transform blocks. EOB will go LOW when the last data point of each 8x1 (one dimensional mode) or 8x8 (two dimensional mode) transform is output. The user can program these flags to appear with their respective data (FC=0) or one data cycle earlier (FC=1). ***Figure 11*** shows the overall timing of a forward 2-D DCT with pre-subtraction and FC=0. ***Figure 12*** shows the overall timing of an inverse 2-D DCT with post addition and FC=1, demonstrating the timing for inputs to auxiliary port DX_{8-0} and the shift in flag timing.

Figure 11. Overall Timing - Forward Transform (Flag Control=0)

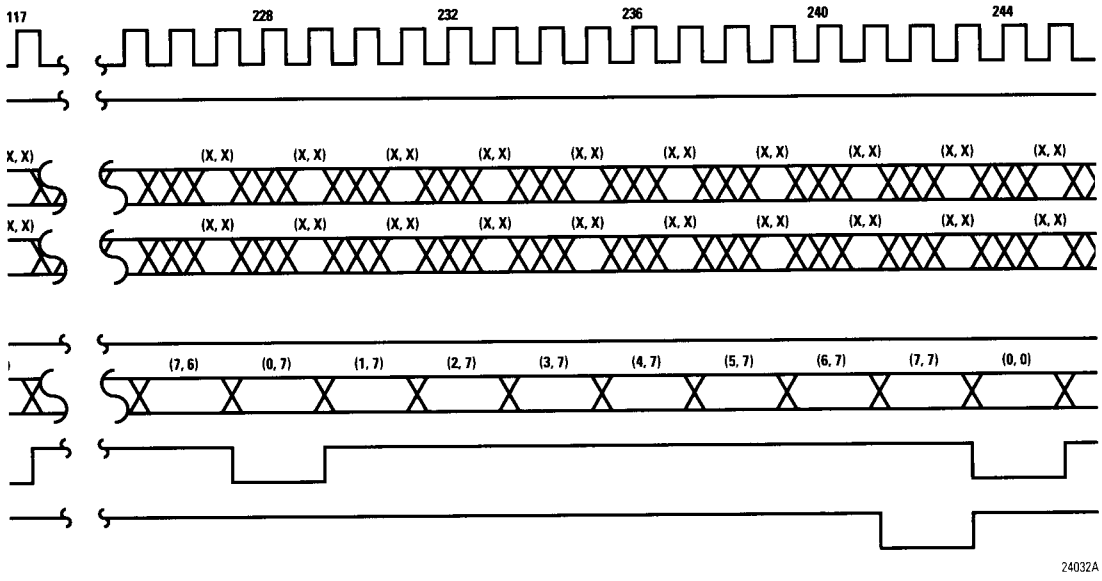


Notes: 1. DIN_{11-0} (i,j) aligned with DX_{8-0} (i,j), but alignment with $DOUT_{11-0}$ is mode-dependent..
2. $DOUT_{11-0}$ (0,0) is valid on CLK rising edge 116 in two-dimensional transfer modes only.

Figure 12. Overall Timing - Inverse Transform (Flag Control=1)



Notes: 1. DX_{8-0} (i,j) precedes $DOUT_{11-0}$ (i,j) by two CLK cycles, but alignment with DIN_{11-0} is mode-dependent.
2. $DOUT_{11-0}$ (0,0) is valid on CLK rising edge 116 in two-dimensional transform modes only.


117
228
232
236
240
244
(X, X)
(7, 6)
(0, 7)
(1, 7)
(2, 7)
(3, 7)
(4, 7)
(5, 7)
(6, 7)
(7, 7)
(0, 0)
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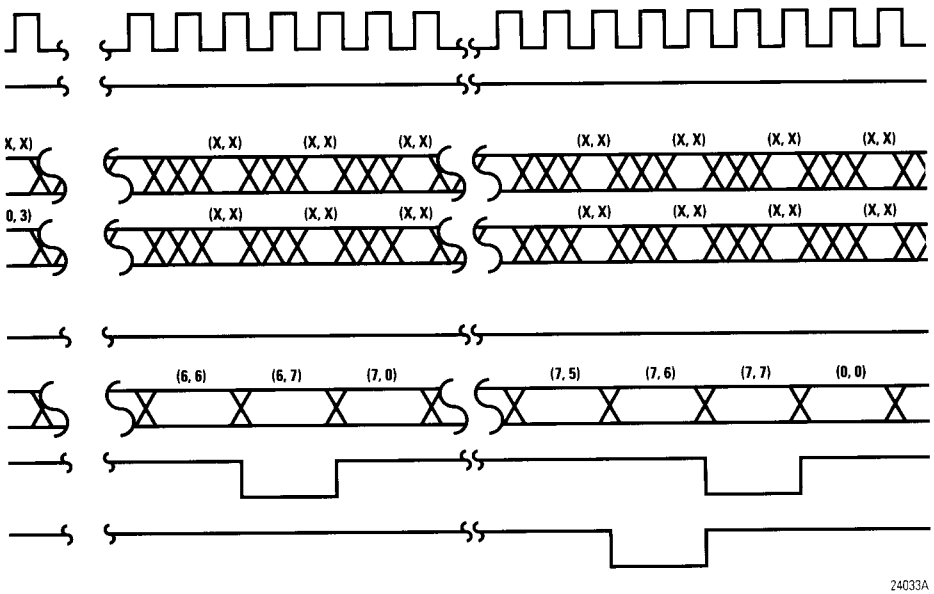
(X, X)
(6, 6)
(6, 7)
(7, 0)
(7, 5)
(7, 6)
(7, 7)
(0, 0)
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Instrumentation Products

Product	Resolution Bits	Conv. Rate[1] (Msps)	RMS/RMS SNR[1] (dB)	Package	Grade[2]	Notes
TDC1035	8	—	—	B7, R3	C, V	Peak digitizer. Digitizes peak value of pulses as narrow as 12 ns.
TDC1038	8	20	45	B6, N6, R3, C3, E1	C, V	Low power version of TDC1048.
TDC1048	8	20	45	B6, N6, C3, E1	C, V, SMD	Industry standard video A/D.
TDC1058	8	20	45	B6, N6, R3, E1	C	New industry standard video A/D. Single +5V power supply. TDC1048 performance equivalent.
TMC1173-10	8	10	45	N2, M7, R3	C	Low power CMOS video A/D with integral Track/
-05	8	5	45	M7, N2, R3	C	Hold. +2.7V to +3.3V power supply.
TMC1175-20	8	20	45	B2, N2, C3, M7, R3	C, V	Low power CMOS video A/D with integral Track/ Hold. Includes D/A
-30	8	30	45	M7, N2, R3	C, V	
-40	8	40	45	M7, N2, R3, E1	C, V	
TDC1049	9	30	48	J0, J3, C1, L1, G8, E1	C, V, SMD	ECL interface
TDC1020	10	20	55	J1, G0, E1	C, V	Monolithic video A/D, TTL interface. ±2V input range.

Notes:
1. Guaranteed. See product specifications for test conditions.
2. A = High reliability, T_C = -55°C to 125°C. C = Commercial, T_A = 0°C to 70°C. V = MIL-STD-883 Compliant, T_C = -55°C to 125°C. SMD = Available per Standardized Military Drawing, T_C = -55°C to 125°C.
3. A = High reliability, T_C = -20°C to 95°C.

Product	Clock Rate[1] (MHz)	Frequency Resolution (Hz)	SFDR (dB)	Output	Package	Grade	Notes
Digital Frequency Synthesizers							
TMC2340-1	25	0.006	106	Dual 16 Bit	G1, H5, L5	C, V	AM, FM, PM inputs.
	20	0.006	106	Dual 16 Bit	G1, H5, L5	C, V	Quadrature outputs.

Pin Drivers	Slew Rate	Voltage Range	Output Swing (p-p)	Output Three State	Package
RC7310	1.2 V/ns	-3.0 to +8V	10 Vp-p	No	28 PLCC
RC7311	2 V/ns	-3.0 to +8.0V	10V	No	28 PLCC, 16 LDCC
RC7315	1.8 V/ns	-2.5 to 7.5V	9.5V	Yes	28 EPLCC
RC7316	3.2 V/ns	-3.0 to 7.0V	9.5V	Yes	28 EPLCC, 16 LDCC

Comparators	Propagation Delay	Voltage Range	Input Bias Current	Input Capacitance	Package
RC7341 (Window)	2.0 ns	-4V to +8V	10 µA (over -4 to +8V)	2 pF	All are
RC7342 (Dual)	2.0 ns	-4V to +8V	10 µA (over -4 to +8V)	1.25 pF	available in
RC73687 (Dual)	2.2 ns	-4V to +8V	5 µA	2 pF	

Precision Measurement Unit	Force Voltage Range	Force Current Ranges	Force Current Resolution	Accuracy	Package
RC7351	-5V to +15V	(4 Ranges)	±0.05%	12 bits, 0.5%	28 PLCC
		±500 nA to ±20 µA		gain error	
		±2 µA to ±200 µA			
		±10 µA to ±1 mA			
		±500 µA to ±40 mA			

Notes:
1. Both the RC7342 and the RC73687 are pin-for-pin compatible with 9687 standard comparators.

For Applications Information, call (619) 457-1000.
For Technical Literature, call 1-800-722-7074.

Electrical characteristics within specified operating conditions[1]

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
I_{DDQ}	Supply Current, Quiescent[2]	V_{DD}=Max, V_{IN}=0V, TS=5V		30	mA
I_{DDU}	Supply Current, Unloaded	V_{DD}=Max, f=30MHz, TS=5V		130	mA
I_{IL}	Input Current, Logic LOW	V_{DD}=Max, V_{IN}=0V		–10	µA
I_{IH}	Input Current, Logic HIGH	V_{DD}=Max, V_{IN}=V_{DD}		+10	µA
V_{OL}	Output Voltage, Logic LOW	V_{DD}=Min, I_{OL}=Max		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD}=Min, I_{OH}=Max	2.4		V
I_{OZL}	Hi-Z Output Leakage Current,	V_{DD}=Max, V_{IN}=0V Output LOW		–40	mA
I_{OZH}	Hi-Z Output Leakage Current,	V_{DD}=Max, V_{IN}=0V Output HIGH		+40	mA
I_{OS}	Short Circuit Output Current	V_{DD}=Max, Output HIGH one pin to ground one second duration max.		–45	mA
C_I	Input Capacitance	T_A=25°C, f=1MHz		10	pF
C_O	Output Capacitance	T_A=25°C, f=1MHz		10	pF

Note: 1. Actual test conditions may vary from those shown above, but guarantee operation as specified.
2. Following power-on, the TMC2311 must be clocked for at least 10 clock cycles before the clock is disabled.

Switching characteristics within specified operating conditions[1]

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
t_{DO}	Output Delay	V_{DD}=Min, C_{Load}=40pF		16	ns
	TMC2311			16	
	TMC2311-1			16	
	TMC2311-2			12	
t_{HO}	Output Hold Time	V_{DD}=Max, C_{Load}=40pF	4		ns
t_{ENA}	Three-State Output Enable Delay	V_{DD}=Min, C_{Load}=40pF		16	ns
	TMC2311			16	
	TMC2311-1			16	
	TMC2311-2			12	
t_{DIS}	Three-State Output Disable Delay	V_{DD}=Min, C_{Load}=40pF		22	ns

Note: 1. All transitions except for t_{DIS} and t_{ENA} are measured at a 1.5V level.

Figure 13. Equivalent Input Circuit

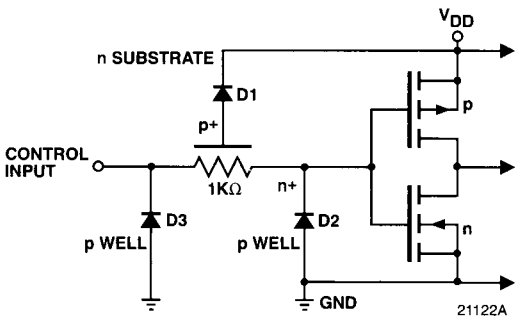
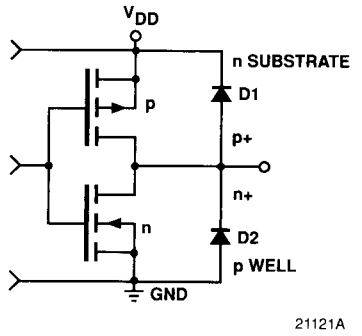


Figure 14. Equivalent Output Circuit



Applications Discussions

Frequency Domain Coding - Basic System

Frequency domain coding entails partitioning an image into (for example) 8x8 pixel blocks, then determining the two-dimensional spatial frequency spectrum of each block. In image compression, each component is then quantized by a frequency-specific factor, which tends to be smaller (more precise) for the dominant lower- frequency components and larger (coarser) for the less crucial higher-frequency components. Quantization effects compression by reducing the number of bits per frequency bin and by zeroing out high-frequency, low-energy bins. Following the quantizer, the scaled frequency data are then (arithmetic or Huffman) coded into a format that will allow them to be transmitted (or archived) even more economically. In particular, the JPEG modified Huffman coding represents each string of "zeroed out" bins with a compact code.

The transmitted images are reconstructed by reversing these operations. Coded information is received and restored to frequency information through a decoder. The received (or retrieved) data then pass through an inverse quantizer that restores the most important frequency components, albeit at somewhat grainier than original levels. Finally, the image is reconstructed by the inverse DCT. In practice, compression ratios of up to 20:1 can provide visually acceptable results with still images.

The basic compression circuit (*Figure 15*) shows a sample implementation of an intraframe compressor. The system contains an encoder comprising the TMC2311 DCT chip, a quantizer and a coder. Images are reconstructed in a complementary system with a decoder, a dequantizer, and a TMC2311 (inverse) DCT chip.

Figure 15. Basic System

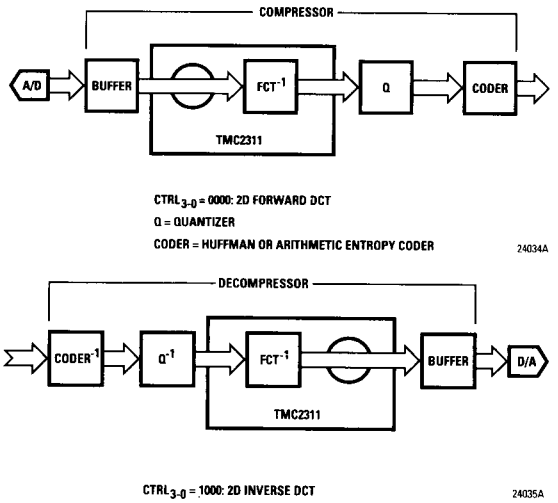
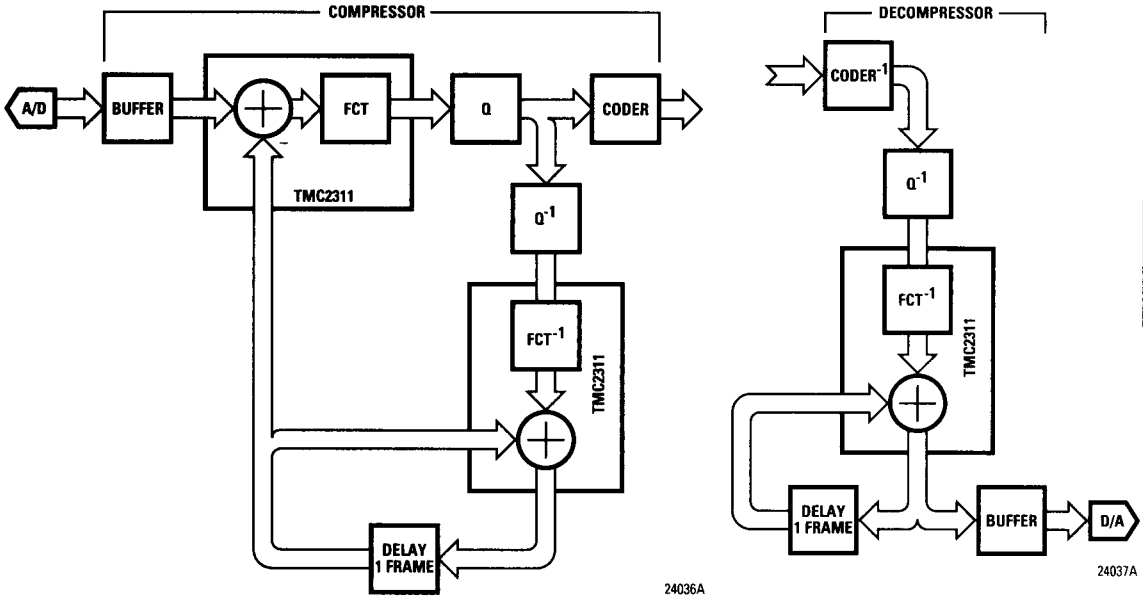


Figure 16. Interframe Compression System



Interframe Compression

Figure 16 shows a moving picture extension of frequency domain coding, which processes differences between the corresponding pixels of successive image frames. Interframe compression describes areas of change within a moving image by comparing each new frame against earlier frames. Prior to the DCT, a block from the new frame is subtracted from the corresponding block of the previous frame. The resulting differences are transformed, quantized, coded, and transmitted. The compressed data are then reconstructed by reversing the processing steps: decode, dequantize, inverse DCT, then accumulate differences from frame to frame. Transforming only these differences increases the achievable compression.

Linear Predictive Coding System

Many critical biomedical and defense applications require that images be compressed and then restored "losslessly," i.e., without degradation. One technique, referred to as Linear Predictive Coding (LPC), has been very effective in speech compression. For image compression, LPC entails coding the differences between the current and previous pixel blocks of the same frame. This technique of intraframe compression can be used with or without the DCT. Much of the *Figure 16* interframe compression architecture can also be applied here, although the delay block now corresponds to delay within a single frame.

To obtain lossless compression, the user may code the differences between pixel blocks directly, without the DCT. This variety of intraframe compression, demonstrated in *Figure 17*, uses just the auxiliary adder of the TMC2311. In the forward direction, the differences are computed and transferred to the quantizer and coder circuitry where they are readied for transmission. In the inverse direction, the reconstruction process involves inverse coding and quantization, followed by cumulative addition of the image differences by the TMC2311's auxiliary adder.

Package Interconnections

Signal Type	Signal Name	Function	Value	R1 Package Pin
Power	V_{DD}	Supply Voltage	+5.0V	2 10 17 33 53 68
	GND	Ground	0.0V	1 4 9 13 18 26 35 52 67
Clock	CLK	System Clock	TTL	65
Inputs	DIN_{11-0}	Data Inputs	TTL	44 45 46 47 48 49 50 51 54 55 56 57
	DX_{8-0}	Aux Adder In	TTL	34 36 37 38 39 40 41 42 43
Outputs	$DOUT_{11-0}$	Data Outputs	TTL	5 6 7 8 11 12 14 15 16 19 20 21
	BOT	Begin Transform	TTL	22
	EOB	End Of Block	TTL	23
Control	INIT	Initialize	TTL	60
	NOOP	No Operation	TTL	61
	$\overline{WR}$	Control Preload	TTL	66
	$\overline{RD}$	Read Control	TTL	64
	ISEL	Input Data Select	TTL	59
	OSEL	Output Select	TTL	58
	$\overline{OE}$	Output Enable	TTL	3
	$\overline{FE}$	Flag Enable	TTL	62
	$CTRL_{7-0}$	Control Params	TTL	32 31 30 29 28 27 25 24
	DNR	Test Pin	—	63
Do Not Connect				

Ordering Information

Product Number	Data Rate MHz	Temperature Range	Screening	Package	Package Marking
TMC2311R1C	13.5	STD-T_A = 0°C to 70°C	Commercial	68 Pin PLCC	2311R1C
TMC2311R1C1	14.5	STD-T_A = 0°C to 70°C	Commercial	68 Pin PLCC	2311R1C1
TMC2311R1C2	17.8	STD-T_A = 0°C to 70°C	Commercial	68 Pin PLCC	2311R1C2

40G06753 Rev B 8/93