

SCAN182374A

D Flip-Flop with 25Ω Series Resistor Outputs

General Description

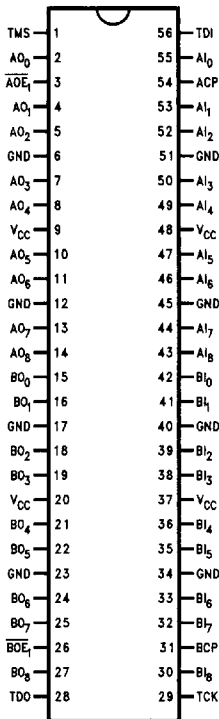
The SCAN182374A is a high performance BiCMOS D-type flip-flop featuring separate D-type inputs organized into dual 9-bit bytes with byte-oriented clock and output enable control signals. This device is compliant with IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture with the incorporation of the defined boundary-scan test logic and test access port consisting of Test Data Input (TDI), Test Data Out (TDO), Test Mode Select (TMS), and Test Clock (TCK).

Features

- IEEE 1149.1 (JTAG) Compliant
- High performance BiCMOS technology
- 25Ω series resistor outputs eliminate need for external terminating resistors
- Buffered positive edge-triggered clock
- TRI-STATE® outputs for bus-oriented applications
- 25 mil pitch SSOP (Shrink Small Outline Package)
- Includes CLAMP, IDCODE and HIGHZ instructions
- Additional instructions SAMPLE-IN, SAMPLE-OUT and EXTTEST-OUT
- Power up TRI-STATE for hot insert
- Member of National's SCAN Products

Ordering Code: See Section 11

Connection Diagram



TL/F/11545-1

Pin Names	Description
AI ₍₀₋₈₎ , BI ₍₀₋₈₎	Data Inputs
ACP, BCP	Clock Pulse Inputs
$\overline{AOE}_1, \overline{BOE}_1$	TRI-STATE Output Enable Inputs
AO ₍₀₋₈₎ , BO ₍₀₋₈₎	TRI-STATE Outputs

Order Number	Description
SCAN182374ASSC	SSOP in Tubes
SCAN182374ASSCX	SSOP in Tape and Reel
SCAN182374AFMQB	Flatpak Military

Truth Tables

Inputs			$AO_{(0-8)}$
ACP	$\uparrow AO\bar{E}_1$	$AI_{(0-8)}$	
X	H	X	Z
\swarrow	L	L	L
\swarrow	L	H	H

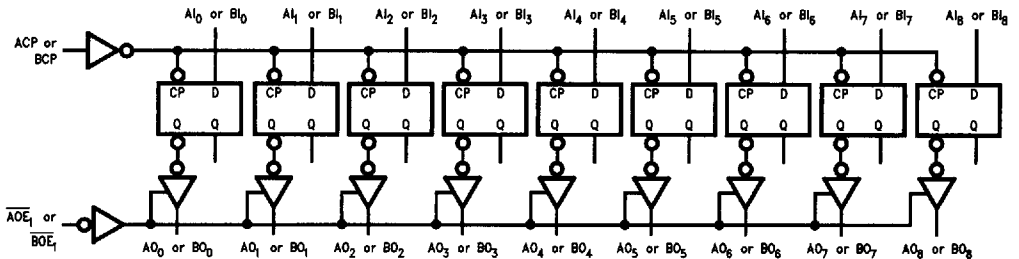
Inputs			$BO_{(0-8)}$
BCP	$\uparrow BO\bar{E}_1$	$BI_{(0-8)}$	
X	H	X	Z
\swarrow	L	L	L
\swarrow	L	H	H

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance
 \swarrow = L-to-H Transition
 \uparrow = Inactive-to-active transition must occur to enable outputs upon power-up.

Functional Description

The SCAN182374A consists of two sets of nine edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable pins are common to all flip-flops. Each set of the nine flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (ACP or BCP) transition. With the Output Enable (\bar{AOE}_1 or \bar{BOE}_1) LOW, the contents of the nine flip-flops are available at the outputs. When the Output Enable is HIGH, the outputs go to the high impedance state. Operation of the Output Enable input does not affect the state of the flip-flops.

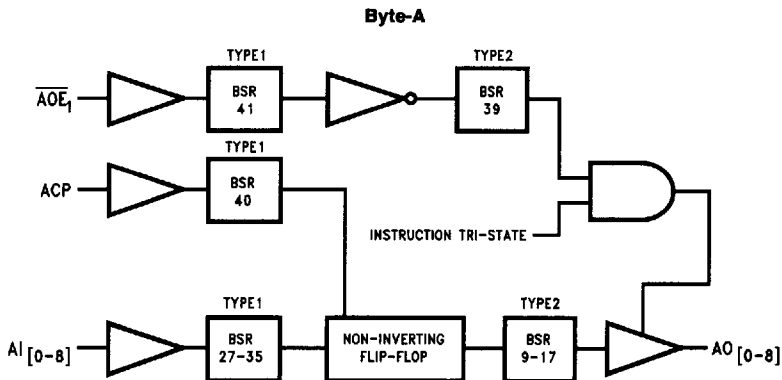
Logic Diagram



TL/F/11545-2

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

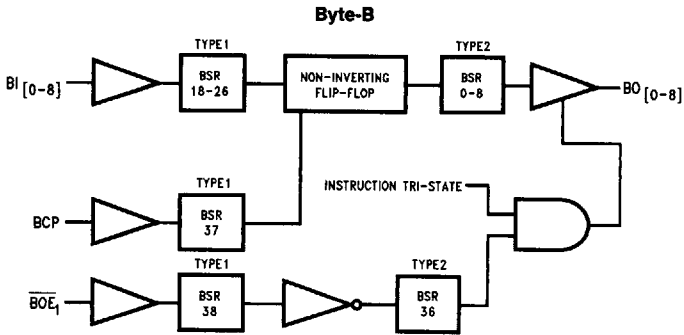
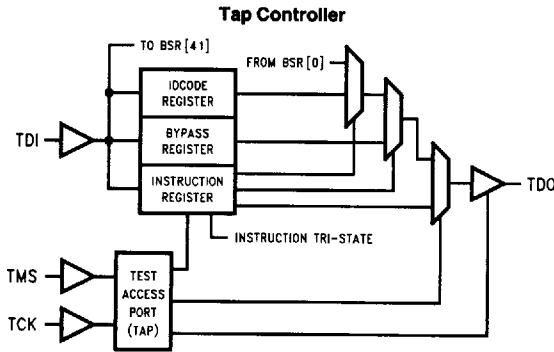
Block Diagrams



TL/F/11545-3

Note: BSR stands for Boundary Scan Register

Block Diagrams (Continued)



Note: BSR stands for BOUNDARY-SCAN Register

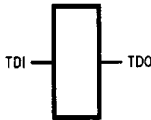
Description of BOUNDARY-SCAN Circuitry

The scan cells used in the BOUNDARY-SCAN register are one of the following two types depending upon their location. Scan cell TYPE1 is intended to solely observe system data, while TYPE2 has the additional ability to control system data. (See IEEE Standard 1149.1 *Figure 10-11* for a further description of scan cell TYPE1 and *Figure 10-12* for a further description of scan cell TYPE2.)

Scan cell TYPE1 is located on each system input pin while scan cell TYPE2 is located at each system output pin as well as at each of the two internal active-high output enable signals. AOE controls the activity of the A-outputs while BOE controls the activity of the B-outputs. Each will activate their respective outputs by loading a logic high.

The BYPASS register is a single bit shift register stage identical to scan cell TYPE1. It captures a fixed logic low.

Bypass Register Scan Chain Definition Logic 0



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SCAN182374A Product IDCODE (32-Bit Code per IEEE 1149.1)

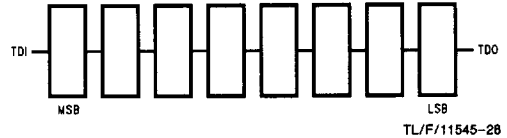
Version	Entity	Per Number	Manufacturer ID	Required by 1149.1
0000	111111	0000000111	00000001111	1

MSB

LSB

The INSTRUCTION register is an 8-bit register which captures the default value of 10000001 (SAMPLE/PRELOAD) during the CAPTURE-IR instruction command. The benefit of capturing SAMPLE/PRELOAD as the default instruction during CAPTURE-IR is that the user is no longer required to shift in the 8-bit instruction for SAMPLE/PRELOAD. The sequence of: CAPTURE-IR → EXIT1-IR → UPDATE-IR will update the SAMPLE/PRELOAD instruction. For more information refer to the section on instruction definitions.

Instruction Register Sscan Chain Definition

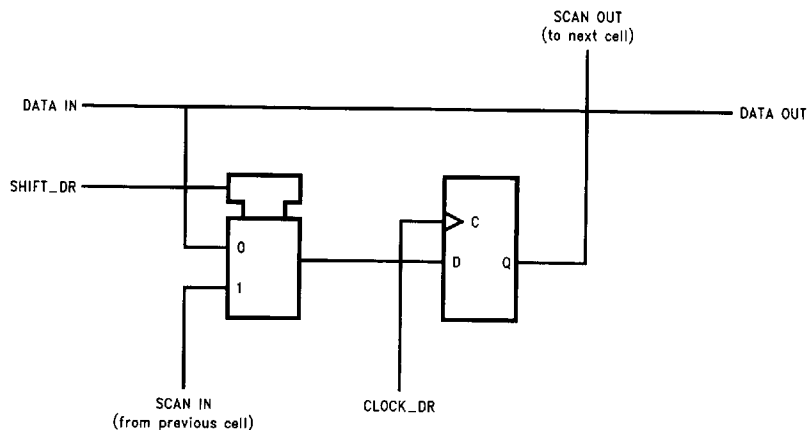


MSB → LSB

Instruction Code	Instruction
00000000	EXTTEST
10000001	SAMPLE/PRELOAD
10000010	CLAMP
00000011	HIGH-Z
01000001	SAMPLE-IN
01000010	SAMPLE-OUT
00100010	EXTTEST-OUT
10101010	IDCODE
11111111	BYPASS
All Other	BYPASS

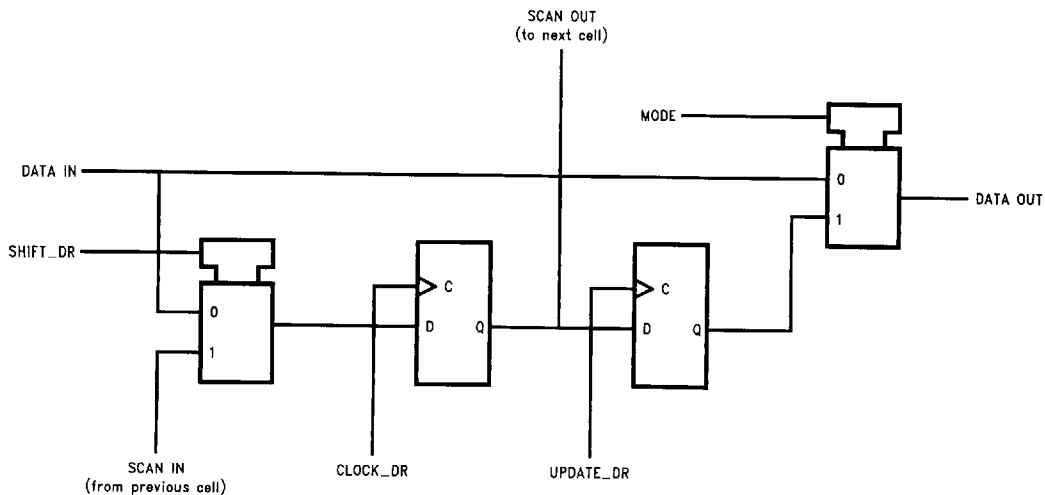
Description of BOUNDARY-SCAN Circuitry (Continued)

Scan Cell TYPE1



TL/F/11545-19

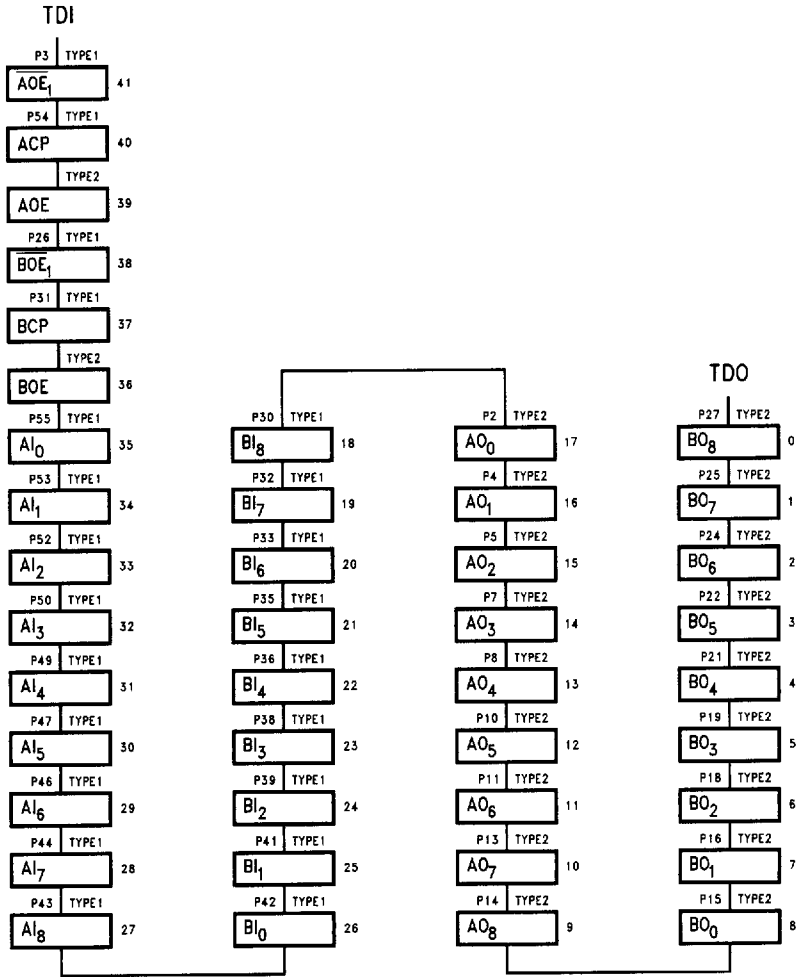
Scan Cell TYPE2



TL/F/11545-20

Description of BOUNDARY-SCAN Circuitry (Continued)

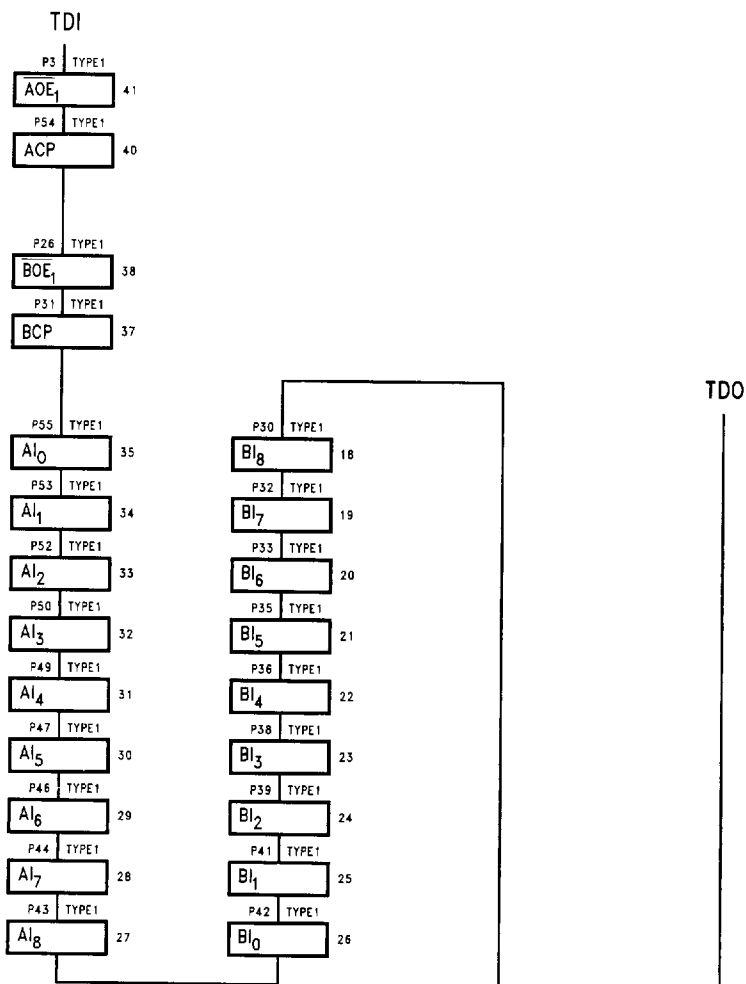
BOUNDARY-SCAN Register SCAN182374A Scan Chain Definition (42 Bits in Length)



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Description of BOUNDARY-SCAN Circuitry (Continued)

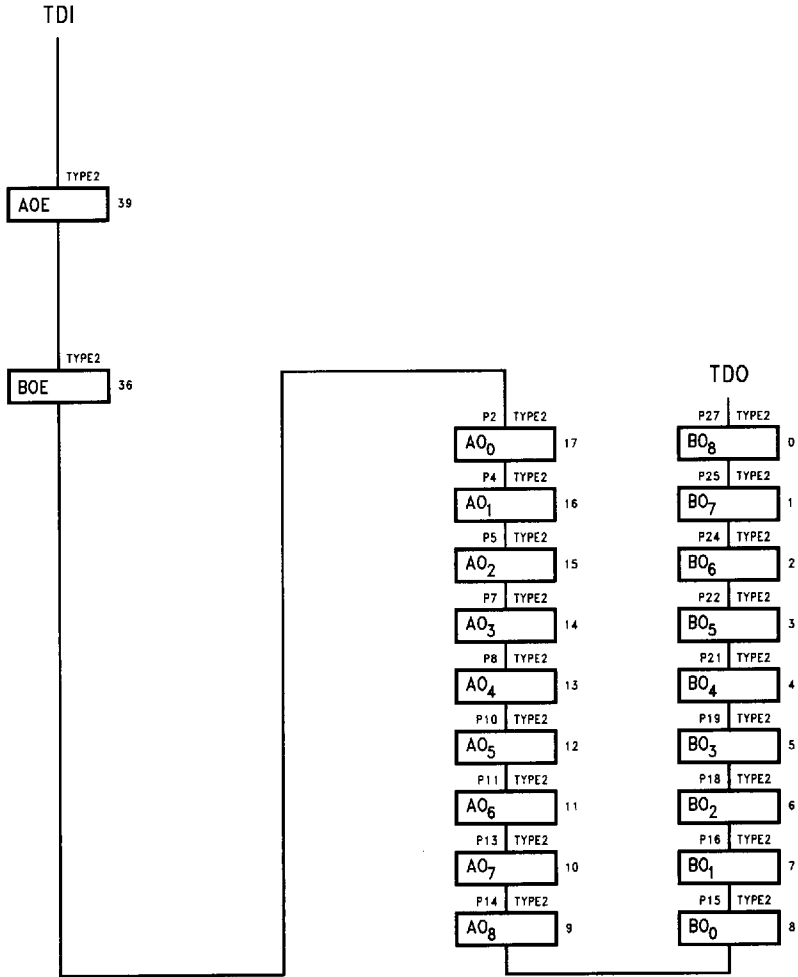
Input BOUNDARY-SCAN Register Scan Chain Definition (22 Bits in Length) When Sample In is Active



TL/F/11545-28

Description of BOUNDARY-SCAN Circuitry (Continued)

Output BOUNDARY-SCAN Register
Scan Chain Definition (20 Bits in Length)
When Sample Out and EXTEST Out are Active



TL/F/11545-30

Description of BOUNDARY-SCAN Circuitry (Continued)

BOUNDARY-SCAN Register Definition Index

Bit No.	Pin Name	Pin No.	Pin Type	Scan Cell Type	
41	\overline{AOE}_1	3	Input	TYPE1	Control Signals
40	ACP	54	Input	TYPE1	
39	AOE		Internal	TYPE2	
38	\overline{BOE}_1	26	Input	TYPE1	
37	BCP	31	Input	TYPE1	
36	BOE		Internal	TYPE2	
35	Al ₀	55	Input	TYPE1	A-in
34	Al ₁	53	Input	TYPE1	
33	Al ₂	52	Input	TYPE1	
32	Al ₃	50	Input	TYPE1	
31	Al ₄	49	Input	TYPE1	
30	Al ₅	47	Input	TYPE1	
29	Al ₆	46	Input	TYPE1	
28	Al ₇	44	Input	TYPE1	
27	Al ₈	43	Input	TYPE1	
26	Bl ₀	42	Input	TYPE1	B-in
25	Bl ₁	41	Input	TYPE1	
24	Bl ₂	39	Input	TYPE1	
23	Bl ₃	38	Input	TYPE1	
22	Bl ₄	36	Input	TYPE1	
21	Bl ₅	35	Input	TYPE1	
20	Bl ₆	33	Input	TYPE1	
19	Bl ₇	32	Input	TYPE1	
18	Bl ₈	30	Input	TYPE1	
17	AO ₀	2	Output	TYPE2	A-out
16	AO ₁	4	Output	TYPE2	
15	AO ₂	5	Output	TYPE2	
14	AO ₃	7	Output	TYPE2	
13	AO ₄	8	Output	TYPE2	
12	AO ₅	10	Output	TYPE2	
11	AO ₆	11	Output	TYPE2	
10	AO ₇	13	Output	TYPE2	
9	AO ₈	14	Output	TYPE2	
8	BO ₀	15	Output	TYPE2	B-out
7	BO ₁	16	Output	TYPE2	
6	BO ₂	18	Output	TYPE2	
5	BO ₃	19	Output	TYPE2	
4	BO ₄	21	Output	TYPE2	
3	BO ₅	22	Output	TYPE2	
2	BO ₆	24	Output	TYPE2	
1	BO ₇	25	Output	TYPE2	
0	BO ₈	27	Output	TYPE2	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	
Ceramic	-55°C to +175°C
Plastic	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State in the HIGH State	-0.5V to +5.5V -0.5V to V _{CC}
Current Applied to Output in LOW State (Max)	Twice the Rated I _{OL} (mA)

DC Latchup Source Current

Commercial	-500 mA
Military	-300 mA

Over Voltage Latchup (I/O)

10V

ESD (HBM) Min.

2000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature

Military	-55°C to +125°C
Commercial	-40°C to +85°C

Supply Voltage

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

Minimum Input Edge Rate

Data Input	($\Delta V/\Delta t$) 50 mV/ns
Enable Input	20 mV/ns

DC Electrical Characteristics

Symbol	Parameter	V _{CC}	Min	Typ	Max	Units	Conditions
V _{IH}	Input HIGH Voltage		2.0			V	Recognized HIGH Signal
V _{IL}	Input LOW Voltage				0.8	V	Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage	Min			-1.2	V	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	Min	2.5			V	I _{OH} = -3 mA
		Mil Min	2.0			V	I _{OH} = -24 mA
		Comm Min	2.0			V	I _{OH} = -32 mA
V _{OL}	Output LOW Voltage	Mil Min		0.8		V	I _{OL} = 12 mA
		Comm Min		0.8		V	I _{OL} = 15 mA
I _{IH}	Input HIGH Current	All Others	Max		5	μA	V _{IN} = 2.7V (Note 1)
			Max		5	μA	V _{IN} = V _{CC}
			TMS, TDI	Max		5	μA
I _{BVI}	Input HIGH Current Breakdown Test	Max		7	μA	V _{IN} = 7.0V	
I _{BVIT}	Input HIGH Current Breakdown Test(I/O)	Max		100	μA	V _{IN} = 5.5V	
I _{IL}	Input LOW Current	All Others	Max		-5	μA	V _{IN} = 0.5V (Note 1)
			Max		-5	μA	V _{IN} = 0.0V
		TMS, TDI	Max		-385	μA	V _{IN} = 0.0V
V _{ID}	Input Leakage Test	0.0	4.75			V	I _{ID} = 1.9 μA All Other Pins Grounded
I _{IH} + I _{OZH}	Output Leakage Current	Max			50	μA	V _{OUT} = 2.7V
I _{IL} + I _{OZL}	Output Leakage Current	Max			-50	μA	V _{OUT} = 0.5V
I _{OZH}	Output Leakage Current	Max			50	μA	V _{OUT} = 2.7V
I _{OZL}	Output Leakage Current	Max			-50	μA	V _{OUT} = 0.5V

Note 1: Guaranteed not tested.

DC Electrical Characteristics (Continued)

Symbol	Parameter	V _{CC}	Min	Typ	Max	Units	Conditions	
I _{OS}	Output Short-Circuit Current	Max	-100		-275	mA	V _{OUT} = 0.0V	
I _{CEX}	Output High Leakage Current	Max			50	μA	V _{OUT} = V _{CC}	
I _{ZZ}	Bus Drainage Test	0.0			100	μA	V _{OUT} = 5.5V All Others Grounded	
I _{CCH}	Power Supply Current	Max			250	μA	V _{OUT} = V _{CC} ; TDI, TMS = V _{CC}	
		Max			1.0	mA	V _{OUT} = V _{CC} ; TDI, TMS = GND	
I _{CCL}	Power Supply Current	Max			65	mA	V _{OUT} = LOW; TDI, TMS = V _{CC}	
		Max			65.8	mA	V _{OUT} = LOW; TDI, TMS = GND	
I _{CCZ}	Power Supply Current	Max			250	μA	TDI, TMS = V _{CC}	
		Max			1.0	mA	TDI, TMS = GND	
I _{CC1}	Additional I _{CC} /Input	All Other Inputs TDI, TMS Inputs	Max			2.9	mA	V _{IN} = V _{CC} - 2.1V
			Max			3	mA	V _{IN} = V _{CC} - 2.1V
I _{CCD}	Dynamic I _{CC}	No Load	Max		0.2	mA/ MHz	Outputs Open One Bit Toggling, 50% Duty Cycle	

AC Electrical Characteristics Normal Operation: See Section 4

Symbol	Parameter	V _{CC} [*] (V)	Military			Commercial			Units	Fig. No.
			T _A = -55°C to +125°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF				
			Min	Typ	Max	Min	Typ	Max		
t _{PLH}	Propagation Delay	5.0				1.4	4.6	6.1	ns	4-1, 2
t _{PHL}	CP to Q					2.1	4.9	6.8		
t _{PLZ}	Disable Time	5.0				1.9	4.6	8.0	ns	4-3, 4
t _{PHZ}						1.8	4.8	8.7		
t _{PZL}	Enable Time	5.0				2.0	6.7	9.4	ns	4-3, 4
t _{PZH}						1.4	6.0	8.2		

*Voltage Range 5.0V ±0.5V

AC Operating Requirements Normal Operation: See Section 4

Symbol	Parameter	V _{CC} [*] (V)	Military			Commercial			Units	Fig. No.
			T _A = -55°C to +125°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF				
			Guaranteed Minimum							
t _S	Setup Time, H or L Data to CP	5.0				2.8		ns	4-5	
t _H	Hold Time, H or L CP to Data	5.0				2.4		ns	4-5	
t _W	CP Pulse Width	5.0				0.0		ns	4-2	
f _{max}	Maximum ACP/BCP Clock Frequency	5.0				50		MHz		

*Voltage Range 5.0 is 5.0V ±0.5V.

AC Electrical Characteristics

Scan Test Operation: See Section 4

Symbol	Parameter	V _{CC} * (V)	Military			Commercial			Units	Fig. No.
			T _A = -55°C to +125°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF				
			Min	Typ	Max	Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay TCK to TDO	5.0				2.9 4.0	5.8 7.3	9.5 11.5	ns	4-8
t _{PLZ} t _{PHZ}	Disable Time TCK to TDO	5.0				1.9 3.0	5.6 7.1	10.0 12.1	ns	4-9, 10
t _{PZL} t _{PZH}	Enable Time TCK to TDO	5.0				4.4 2.7	8.4 6.4	13.2 10.9	ns	4-9, 10
t _{PLH} t _{PHL}	Propagation Delay TCK to Data Out during Update-DR State	5.0				3.4 4.3	6.5 8.1	10.5 12.7	ns	4-8
t _{PLH} t _{PHL}	Propagation Delay TCK to Data Out during Update-IR State	5.0				3.9 4.7	7.8 9.1	12.8 14.5	ns	4-8
t _{PLH} t _{PHL}	Propagation Delay TCK to Data Out during Test Logic Reset State	5.0				4.7 5.6	9.5 10.9	15.6 17.4	ns	4-8
t _{PLZ} t _{PHZ}	Disable Time TCK to Data Out during Update-DR State	5.0				3.2 3.9	7.8 8.5	13.6 14.2	ns	4-9, 10
t _{PLZ} t _{PHZ}	Disable Time TCK to Data Out during Update-IR State	5.0				3.2 3.8	8.6 9.3	15.0 15.6	ns	4-9, 10
t _{PLZ} t _{PHZ}	Disable Time TCK to Data Out during Test Logic Reset State	5.0				4.2 5.0	10.2 11.0	18.0 18.5	ns	4-9, 10
t _{PZL} t _{PZH}	Enable Time TCK to Data Out during Update-DR State	5.0				5.0 3.7	9.6 7.7	15.3 13.0	ns	4-9, 10
t _{PZL} t _{PZH}	Enable Time TCK to Data Out during Update-IR State	5.0				5.3 4.0	10.8 9.0	17.4 15.1	ns	4-9, 10
t _{PZL} t _{PZH}	Enable Time TCK to Data Out during Test Logic Reset State	5.0				6.2 4.7	12.6 10.7	20.4 18.1	ns	4-9, 10

*Voltage Range 5.0V ±0.5V

AC Operating Requirements

Scan Test Operation: See Section 4

Symbol	Parameter	V _{CC} * (V)	Military	Commercial	Units	Fig. No.
			T _A = -55°C to +125°C C _L = 50 pF	T _A = -40°C to +85°C C _L = 50 pF		
			Guaranteed Minimum			
t _S	Setup Time Data to TCK (Note 2)	5.0		2.7	ns	4-11
t _H	Hold Time Data to TCK (Note 2)	5.0		3.1	ns	4-11
t _S	Setup Time, H or L AOE ₁ , BOE ₁ to TCK (Note 1)	5.0		5.0	ns	4-11
t _H	Hold Time, H or L TCK to AOE ₁ , BOE ₁ (Note 1)	5.0		1.8	ns	4-11
t _S	Setup Time, H or L Internal AOE, BOE to TCK (Note 3)	5.0		3.6	ns	4-11
t _H	Hold Time, H or L TCK to Internal AOE, BOE (Note 3)	5.0		2.1	ns	4-11
t _S	Setup Time ACP, BCP (Note 4) to TCK	5.0		3.4	ns	4-11
t _H	Hold Time TCK to ACP, BCP (Note 4)	5.0		1.8	ns	4-11
t _S	Setup Time, H or L TMS to TCK	5.0		8.7	ns	4-11
t _H	Hold Time, H or L TCK to TMS	5.0		1.8	ns	4-11
t _S	Setup Time, H or L TDI to TCK	5.0		6.4	ns	4-11
t _H	Hold Time, H or L TCK to TDI	5.0		3.2	ns	4-11
t _W	Pulse Width TCK	H L	5.0	8.2 11.2	ns	4-12
f _{max}	Maximum TCK Clock Frequency	5.0		50	MHz	
t _{PU}	Wait Time, Power Up to TCK	5.0		100	ns	
t _{DN}	Power Down Delay	0.0		100	ms	

*Voltage Range 5.0V ±0.5V

All Input Timing Delays involving TCK are measured from the rising edge of TCK.

Note 1: Timing pertains to BSR 38 and 41 only.**Note 2:** This delay represents the timing relationship between the data input and TCK at the associated scan cells numbered 0-8, 9-17, 18-26 and 27-35.**Note 3:** This delay represents the timing relationship between AOE/BOE and TCK for scan cells 36 and 39 only.**Note 4:** Timing pertains to BSR 37 and 40 only.

Capacitance

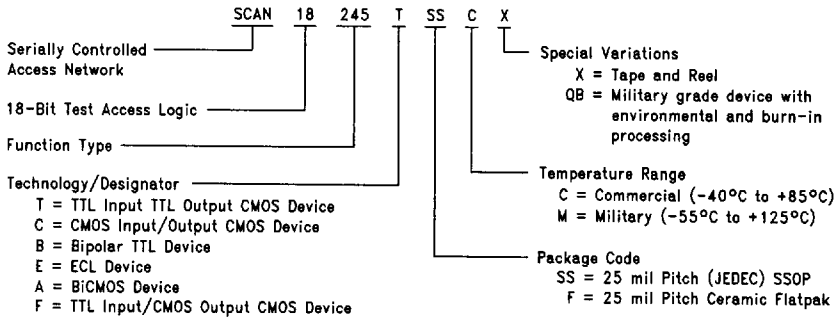
T_A = 25°C

Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	5.8	pF	V _{CC} = 0.0V
C _{OUT} (Note 1)	Output Capacitance	13.8	pF	V _{CC} = 5.0V

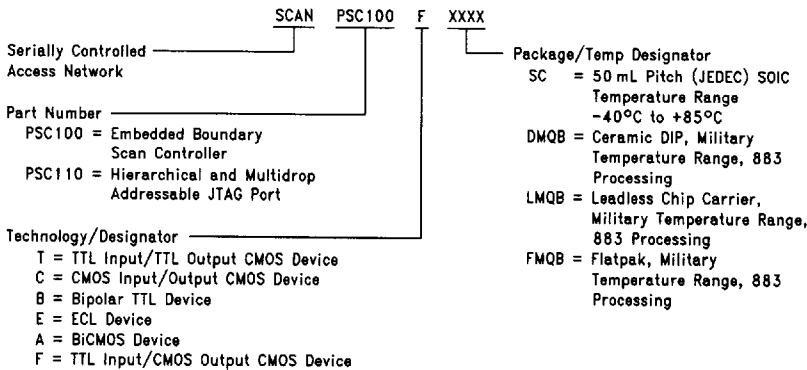
Note 1: C_{OUT} is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

Ordering Information and Physical Dimensions

Ordering Information



TL/F/11596-9



TL/F/11596-10

SSOP Package Thermal Information

THERMAL RESISTANCE FOR SSOP PACKAGES

Package	Paddle Dimensions (mils)	θ_{JA} 0 LFPM (°C/W)	θ_{JA} 225 LFPM (°C/W)	θ_{JA} 500 LFPM (°C/W)	θ_{JA} 900 LFPM (°C/W)	θ_{JC}
20LD SSOP	110 x 144	127.0	99.4	90.1	78.5	N/A
24LD SSOP	98 x 106	117.0	91.4	82.7	73.5	N/A
24LD SSOP	120 x 150	100.8	81.3	72.1	65.7	25.7
48LD SSOP	190 x 190	75.5	58.0	51.5	44.0	21.5
56LD SSOP	190 x 190	67.8	53.0	47.4	42.1	18.5

THERMAL RESISTANCES FOR THE MILITARY FLATPAK PACKAGES

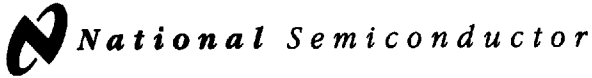
Package	Cavity Dimensions (mils)	θ_{JA} 0 LFPM (°C/W)	θ_{JA} 225 LFPM (°C/W)	θ_{JA} 500 LFPM (°C/W)	θ_{JA} 900 LFPM (°C/W)	θ_{JC}
48LD	250 x 250	74.4	58.1	50.0	43.9	6.6
56LD	250 x 250	59.8	47.9	39.0	35.1	3.4


Dry Pack

Dry Pack is moisture proof packing that is used to store SSOP devices to reduce the susceptibility of the "popcorn effect". Humidity collects inside the package by seeping through the plastic. If moisture is inside the device when the unit goes through a solder machine, the heat quickly changes the moisture to steam, and the pressurized steam pops open the package . . . thus the popcorn effect.

The Dry Pack bag is hermetically sealed and contains a small bag of desiccant which further helps to reduce moisture. All of the SCAN 56-pin SSOP devices will be shipped in Dry Pack bags. Included with the devices will be the following warning label and instructions for re bake:

Dry Pack Warning Label for Surface Mount Packages






CAUTION

This Bag Contains

MOISTURE SENSITIVE DEVICES



1. Shelf life in sealed bag: 24 months at <math><40^{\circ}\text{C}</math> and <math><90\%</math> Relative Humidity (RH).
2. Upon opening this bag, devices to be subjected to I.R., V.P.R. or equivalent process must be:
 - a. Mounted within 48 hours at factory conditions of <math><30^{\circ}\text{C}/60\%</math> RH, or
 - b. Stored at <math><10\%</math> RH.
3. Devices require baking, before mounting, if:
 - a. Humidity Indicator Card is >20% when read at $23^{\circ}\text{C} \pm 5^{\circ}\text{C}$.
 - b. 2a or 2b are not met.
4. If baking is required, devices may be baked for:
 - a. 19 hours at $40^{\circ}\text{C} + 5^{\circ}\text{C}/ - 0^{\circ}\text{C}$ and <math><5\%</math> RH for low temperature device containers, or
 - b. 8 hours at $125^{\circ}\text{C} \pm 5^{\circ}\text{C}$ for high temperature device containers.

Dry-Pack Seal Date: _____

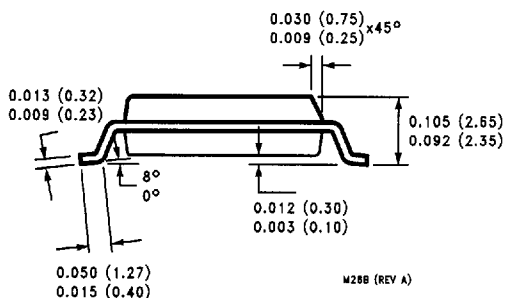
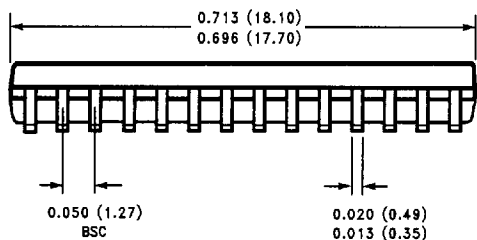
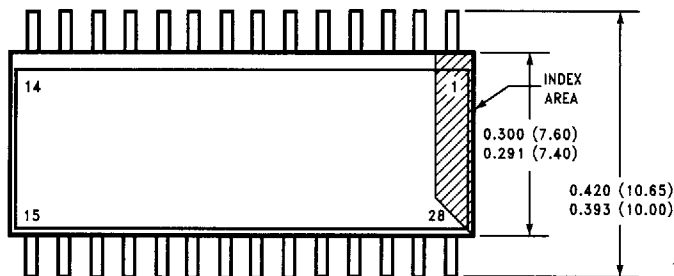
(IF BLANK, SEE BAR CODE LABEL)

BAG SN 045317 MFR LOT No. C32729

Please follow these instructions carefully to avoid the popcorn effect.

28 Lead (0.300" Wide) Molded Small Outline Package, JEDEC NS Package Number M28B

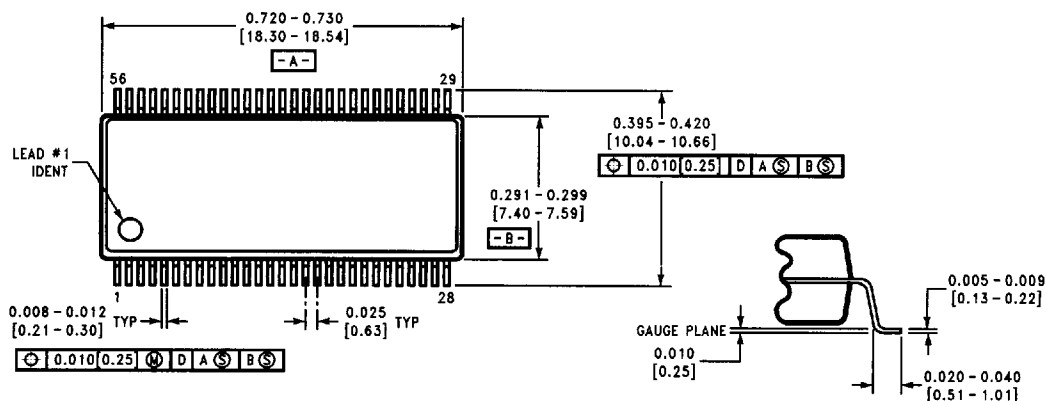
All dimensions are in inches (millimeters)



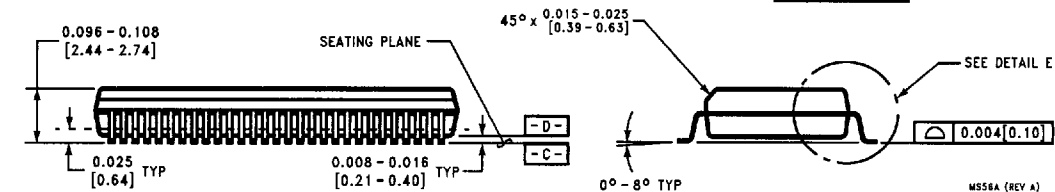
M28B (REV A)

56 Lead (0.300" Wide) Molded Shrink Small Outline Package, JEDEC NS Package Number MS56A

All dimensions are in inches [millimeters]

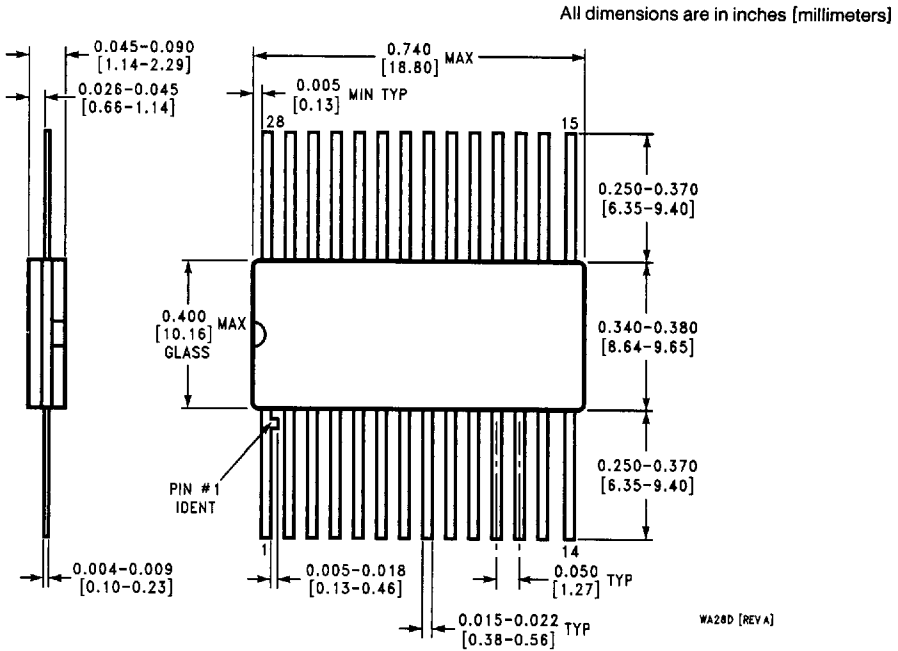


DETAIL E TYP



MS56A (REV A)

28 Lead Cerpack NS Package Number WA28D



56 Lead Cerpack NS Package Number WA56A

