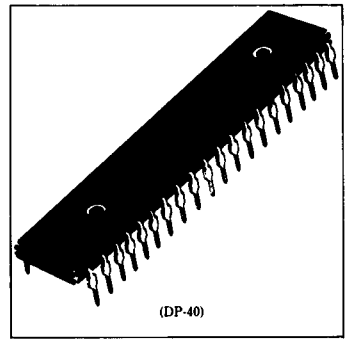
# HN62201P — Preliminary

## 65536-word x 16-bit CMOS Mask Programmable Read Only Memory

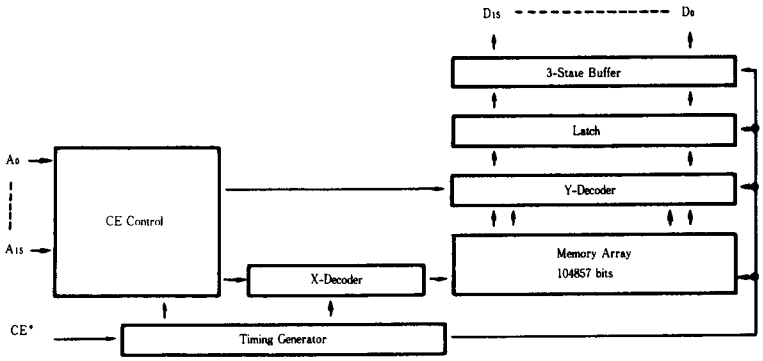
### ■ FEATURES

- Single +5V Power Supply
- Three-state Data Output for OR-ties
- Mask Programmable Chip Enable
- TTL Compatible
- Maximum Access Time: 3.5 μs
- Low Power Standby and Low Power Operation; Standby 50 μW (typ.), Operation 20 mW (typ.)



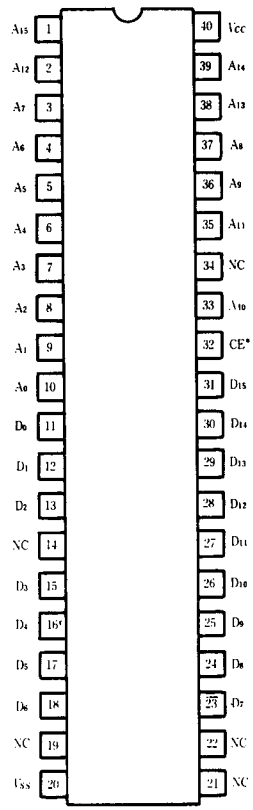
(DP-40)

### ■BLOCK DIAGRAM




* Active level defined by the user

### ■PIN ARRANGEMENT




(Top View)

* Mask Programmable

### ■ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage* | $V_{CC}$ | −0.3 to +7.0 | V |
| All Input and output Voltage* | $V_T$ | −0.3 to $V_{CC}$ | V |
| Operating Temperature Range | $T_{opr}$ | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | −55 to +125 | °C |
| Storage Temperature Range (Under Bias) | $T_{bias}$ | −20 to +85 | °C |

* with respect to $V_{SS}$

NOTES: The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications

## ■ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V\pm10\%$, $V_{SS}=0V$, $T_a=0\sim+70°C$)

| Item | | Symbol | Test Condition | | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input Voltage | | $V_{IH}$ | | | 2.2 | – | $V_{CC}$ | V |
| | | $V_{IL}$ | | | −0.3 | – | 0.8 | V |
| Output Voltage | | $V_{OH}$ | $I_{OH}=-100\mu A$ | | 2.4 | – | – | V |
| | | $V_{OL}$ | $I_{OL}=1.6mA$ | | – | – | 0.4 | V |
| Input Leakage Current | | $I_{LI}$ | $V_{IN}=0$ to 5.5V | | – | – | 2.5 | $\mu A$ |
| Output Leakage Current | | $I_{LOH}$ | CE=0.8V, $\overline{CE}$=2.2V | $V_{out}=2.4V$ | – | – | 10 | $\mu A$ |
| | | $I_{LOL}$ | | $V_{out}=0.4V$ | – | – | 10 | $\mu A$ |
| Supply Current | Active | $I_{CC}$ | $V_{CC}=5.5V$, $I_{out}=0mA$, $t_{RC}=4\mu s$ | | – | – | 10 | mA |
| | Standby | $I_{SB}$ | $V_{CC}=5.5V$, $\overline{CE}\geq V_{CC}-0.2V$, CE≦0.2V | | – | – | 50 | $\mu A$ |
| Input Capacitance | | $C_{in}$* | $V_{in}=0V$, $f$=1MHz, $T_a=25°C$ | | – | – | 10 | PF |
| Output Capacitance | | $C_{out}$* | | | – | – | 15 | PF |

* This parameter is sampled and not 100% tested.

## ■RECOMMENDED AC OPERATING CONDITIONS (READ SEQUENCE)

| Item | Symbol | min | max | Unit |
|---|---|---|---|---|
| Read Cycle Time | $t_{RC}$ | 4.0 | – | $\mu s$ |
| Address Access Time | $t_{AACC}$ | – | 3.5 | $\mu s$ |
| Chip Enable Access Time | $t_{EACC}$ | – | 3.0 | $\mu s$ |
| Data Hold Time from Address | $t_{DF}$* | – | 0.5 | $\mu s$ |
| Address Setup Time | $t_{AS}$ | 0.5 | – | $\mu s$ |
| Address Hold Time | $t_{AH}$ | 0 | – | $\mu s$ |
| Chip Enable ON Time | $t_{\overline{CE}}$ | 3.0 | – | $\mu s$ |
| Chip Enable OFF Time | $t_{CE}$ | 0.5 | – | $\mu s$ |

* $t_{DF}$ defines the time at which the output achieves the open circuit condition and is not reference to output voltage levels.

### ● AC TEST LOAD