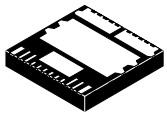
Document order number MC33982/D
Rev 3, 01/2003

Preliminary Information

Intelligent High Current Self-Protected Silicon High-Side Switch

33982

INTELLIGENT SWITCH
2 mΩ



FC SUFFIX
PLASTIC PACKAGE
CASE 1402
PQFN

The 33982 is a self-protected silicon 2 mΩ high-side switch used to replace electromechanical relays, fuses, and discrete devices in power management applications. The 33982 is designed for harsh environments, and it includes self-recovery features. The device is suitable for loads with high inrush current, as well as motors and all types of resistive and inductive loads.

Programming, control, and diagnostics are implemented via the Serial Peripheral Interface (SPI). A dedicated parallel input is available for alternate and Pulse Width Modulation (PWM) control of the output. SPI programmable fault trip thresholds allow the device to be adjusted for optimal performance in the application.

The 33982 is packaged in a power enhanced 12 x 12 PQFN package with exposed tabs.

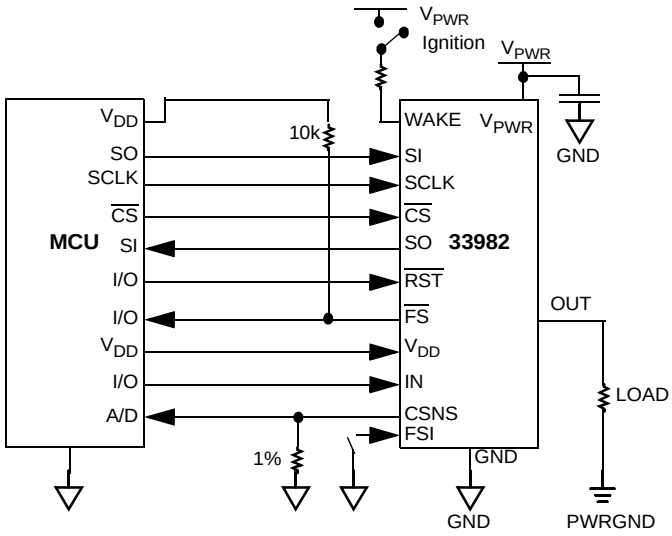
Features:

- Single 2.0 mΩ Max High-Side Switch with Parallel Input or SPI Control
- 6.0 V to 27 V Operating Voltage with Standby Currents < 5.0 µA
- Output Current Monitoring Output with two SPI Selectable Current Ratios
- SPI Control of: Overcurrent Limit, Overcurrent Fault Blanking Time, Output-OFF Open Load Detection, Output ON/OFF Control, Watchdog Timeout, slew rates and Fault Status Reporting
- SPI Status Reporting of: Overcurrent, Open and Shorted Loads, Over Temperature, Under and Overvoltage Shutdown, Fail-Safe Pin Status, and Program Status.
- Enhanced 16 V Reverse Polarity V_{PWR} Protection

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
PC33982FC/R2	- 40°C to +125°C	PQFN

33982 Simplified Application Schematic



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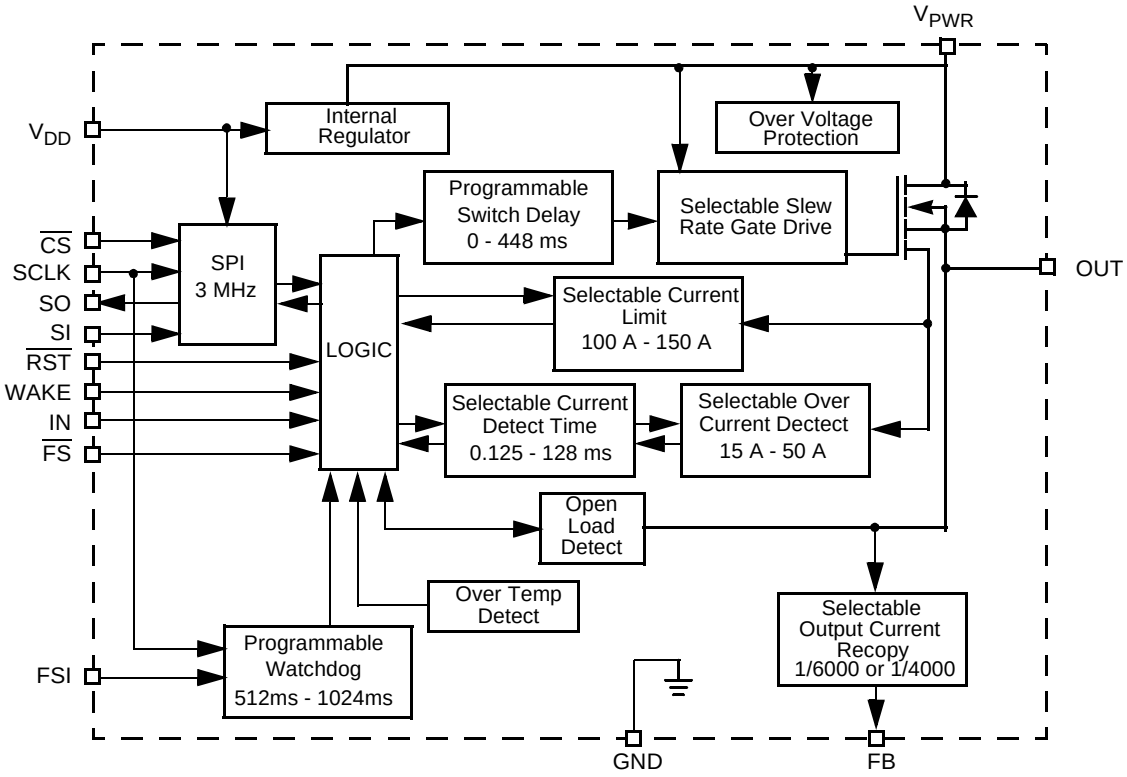
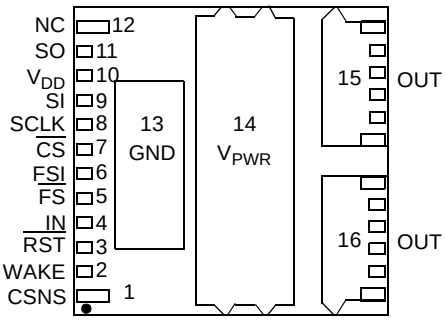


Figure 1. 33982 Internal Block Diagram



PIN FUNCTION DESCRIPTION

Pin	Pin Name	Description
1	CSNS	**Output Current Monitoring.** This pin is used to output a current proportional to the high-side output current and used externally to generate a ground referenced voltage for the microcontroller to monitor output current.
2	WAKE	**WAKE.** This pin is used to input a logic [1] signal so as to enable the Watchdog timer function. An internal clamp protects this pin from high damaging voltages when the output is current limited with an external resistor. This input has an internal passive pull-down.
3	$\overline{RST}$	**Reset.** This is an input used to initialize the device configuration and fault registers, as well as place the device in a low current sleep mode. The pin also starts the Watchdog timer when transitioning from logic LOW-to-logic HIGH. This pin should not be allowed to be logic HIGH until V_{DD} is in regulation. This pin has an internal passiv pull down.
4	IN	**Serial Input.** The Input pin is used to directly control the output. This input has an internal active pull-down and requires CMOS logic levels. This input may be configured via SPI.
5	$\overline{FS}$	**Fault Status.** This is an open drain configured output requiring an external pull-up resistor to V_{DD} for fault reporting. A device fault condition is detected, this pin is active LOW. Specific device diagnostic faults are reported via the SPI SO pin.
6	FSI	**Fail-Safe Input.** The level of this pin determines the state of the output after a Watchdog timeout occurs. This pin incorporates and internal pull-up. If the FSI pin is left to float up to a logic [1] level, the output will turn-ON when in the fail-safe state. When the FSI pin is connected to GND, the Watchdog circuit and fail-safe operation are disabled.
7	$\overline{CS}$	**Chip Select.** This is an input pin connected to a chip select output of a system microcontroller. The microcontroller determines which device is addressed (selected) to receive data by pulling the $\overline{CS}$ pin of the selected device logic LOW, enabling SPI communication with the device. Other *unselected* devices on the serial link having their $\overline{CS}$ pins pulled-up logic HIGH disregard the SPI communication data sent.
8	SCLK	**Serial Clock.** This is an input pin connected to the master microcontroller providing the required bit shift clock for SPI communication. It transitions one time per bit transferred at an operating frequency, f_{SPI}, defined by the communication interface. **See** the SPI Interface Characteristics table. The 50 percent duty cycle CMOS level serial clock signal is idle between command transfers. The signal is used to shift data into and out-of the device. See operational description of SPI.
9	SI	**Serial Input.** This is a command data input pin connected to the SPI Serial Data Output of the master microcontroller or to the SO pin of the previous device of a daisy chain of devices. The input requires CMOS logic level signals and incorporates an internal active pull-down. Device control is facilitated by the input's receiving the MSB first of a serial 8-bit control command. The master ensures data is available upon the falling edge of SCLK. The logic state of SI present upon the rising edge of SCLK loads that bit command into the internal command shift register.

PIN FUNCTION DESCRIPTION

Pin	Pin Name	Description
10	V_{DD}	**Digital Drain Voltage (Power).** This is an external voltage input pin used to supply power to the SPI circuit. In the event V_{DD} is lost, an internal supply provides power to a portion of the logic, ensuring limited functionality of the device.
11	SO	**Serial Output.** This is an output pin connected to the SPI Serial Data Input pin of the master microcontroller or to the SI pin of the next device of a daisy chain of devices. This output will remain tri-stated (high impedance OFF condition) so long as the $\overline{CS}$ pin of the device is logic HIGH. SO is only active when the $\overline{CS}$ pin of the device is asserted logic LOW. The generated SO output signals are CMOS logic levels. SO output data is available on the falling edge of SCLK and transitions immediately on the rising edge of SCLK. Serial output data provides status information for each bit assigned following an MSB first-in-first-out protocol when the device is addressed. Fault bit assignments for return data follow OD7 through OD0 are output status bits for message bits 7 through 0. See **SPI** operational details, command verification, and daisy chain operation.
12	NC	**No Connect.** No internal connection to this pin.
13	GND	**Ground.** This pin is the ground for the logic and analog circuitry of the device.
14	V_{PWR}	**Positive Power Supply.** This pin connects to the positive power supply and is the source input of operational power for the device. The V_{PWR} pin is a backside surface mount tab of the package.
15 and 16	OUT	**Output.** Protected high-side power output to the load. All pins of output have to be connected in parallel for operation according to this specification.

MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
Operating Voltage Range Steady-State	$V_{PWR(SS)}$	-16 to 41	V
Input Voltage (Note 1)	V_{IN}, $\overline{RST}$, FSI	-0.3 to 7.0	V
WAKE Input Clamp Current	$I_{CL(WAKE)}$	2.5	mA
CSNS Input Clamp Current	$I_{CL(CSNS)}$	2.5	mA
Output Current (Note 2)	I_{OUTt}	60	A
Output Clamp Energy (Note 3)	E_{CL}	TBD	J
Storage Temperature	T_{STG}	-55° to 150°	°C
Operating Junction Temperature	T_J	-40° to 150°	°C
Junction to Case Thermal Resistance	Θ_{JC}	<1.0	C/W
Junction to Ambient Thermal Resistance	Θ_{JA}	—	C/W
ESD Voltage Human Body Model (Note 4) Machine Model (Note 5)	 V_{ESD1} V_{ESD2}	 2000 200	V

Notes:

1. Exceeding voltage limits on $\overline{RST}$, IN, or FSI pins may cause a malfunction or permanent damage to the device.
2. Continuous high-side output current rating so long as maximum junction temperature is not exceeded. Calculation of maximum output current using package thermal resistance is required .
3. Active clamp energy using single pulse method.
4. E_{SD1} testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} - 1500 Ω).
5. E_{SD2} testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} - 0 Ω) and in accordance with the system module specification with a capacitor > 0.01 µF connected form OUT to GND.

STATIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions 4.5 V ≤ V_{DD} ≤ 5.5 V, 6 V ≤ V_{PWR} ≤ 27 V, -40°C ≤ T_J ≤ 150°C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Power Input

Characteristic	Symbol	Min	Typ	Max	Unit
Battery Supply Voltage Range Full Operational	V_{PWR}	 6.0	 —	 27	V
V_{PWR} Operating Supply Current (Measured with Output ON, I_{OUT} = 0)	$I_{PWR(on)}$	—	—	20	mA
V_{PWR} Supply Current (Output OFF, Open Load Detect Disabled, WAKE > 0.7 V_{DD}, $\overline{RST}$ = $V_{LOGIC\ HIGH}$)	$I_{PWR(sby)}$	—	—	5.0	mA
Sleep State Supply Current (V_{PWR} < 14 V, $\overline{RST}$ < 0.5 V, WAKE < 0.5 V) T_J= 25° C T_J = 85° C	$I_{PWR(sleep)}$	 — —	 — —	 10 50	µA
V_{DD} Supply Voltage	$V_{DD(on)}$	4.5	5.0	5.5	V
V_{DD} Supply Current	$I_{DD(on)}$			2.0	mA
V_{DD} Sleep State Current	$I_{DD(sleep)}$			5.0	µA
Over Voltage Shutdown	$V_{PWR(on)}$	28	32	36	V
Over Voltage Shutdown Hysteresis	$V_{PWR(ouhys)}$	0.2	0.8	1.5	V
Under Voltage Output Shutdown (Note 6)	$V_{P(uv)}$	5.0	5.5	6.0	V
Under Voltage Power-ON Reset	$V_{P(und)}$	—	—	5.0	V

Notes:

6. Output will automatically recover to instructed state when V_{PWR} voltage is restored to normal so long as the V_{PWR} degradation level did not go below the under voltage power-on reset threshold. This applies to all internal device logic that is supplied by VPWR and assumes that the external Vdd supply is within specification.

STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions 4.5 V ≤ V_{DD} ≤ 5.5 V, 6 V ≤ V_{PWR} ≤ 27 V, -40°C ≤ T_J ≤ 150°C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Output

Characteristic	Symbol	Min	Typ	Max	Unit
Output Drain-to-Source ON Resistance	$R_{DS(on)25}$				mΩ
(I_{OUT} = 30 A, T_J = 25°C)					
V_{PWR} = 6.0 V		—	—	3.0	
V_{PWR} = 9.0 V		—	—	2.0	
V_{PWR} = 13 V		—	—	2.0	
Output Drain-to-Source ON Resistance	$R_{DS(on)150}$				mΩ
(I_{OUT} = 30 A, T_J = 150°C)					
V_{PWR} = 6.0 V		—	—	5.1	
V_{PWR} = 9.0 V		—	—	3.4	
V_{PWR} = 13 V		—	—	3.4	
Output Source-to-Drain ON Resistance (Note 7)	$R_{SD(on)}$	—	—	4.0	mΩ
(I_{OUT} = 30 A, T_J = 25°C) V_{PWR}= -12 V					
Output Overcurrent High Detection Levels (9.0 V ≤ V_{PWR} ≤ 16 V)					A
SOCH = 0	I_{OCH0}	120	150	180	
SOCH = 1	I_{OCH1}	80	100	120	
Over current Low Detection Levels (SOCLA[2:0])					
(000)	I_{OCL0}	41	50	59	A
(001)	I_{OCL1}	36	45	54	
(010)	I_{OCL2}	32	40	48	
(011)	I_{OCL3}	29	35	41	
(100)	I_{OCL4}	25	30	35	
(101)	I_{OCL5}	20	25	30	
(110)	I_{OCL6}	16	20	24	
(111)	I_{OCL7}	12	15	18	
Current Sense Ratio (9.0 V ≤ V_{PWR} ≤ 16 V CSNS ≤ 4.5 V)					
DICR D2 =0	CSR0	—	1/40000	—	
DICR D2=1	CSR1	—	1/6000	—	
Current Sense Ratio (C_{SR0}) Accuracy					
Output Current:					
10 A		-20	—	20	%
20 A		-14	—	14	
25 A		-13	—	13	
30 A		-12	—	12	
40 A		-13	—	13	
50 A		-13	—	13	

Current Sense Ratio (C_{SR1}) Accuracy Output Current: 10 A 20 A 25 A 30 A 40 A 50 A		 TBD TBD TBD TBD TBD TBD	 — — — — — —	 TBD TBD TBD TBD TBD TBD	%
Maximum Current Sense Clamp Voltage I_{CSNS} = 15 mA	$V_{CL(maxsns)}$	4.5	6.0	7.0	V
Open Load Detect Current (Note 8)	I_{OLDC}	30	—	100	µA
Output Fault Detect Threshold Output Programmed OFF	$V_{OLD(thres)}$	2.0	3.0	4.0	V
Output Negative Clamp Voltage 0.5A ≤ = I_{OUT} ≤ = 2.0 A, Output OFF	V_{CL}	-20	—	—	V
Over Temperature Shutdown (Output OFF) (Note 9) (T_A = 125° C)	T_{SD}	160	175	190	°C
Over Temperature Shutdown Hysteresis (Note 9)	$TSD_{(hys)}$	5.0	—	20	°C

Notes:

7. Source-Drain ON Resistance (Reverse Drain-to-Source ON Resistance) with negative polarity V_{PWR}.
8. Output OFF Open Load Detect Current is the current required to flow through the load for the purpose of detecting the existence of an open load condition when the specific output is commanded OFF.
9. Guaranteed by process monitor. Not production tested.

STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions 4.5 V ≤ V_{DD} ≤ 5.5 V, 6 V ≤ V_{PWR} ≤ 27 V, -40°C ≤ T_J ≤ 150°C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Control Interface

Characteristic	Symbol	Min	Typ	Max	Unit
Input Logic High Voltage (Note 10)	V_{IH}	0.7V_{DD}	—	—	V
Input Logic Low Voltage (Note 10)	V_{IL}	—	—	0.2V_{DD}	V
Input Logic Voltage Hysteresis (Note 10)	$V_{IN(hys)}$	100	350	750	mV
Input Logic Pull-Down Current (SCLK, IN,SI)	I_{DWN}	5.0	—	20	µA
$\overline{RST}$ Input Voltage Range	V_{RST}	4.5	5.0	5.5	V
SO, $\overline{FS}$ Tri-State Capacitance (Note 11)	C_{SO}	—	—	20	pF
Input Logic Pull-Down Resistor ($\overline{RST}$) and WAKE	I_{DWN}	100	200	400	kΩ
Input Capacitance (Note 12)	C_{IN}	—	4.0	12	pF
Wake Input Clamp Voltage ($I_{CL(WAKE)}$<2.5 mA) (Note 13)	$V_{CL(WAKE)}$	7.0	—	14	V
Wake Input Forward Voltage ($I_{CL(WAKE)}$ = -2.5 mA)	$V_{F(WAKE)}$	-2.0	—	-0.3	V
SO High State Output Voltage (I_{OH} = 1.0 mA)	V_{SOH}	0.8 V_{DD}	—	—	V
$\overline{FS}$, SO Low State Output Voltage (I_{OL} = -1.6 mA)	V_{SOL}	—	0.2	0.4	V
SO Tri-State Leakage Current ($\overline{CS}$ ≥ 0.7V_{DD})	$I_{SO(leak)}$	-5.0	0	5.0	µA
Input Logic Pull-Up Current ($\overline{CS}$, FSI, Vin >0.7 V_{DD}) (Note 14)	I_{UP}	5.0	—	20	µA

Notes:

10. Upper and lower logic threshold voltage range applies to SI, $\overline{CS}$, SCLK, $\overline{RST}$, IN and WAKE input signals. The WAKE and $\overline{RST}$ signals may be supplied by a derived voltage reference to V_{PWR}.
11. Parameter is guaranteed by process monitor but is not production tested.
12. Input capacitance of SI, $\overline{CS}$, SCLK, $\overline{RST}$, and WAKE. This parameter is guaranteed by process monitor; but is not production tested.
13. The current must be limited by a series resistance when using voltages > 7.0 V.
14. Pull-up current is with $\overline{CS}$ OPEN. $\overline{CS}$ has an active internal pull-up to V_{DD}.

DYNAMIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions 4.5 V ≤ V_{DD} ≤ 5.5 V, 6 V ≤ V_{PWR} ≤ 27 V, -40°C ≤ T_J ≤ 150°C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Power Output Timing

Characteristic	Symbol	Min	Typ	Max	Unit
Output Rising Slow Slew Rate A (Note 15) (DICR D3 = 0) 6 V< V_{PWR} <9 V 9 V< V_{PWR} <16 V 16 V< V_{PWR} <27 V	SR_{rA_slow}	—	0.6	—	V/µs
Output Rising Slow Slew Rate B (Note 17) (DICR D3 = 0) 6 V< V_{PWR} <9 V 9 V< V_{PWR} <16 V 16 V< V_{PWR} <27 V	SR_{RB_SLOW}	—	0.05	—	V/µs
Output Rising Fast Slew Rate A (Note 15) (DICR D3 = 1) 6 V< V_{PWR} <9 V 9 V< V_{PWR} <16 V 16 V< V_{PWR} <27 V	SR_{RA_FAST}	—	2.0	—	V/µs
Output Rising Fast Slew Rate B(Note 16) (DICR D3 = 1) 6 V< V_{PWR} <9 V 9 V< V_{PWR} <16 V 16 V< V_{PWR} <27 V	SR_{RB_FAST}	—	0.2	—	V/µs
Output Falling Slow Slew Rate A (Note 15) (DICR D3 = 0) 6 V< V_{PWR} <9 V 9 V< V_{PWR} <16 V 16 V< V_{PWR} <27 V	SR_{RA_SLOW}	—	0.6	—	V/µs
Output Falling Slow Slew Rate B (Note 16) (DICR D3 = 0) 6 V< V_{PWR} <9 V 9 V< V_{PWR} <16 V 16 V< V_{PWR} <27 V	SR_{RB_SLOW}	—	0.05	—	V/µs
Output Falling Fast Slew Rate A (Note 15) (DICR D3 = 1) 6 V< V_{PWR} <9 V 9 V< V_{PWR} <16 V 16 V< V_{PWR} <27 V	SR_{RA_FAST}	—	2.0	—	V/µs
Output Falling Fast Slew Rate B (Note 16) (DICR D3=1) 6 V< V_{PWR} <9 V 9 V< V_{PWR} <16 V 16 V< V_{PWR} <27 V	SR_{RB_FAST}	—	0.2	—	V/µs

DYNAMIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions 4.5 V ≤ V_{DD} ≤ 5.5 V, 6 V ≤ V_{PWR} ≤ 27 V, -40°C ≤ T_J ≤ 150°C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Power Output Timing

Characteristic	Symbol	Min	Typ	Max	Unit
Output Turn-ON Delay Time (Note 17)	$t_{dly(on)}$	1.0	15	100	µs
Output Turn-OFF Delay Time (Note 18)	$t_{dly(off)}$	20	80	200	µs
Direct Input Switching Frequency	f_{PWM}	—	300	—	Hz
Over Current Detect Blank (OCTL [1:0]) Time					
00	t_{OCL0}	108	155	202	ms
01	t_{OCL1}	6.7	9.7	12.7	
10	t_{OCL2}	0.84	1.2	1.6	
11	t_{OCL3}	0.10	0.15	0.2	
Over Current Hi Detect Blank Time	t_{ILB}	1	10	20	µs
$\overline{CS}$ to CSNS Valid Time	CNS_{VAL}	—	—	10	µs
Output Switching Delay Time (OSDR [2:0])					
000	t_{OSD0}		0		ms
001	t_{OSD1}	44.8	64	83.2	
010	t_{OSD2}	89.6	128	166.4	
011	t_{OSD3}	134.4	192	250	
100	t_{OSD4}	179	256	333	
101	t_{OSD5}	224	320	416	
110	t_{OSD6}	268	384	500	
111		313	448	583	
Watchdog Timeout (Note 19) (WD[1:0])					ms
00	t_{WDTO0}	496	620	806	
01	t_{WDTO1}	248	310	403	
10	t_{WDTO2}	2000	2500	3250	
11	t_{WDTO3}	1000	1250	1625	

Notes:

15. Rise and Fall Slew Rates A measured across a 5.0 Ω resistive load at HS output = 0.5V to V_{PWR}-3 V. These parameters are guaranteed by process monitoring.
16. Rise and Fall Slow Slew Rates B measured across a 5.0 Ω resistive load at HS output = 0.5V to V_{PWR}-3 V. These parameters are guaranteed by process monitoring.
17. Turn-ON Delay time measured from rising edge of any signal (IN, SCLK, $\overline{CS}$) that would turn the output ON to Vout=0.5V with RL=5 Ohm resistive load.
18. Turn-OFF delay time measured from falling edge of any signal (IN, SCLK, $\overline{CS}$) that would turn the output OFF to Vout=VPWR-0.5V with RL=5 Ohm resistive load.
19. Watchdog Timeout delay measured from the rising edge of WAKE to $\overline{RST}$ from a sleep state condition, to output turn-ON with the output driven OFF and FSI floating. The values shown are for WDR setting of [00]. The accuracy of t_{WD} is consistent for all configured watchdog timeouts.

SPI INTERFACE CHARACTERISTICS

Characteristics noted under conditions 4.5 V ≤ V_{DD} ≤ 5.5 V, 6 V ≤ V_{PWR} ≤ 27 V, -40°C ≤ T_J ≤ 150°C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Recommended Frequency of SPI Operation	f_{SPI}	—	—	3.0	MHz
Required Low State Duration for $\overline{RST}$ (Note 20)	t_{WRST}	—	50	167	nS
Rising Edge of $\overline{CS}$ to Falling Edge of $\overline{CS}$ (Required Setup Time) (Note 21)	$t_{\overline{CS}}$	—		300	nS
Rising Edge of $\overline{RST}$ to Falling Edge of $\overline{CS}$ (Required Setup Time) (Note 21)	t_{ENBL}	—		5	µS
Falling Edge of $\overline{CS}$ to Rising Edge of SCLK (Required Setup Time) (Note 21)	t_{LEAD}	—	50	167	nS
Required High State Duration of SCLK (Required Setup Time) (Note 21)	t_{WSCLKh}			167	ns
Required Low State Duration of SCLK (Required Setup Time) (Note 21)	t_{WSCLKl}			167	ns
Falling Edge of SCLK to Rising Edge of $\overline{CS}$ (Required Setup Time) (Note 21)	t_{LAG}	—	50	167	nS
SI to Falling Edge of SCLK (Required Setup Time) (Note 22)	$t_{SI(SU)}$	—	25	83	nS
Falling Edge of SCLK to SI (Required Setup Time) (Note 22)	$t_{SI(HOLD)}$	—	25	83	nS
SO Rise Time (CL = 200 pF)	t_{RSO}	—	25	50	nS
SO Fall Time (CL = 200 pF)	t_{fSO}	—	25	50	nS
SI, $\overline{CS}$, SCLK, Incoming Signal Rise Time (Note 22)	t_{RSI}	—	—	50	nS
SI, $\overline{CS}$, SCLK, Incoming Signal Fall Time (Note 22)	t_{RSI}	—	—	50	nS
Time from Falling Edge of $\overline{CS}$ to SO Low Impedance (Note 23)	$t_{SO(EN)}$	—	—	145	nS
Time from Rising Edge of $\overline{CS}$ to SO High Impedance (Note 24)	$t_{SO(DIS)}$	—	65	145	nS
Time from Rising Edge of $\overline{SCLK}$ to SO Data Valid (Note 25) 0.2 V_{DD} < = SO > = 0.8 V_{DD}, CL = 200 pF	t_{VALID}	—	65	105	nS

Notes:

20. $\overline{RST}$ low duration measured with outputs enabled and going to OFF or disabled condition.
21. Maximum setup time required for the 33982 is the minimum guaranteed time needed from the micro.
22. Rise and Fall time of incoming SI, $\overline{CS}$, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
23. Time required for output status data to be available for use at SO. 1 kΩ on pull-up on $\overline{CS}$.
24. Time required for output status data to be terminated at SO. 1 kΩ on pull-up on $\overline{CS}$.
25. Time required to obtain valid data out from SO following the rise of SCLK.

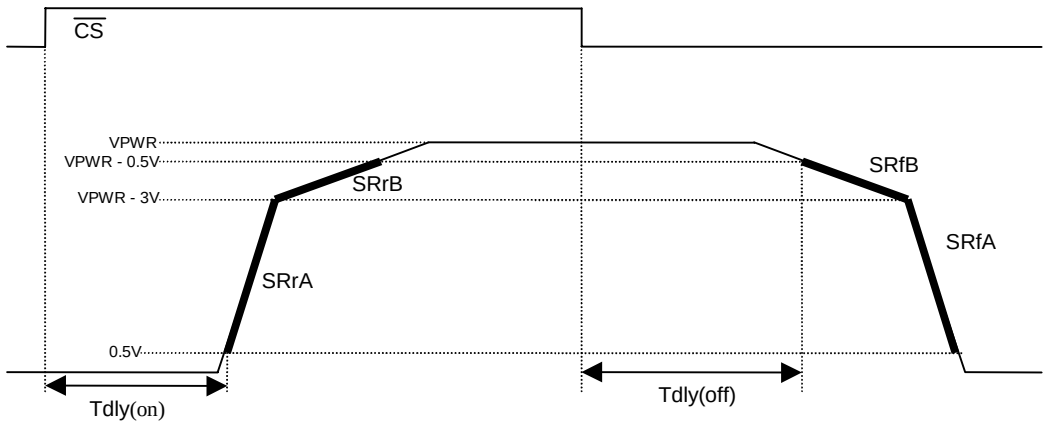


Figure 2. Output Slew Rate and Time Delays

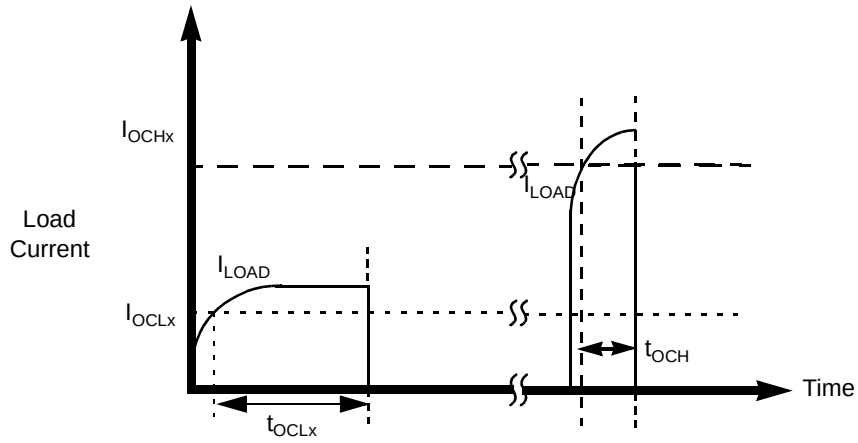


Figure 3. Over Current Shutdown

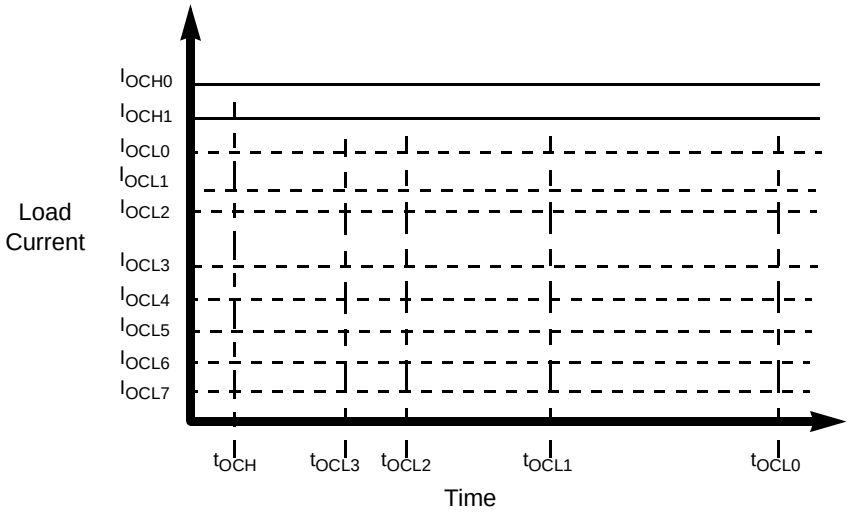


Figure 4. Over Current Low and High Detection

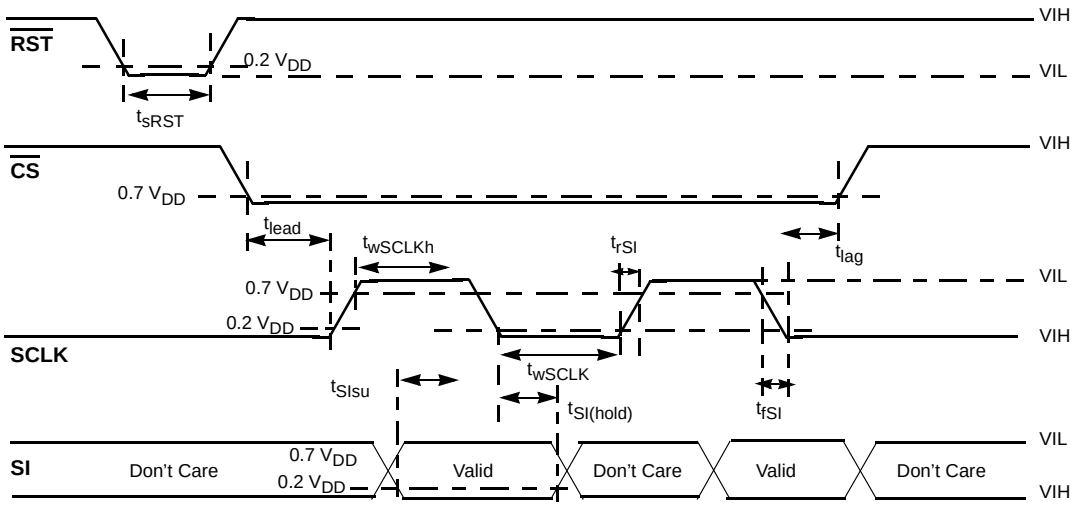


Figure 5. Input Timing Switching Characteristics

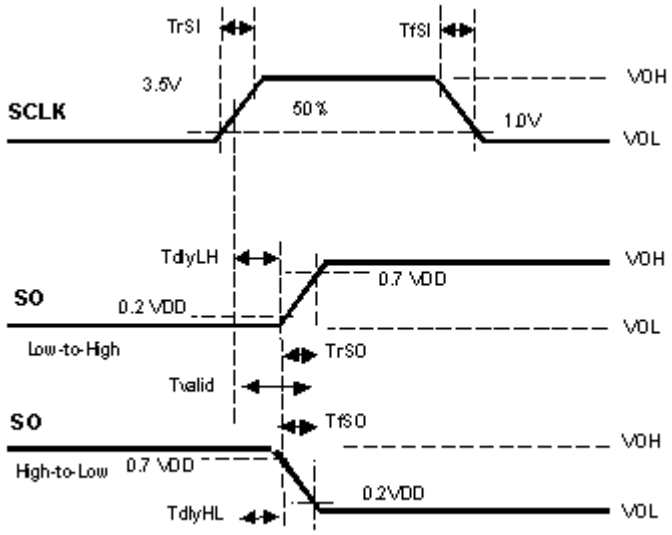


Figure 6. Valid Data Delay Time and Valid Time Waveforms

SYSTEM APPLICATION INFORMATION

INTRODUCTION

SPI Protocol Description

The SPI interface has a full duplex, three wire synchronous data transfer with four I/O lines associated with it:

- SI
- SO
- SCLK
- $\overline{CS}$

The SI/SO pins of the 33982 device follows a first in–first out (D7/D0) protocol with both input and output words transferring the Most Significant Bit (MSB) first. All inputs are compatible with 5.0 V CMOS logic levels.

The SPI lines perform the following functions:

Serial Clock

Serial clocks (SCLK) the internal Shift registers of the 33982 device. The Serial Input (SI) pin accepts data into the input shift register on the falling edge of the SCLK signal while the serial output pin (SO) shifts data information out of the SO Line Driver on the rising edge of the SCLK signal. It is important the SCLK pin be in a logic Low state whenever $\overline{CS}$ makes any transition. For this reason, it is recommended the SCLK pin be in a logic[0] whenever the device is not accessed ($\overline{CS}$ logic [1] state). SCLK has an internal pull-down L_{DWN} . When $\overline{CS}$ is logic [1], signals at the SCLK and SI pins are ignored and SO is tri-stated (high impedance). Please see the Data Transfer Timing diagram in **Figure 7** and **Figure 8**.

Serial Interface

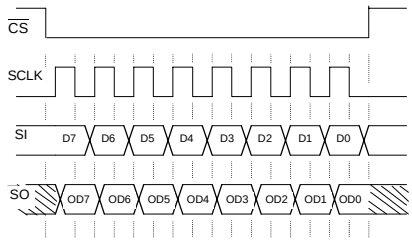
This is a serial interface (SI) command data input pin. SI instruction is read on the falling edge of SCLK. An 8-bit stream of serial data is required on the SI pin, starting with D7 to D0. The internal registers of the 33982 are configured and controlled using a 4 bit adressing scheme, as shown in Table 1. Register addressing and configuration are described in Table 1. The SI input has an internal pulldown L_{DWN}.

Serial Output

The Serial Output (SO) data pin is a tri-stateable output from the shift register. The SO pin remains in a high impedance state until the $\overline{CS}$ pin is put into a logic[0] state. The SO data is capable of reporting the status of the output, the device configuration, and the state of the key inputs. The SO pin changes states on the rising edge of SCLK and reads out on the falling edge of SCLK. Fault and Input Status descriptions are provided in Table 11

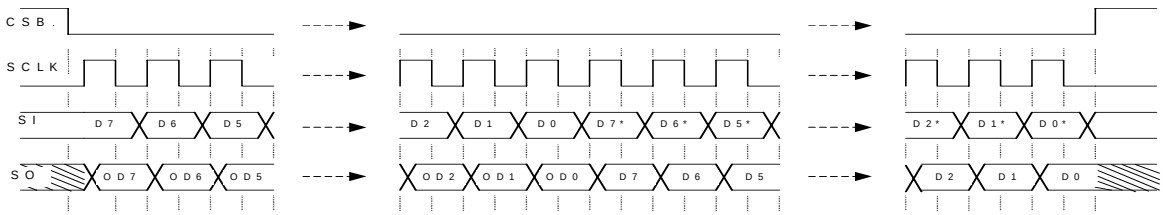
Chip Select Overbar

The Chip Select pin enables communication with the Master device. When this pin is in a logic[0] state, the device is capable of transferring information to and receiving information from the Master. The 33982 device latches-in data from the input shift registers to the addressed registers on the rising edge of $\overline{CS}$. The device transfers status information from the power output to the shift register on the falling edge of $\overline{CS}$. The SO output driver is enabled when $\overline{CS}$ is logic [0]. $\overline{CS}$ should transition from a logic [1] to a logic [0] state only when SCLK is a logic [0]. $\overline{CS}$ has an internal pull-up, L_{UP}.



NOTES:
1. RSTB is in a logic 1 state during the above operation.
2. D0, D1, D2, ..., and D7 relate to the most recent ordered entry of data into the SPSS
3. OD0, OD1, OD2, ..., and OD7 relate to the first 8 bits of ordered fault and status data out of the device.

Figure 7. Single 8-Bit Word SPI Communication



NOTES:
1. RSTB is in a logic 1 state during the above operation.
2. D0, D1, D2, ..., and D7 relate to the most recent ordered entry of data into the SPSS
3. OD0, OD1, OD2, ..., and OD7 relate to the first 8 bits of ordered fault and status data out of the device.
4. OD0, OD1, OD2, ..., and OD7 represent the first 8 bits of ordered fault and status data out of the SPSS

Figure 8. Multiple 8-Bit Word SPI Communication

SI Communication

SPI communication is accomplished using 8-bit messages. A message is transmitted by the master starting with the MSB D7 and ending with the LSB D0. Each incoming command message on the SI pin can be interpreted using the following bit assignment : the MSB, D7, the watchdog bit (seeTable 1)and in some cases, a register address bit (seeTable 1). The next three bits, D6-D4, are used to select the command register. The remaining four bits D3-D0 are used to configure and control the output and its protection features.Multiple messages can be transmitted in succession to accomodate those applications where daisy chaining is desirable, or to confirm transmitted data, as long as the messages are all mutliples of 8-bits. Any attempt made to latch in a message that is not 8-bits will be ignored.

The 33982 has 8 registers defined (and one more for internal use), which are used to configure the device and to control the state of the output. The registers are addressed via D6-D4 of the incoming SPI word (seeTable 1).

Table 1. SI Message Bit Assignment

Bit Sig	SI Msg Bit	Message Bit Description
MSB	D7	Watchdog in: toggled to satisfy watchdog requirements; also used as a Register address bit.
	D6	Register Address Bit
	D5	Register Address Bit
	D4	Register Address Bit
	D3	Used to configure the inputs, outputs, and the device protection features and SO status content.
	D2	Used to configure the inputs, outputs, and the device protection features and SO status content.
	D1	Used to configure the inputs, outputs, and the device protection features and SO status content.
LSB	D0	Used to configure the inputs, outputs, and the device protection features and SO status content.

Device Register Addressing

The nine possible register addresses (D7, D6, D5, D4) and a description of their impact on the device operation are listed below. Also see Table 7.

- **Address x000— Status Register (STATR**).This register is used to read the device status and the various configuration register contents without disrupting the device operation or the register contents. The register bits D2, D1, D0 determine the content of the first eight bits of SO data. In addition to the device status, this feature provides the ability to read the content of the OCR, SOCHLR, CDTOLR, DICR, OSDR, WDR and NAR registers. See *SO Communication* section on page 18.
- **Address x001— Output Control Register (OCR**) allows the master to control the output through the SPI. Incoming message bit D0 reflects the desired states of the high-side output; (IN_SPI); a logic [1] enables the output switch and a logic [0] turns it OFF. A logic [1] on message bit D1 enables the Current Sense (CSNS_EN) pin. Bits D2 and D3 must be logic [0] .Bit D7 is used to feed the watchdog, if enabled.
- **Address x010— Select Over Current High and Low Register (SOCHLR)** allows the Master to configure the output over current low and high detection levels, respectively. In addition to protecting the device, this slow blow fuse emulation feature can be used to optimize the load requirements to match system characteristics. Bits D2-D0 are used to set the over current low detection level to one of eight possible levels are shown in Table 2. Bit D3 is used to set the over current high detection level to one of two levels, outlined in Table 3.

Table 2. Over Current Low Detection Levels

SOCLA2 (D2)	SOCLA1 (D1)	SCOLA0 (D0)	Over Current Low Detection
0	0	0	50 A
0	0	1	45 A
0	1	0	40 A
0	1	1	35 A
1	0	0	30 A
1	0	1	25 A
1	1	0	20 A
1	1	1	15 A

Table 3. Over Current High Detection Levels

SOCH (D3)	Over Current High Detection
0	150 A
1	100 A

- **Address x011—Current Detect Time and Open Load Register (CDTOLR)** is used by the master to determine the amount of time the device will allow an over current low condition before output latches OFF occurs. Bits D1-D0 allow the master to select one of four dead times defined in Table 4. Note that these timeouts apply only to the Over Current Low Detect levels. If the selected Over Current High level is reached, the device will latch off within 20 µs.

Table 4. Over Current Timing

OCTL[1:0]	Over Current Timing
00	155 ms
01	9.7 ms
10	1.2 ms
11	150 µs

A logic [1] on bit D2 disables the Over Current Low (CD dis) Detection timeout feature. A logic [1] on bit D3 disables the Open Load (OL) Detection feature.

- **Address x100— Direct Input Control Register (DICR)** is used by the master to enable, disable, or configure the direct IN pin control of the output. A logic [0] on bits D1 will enable the output for direct control with the IN pin; a logic [1] on D1 bit will disable the output from direct control. While addressing this register, if the Input was enable for direct control, a logic [1] for the D0 bit will result in a Boolean AND of the IN pin with its corresponding D0 message bit when addressing OCR. Similarly, a logic [0] on the D0 pin will result in a Boolean OR of the IN pin to the corresponding message bits when addressing the OCR. This register is especially useful if several loads are required to be independently PWM controlled. For example, the IN pins of several devices can be configured to operate all of the outputs with one PWM output from the master. If each output is then configured to be Boolean ANDed to its respective IN pin, each output can be individually turned OFF by SPI while controlling all of the outputs, commanded on with the single PWM output.
  A logic [1] on bit D2 is used to select the high ratio (Iout/40000) on the CSNS pin. The default value [0] is used to select the low ratio(Iout/6000).
  A logic [1] on bit D3 is used to select the high speed slew rate, the default value [0] corresponds to the low speed slew rate.
- **Address 0101— Output Switching Delay Register (OSDR)** is used to configure the device with a programmable time delay that is active during Output On transitions that are initiated via SPI or the direct input. Whenever the input is commanded to transition from [0] to [1], the output will be held OFF for the time delay configured in the OSDR Register. The programming of the contents of this register have no effect on device fail-safe mode operation. The default value of the OSDR register is 000, equating to no delay, since the switching delay time is 0ms. This feature allows the user a way to minimize inrush currents, or surges, thereby allowing loads to be synchronously switched ON with a single command. There are eight selectable output switching delay times that range from 0 to 448ms.

Table 5. Switching Delay

OSDA[2:0] (D2, D1, D0)	Timing
000	0 ms
001	64 ms
010	128 ms
011	192 ms
100	256 ms
101	320 ms
110	384 ms
111	448 ms

- **Address 1101— Watchdog Register (WDR)** This register is used by the master to configure the Watchdog timeout. The Watchdog timeout is configured using bits D1 and D0. When D1, D0 bits are programmed for the desired watchdog timeout period, the WDSPI bit should be toggled as well to ensure the new timeout period is programmed at the beginning of a new count sequence.· Bit D2 (WDTO) of the WDR register can be read to determine the status of the watchdog circuitry. If WDTO bit is [1], then the watchdog has timed out and the device is in fail-safe mode. IF WDTO is [0] then the device is in normal mode (assuming device is powered and not in sleep mode), with the watchdog either enabled or disabled.

Table 6. WatchDog Time Out

WDA[1:0] (D1, D0)	Timing
00	620 ms
01	310 ms
10	2500 ms
11	1250 ms

- **Address x110—No Action Register (NAR)** can be used to no-operation fill SPI data packets in a daisy-chain SPI configuration. This would allow devices not to be affected by commands being clocked over a daisy-chained SPI configuration, and by toggling the WD bit (D7) the watchdog circuitry would continue to be reset while no programming or data read back functions are being request from the device.
- **Address x111**—This register is reserved for test and is not accessible with SPI during normal operation.

Table 7. SI Address and Configuration Bit Map

2.0 mΩ	SI Data							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
STATR	SOA3	0	0	0	0	SOA2	SOA1	SOA0
OCR	x	0	0	1	0	0	CSNS $\overline{EN}$	IN_SPI
SOCHLR	x	0	1	0	SOCH	SOCLA2	SOCLA1	SOCLA0
SDTOLR	x	0	1	1	OL dis	CD dis	CDT1	CDT0
DICR	x	1	0	0	FAST SR	CSNS high	IN dis	A/O
OSDR	0	1	0	1	0	OSDA2	OSDA1	OSDA0
WDR	1	1	0	1	0	0	WDA1	WDA0
NAR	x	1	1	0	0	0	0	0
TEST	x	1	1	1	Motorola Internal Use (Test)			

SO Communication (Device Status Return Data)

When the $\overline{CS}$ pin is pulled low, the output register is loaded and the data is clocked out MSB (OD7) first, as the new message data is clocked into the SI pin. The first eight bits of data that clocks out of the SO, following a $\overline{CS}$ transition, is dependant upon the previously written SPI word. Bit OD7 reflects the state of the watchdog bit (D7) that was addressed during the prior communication. SO data will represent information ranging from fault status to register contents as chosen by the user by writing to the STATR bits D2,D1,D0 . Note that the SO data will continue to reflect the information that was selected during the most recent STATR write until changed with an updated STATR write.

Any bits clocked out of the SO pin after the first eight will be representative of the initial message bits clocked into the SI pin since the CS pin first transitioned to a logic 0; this feature is useful for daisy chaining devices as well as message verification.

Table 8. SO Output Bit Assignment Device Status Return Format

Bit Sig	SO Msg Bit	Message Bit Description
MSB	0D7=0	Reflects the state of the Watchdog bit from the previously clocked in message(See Table 11 for exception).
	OD6	This bit will be S0A2 as selected by the most recent STATR command. However, when a STATR command of 000 (SOA[2:0]) is sent, D6 will contain the Over Temperature Fault (OTF) status.
	OD5	This bit will be S0A1 as selected by the most recent STATR command. However, when a STATR command of 000 (SOA[2:0]) is sent, D5 will contain the Over Current Detect Hi Fault (OCHF) status.
	OD4	This bit will be S0A0 as selected by the most recent STATR command. However, when a STATR command of 000 (SOA[2:0]) is sent, D4 will contain the Over Current Detect Low Fault (OCLF) status.
	OD3	This bit will reflect the register contents as selected by the most recent STATR command. A STATR command of 000 (SOA[2:0]) will return the Open Load Fault (OLF) status.
	OD2	This bit will reflect the register contents as selected by the most recent STATR command. A STATR command of 000 (SOA[2:0]) will return the Under-Voltage Fault (UVF) status.
	OD1	This bit will reflect the register contents as selected by the most recent STATR command. A STATR command of 000 (SOA[2:0]) will return the Over Voltage Fault (OVF) status.
LSB	OD0	This bit will reflect the register contents as selected by the most recent STATR command. A STATR command of 000 (SOA[2:0]) will return the Fault (FAULT) status, which is the boolean OR of all of the other fault bits.

- **Previous Address 000**—If the previous three MSBs are 000, the bits D6-D0 will reflect the current state of the Fault Register (FLTR)

Table 9. Fault Register

D7	D6	D5	D4	D3	D2	D1	D0
x	OTF	OCHF	OCLF	OLF	UVF	OVF	FAULT

D7. Don't Care

D6. (OTF) = Over Temperature Flag

D5. (OCHF) = Over Current High Flag. (This fault is latched)

D4. (OCLF) = Over Current Low Flag. (This fault is latched)

D3. (OLF) = Open Load Flag

D2. (UVF) = Under Voltage Flag (This fault is latched)

D1. (OVF) = Over Voltage Flag

D0. (FAULT) = This flag reports a fault and is reset by a read operation

Note: The $\overline{FS}$ pin reports a fault and is reset by a new Switch ON command (via SPI or direct input IN).

- **Previous Address 001**— the data in bits OD1 and OD0 will contain respective CSNS_EN and IN_SPI programmed bits.
- **Previous Address 010**— the data in bits OD3, OD2, OD1, and OD0 contains respectively the programmed Over Current high Detection Level (see Table 3)and the Overcurrent low Detection level (see Table 2).
- **Previous Address 011**—Data returned in bits OD1 and OD0 are current values for the Over Current Dead Time, illustrated in Table 4. Bit OD2 reports whethe the Over Current Detection timeout feature is active. OD3 reports whether the open load circuitry is active.
- **Previous Address 100**— The returned data contains the programmed values in the DICR.
- **Previous Address 101**—
  D7=0 The returned data contains the programmed values in the OSDR.
  D7=1 The returned data contains the programmed values in the WDR.
- **Previous Address 110**—OD2 to OD0 Return respectively the state of the IN, FSI and Wake pin (see Table 10).

Table 10. PIN Register

D2	D1	D0
IN Pin	FSI Pin	WAKE Pin

- **Address 111**—Null Data. No previous register Read Back command received, so bits OD2, OD1, and OD0 are null, or 000.

The Table 11summarize the SO register content.

Table 11. SO Bit Map Description

Previous STATR D7, D2, D1, D0				SO Returned Data							
SOA3	SOA2	SOA1	SOA0	D7	D6	D5	D4	D3	D2	D1	D0
x	0	0	0	WDin	OTF	OCHF	OCLF	OLF	UVF	OVF	Fault
x	0	0	1	WDin	0	0	1	0	0	CSNS_EN	IN_SPI
x	0	1	0	WDin	0	1	0	SOCH	SOCLA2	SOCLA1	SOCLA0
x	0	1	1	WDin	0	1	1	OL dis	CD dis	CDT1	CDT0
x	1	0	0	WDin	1	0	0	Fast SR	CSNS high	IN dis	A/O
0	1	0	1	0	1	0	1	0	OSDA2	OSDA1	OSDA0
1	1	0	1	1	1	0	1	0	WDTO	WDA1	WDA0
x	1	1	0	WDin	1	1	0	0	IN pin	FSI pin	WAKE pin
x	1	1	1								

General SO Communication Statements

Any bits clocked out of the SO pin after the first eight will be representative of the initial message bits clocked into the SI pin since the $\overline{CS}$ pin first transitioned to a logic [0]; this feature is useful for daisy chaining devices as well as message verification.

Following a $\overline{CS}$ transition of [0] to [1], determines if the message was of a valid length and if so, the data is latched into the appropriate registers. A valid message length is a multiple of eight bits. At this time, the SO pin is tri-stated and the fault status register is now able to accept new fault status information.

The output status register correctly reflects the status of the STATR selected register data at the time that the $\overline{CS}$ is pulled to a logic [0] during SPI communication, and/or for the period of time since the last valid SPI communication, with the following exceptions:

- The previous SPI communication was determined to be invalid. In this case, the status will be reported as though the invalid SPI communication never occurred.
- Battery transients below 6.0 V resulting in an under-voltage shutdown of the outputs may result in incorrect data loaded into the status register. The SO data transmitted to the master during the first SPI communication following an under-voltage V_{PWR} condition should be ignored.
- The $\overline{RST}$ pin transition from a logic [0] to [1] while the WAKE pin is at logic [0] may result in incorrect data loaded into the status register. The SO data transmitted to the master during the first SPI communication following this condition should be ignored.

Watchdog and Fail-Safe Operation

If the FSI input is a logic [1], that is, not grounded, the Watchdog timeout detection is active when either the WAKE or $\overline{RST}$ input pin transitions from logic[0] to [1]. The WAKE input is capable of being pulled up to V_{PWR} with a series of limiting resistance limiting the internal clamp current according to the specification.

The Watchdog timeout is a multiple of an internal oscillator and is specified in the Table 6. As long as the WD bit (D7) of an incoming SPI message, is toggled within the minimum watchdog timeout period (WDTO, based on the programmed value of the WDR register), the device will operate normally. If an internal watchdog timeout occurs before the WD bit, the device will revert to a Fail-Safe mode until the device is reinitialized.

During the Fail-Safe mode, the output will be driven ON regardless of the state of the various direct inputs and modes. Fail-safe mode can be detected by monitoring the WDTO bit D2 of the WDR register. This bit is logic [1] when the device is in fail-safe mode. The device can be brought out of the Fail-Safe mode by transitioning the WAKE and $\overline{RST}$ pins from logic [1] to logic [0] or forcing the FSI pin to logic [0]. Table 12 summarizes the various methods for resetting the device from the latched Fail-Safe mode.

If the FSI pin is tied to GND, the Watchdog fail-safe operation is disabled.

Loss of V_{DD} and Fail-Safe Mode

The external 5 V supply connected to V_{DD} powers the SPI circuitry and any other internal logic that is not active during device fail-safe operation.

If the external 5 V supply is not within specification or even disconnected, then the 33982 will transition to fail-safe mode, if enabled, otherwise the output will latch off.

The 33982 uses the battery input to power the output MOSFET, related current sense circuitry and any other internal logic providing fail-safe device operation with no V_{DD} supplied. Then, the watchdog, the over voltage, over temperature, and over current circuitry are fully operational (with default values) in the device fail-safe mode of operation regardless the state of V_{DD}.

Table 12. Fail-Safe Operation and Transitions to Other 33982 Modes

WAKE	RST	WDTO	OUT	Comments
0	0	x	OFF	Device is in Sleep mode
1	0	No	OFF	Output is OFF,Watchdog is alive.

Table 12. Fail-Safe Operation and Transitions to Other 33982 Modes

1	0	Yes	ON	Watchdog has timed out and the device is in Fail-Safe Mode. $\overline{RST}$ and WAKE must be transitioned to logic 0 simultaneously to bring the device out of the Fail-safe mode.
0	1	No	S	Device in Normal Operating mode
0	1	Yes	ON	Watchdog has timed out and the device is in Fail-Safe Mode. $\overline{RST}$ and WAKE must be transitioned to logic 0 simultaneously to bring the device out of the Fail-safe mode.
1	1	No	S	Device in Normal Operating mode
1	1	Yes	ON	Watchdog has timed out and the device is in Fail-Safe Mode. $\overline{RST}$ and WAKE must be transitioned to logic 0 simultaneously to bring the device out of the Fail-Safe mode.

x = Don't care

S = State determined by SPI and /or Direct Input configurations

Assumptions: Normal operating voltage and junction temperatures with FSI pin floating

Default or Sleep Mode

The default mode of the 33982 is also the Sleep mode. This is the state of the device after first applying battery voltage (V_{PWR}), prior to any I/O transitions. This is also the state of the device when the WAKE and $\overline{RST}$ are both logic [0]. In the Sleep mode, the output, and all unused internal circuitry, such as the internal 5 V regulator, are off to minimize current draw. In addition, all SPI configurable features of the device are as if set to logic [0]. The device will transition to the normal or fail-safe operating modes based on the Wake and Reset inputs as defined in Table 12.

Fault Logic What Happen During Fail-Safe

This device indicates the faults below as they occur by driving the $\overline{FS}$ pin to [0]:

- Over temperature fault
- Open load fault
- Over current fault (high and low)
- Over voltage and under voltage fault

Some of the faults are latched. See Table 9.

The $\overline{FS}$ pin will return to [1] when the fault condition is removed. Specific fault information is retained in the fault register and is available via the SO pin during the first valid SPI communication after the STATR D[3:0] bits are configured to 0000.

Over Temperature Fault

The 33982 device incorporates over temperature detection and shutdown circuitry in the output structure. Over temperature detection occurs when the output is in the ON state.

For the output, an over temperature fault (OTF) condition will result in the output turning OFF until the temperature falls below the $T_{LIM(hyst)}$. This cycle will continue indefinitely until action is taken by the master to shut OFF the output, or until the offending load is removed.

When experiencing this fault, the OTF fault bit will be set in the status register and cleared after either a valid SPI read, a power reset of the device.

Over Voltage Fault

The 33982 shuts down the output during an over voltage fault (OVF) condition on the V_{PWR} pin. The output remains in the OFF state, until the over voltage condition is removed. When experiencing this fault, the OVF fault bit is set in the status register and cleared after either a valid SPI read, a power reset of the device.

Open Load Fault

The 33982 incorporates open load detection circuitry on the output. output Open Load Fault (OLF) is detected and reported as a fault condition when the output is disabled (OFF). The open load fault is detected and latched into the status register after the internal gate voltage is pulled low enough to turn OFF the output. The OLF fault bit is set in the status register. If the open load fault is removed, the status register will be cleared after reading the register.

Over Current Fault

The device has eight programmable over current low detection levels and two programmable over current high detection levels for maximum device protection. The two selectable, overriding over current detection levels, defined by IOCH0 and IOCH are illustrated in Figure 4. There are also eight different over current low detect levels (IOCL0, IOCL1, IOCL2, IOCL3, IOCL4, IOCL5, IOCL6, & IOCL7) also illustrated in Figure 4.

If the load current level ever reaches the selected over current low detect level, and the over current condition exceeds the programmed over current time period (t_{OCx}) , then the device will latch the output off.

If, at any time, the current reaches the selected IOCH level, then the device will latch off immediately, regardless of the selected t_{OCLx} driver.

For both cases, the device output will stay off indefinitely, until the device is commanded off and then on again.

Reverse Battery

The output survives the application of reverse voltage as low as -16 V. Under these conditions, the output will enhance to

keep the junction temperature less than 150°C and the ON resistance of the output will fairly be the same than in normal mode. No additional passive component are required

Ground Disconnect Protection

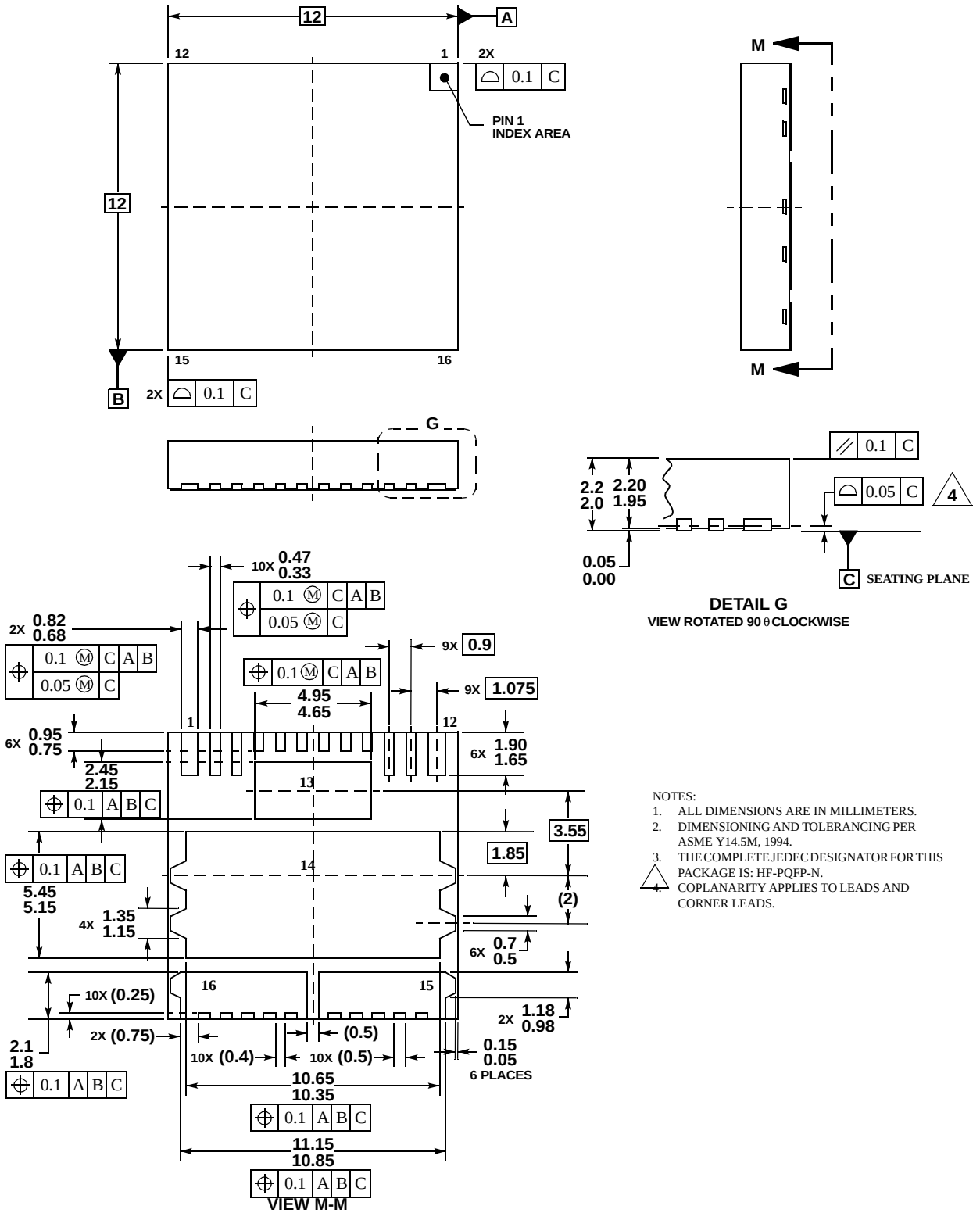
In the event the 33982 ground is disconnected from load ground, the device protects itself and safely turns OFF the output, regardless the state of the output at the time of disconnection.

Under Voltage Shutdown

The output latches off at some battery voltage between 5.0 V and 6.0 V. As long as the V_{DD} level stays within the normal specified range, the internal logic states within the device will be sustained. This ensures that when the battery level then returns above 6.0 V, the device can be returned to the state that it was in prior to the low V_{PWR} excursion. Once the output latches OFF, the device must be turned off and then on again to re-enable the output.

PACKAGE DIMENSIONS

FC SUFFIX
PLASTIC PACKAGE
CASE 1402-01
PQFN
ISSUE A



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF-PQFP-N.
4. COPLANARITY APPLIES TO LEADS AND CORNER LEADS.

NOTES

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