

SN65563A, SN65564A, SN75563A, SN75564A ELECTROLUMINESCENT ROW DRIVERS

D3223, MAY 1986 REVISED DECEMBER 1989

- Each Device Drives 34 Electrodes
- Selectable Open-Source or Open-Drain Output
- Outputs Rated at 240 V
- Output Current Capability:
 - 150 mA to 100 mA (SN65')
 - 150 mA to 120 mA (SN75')
- CMOS-Compatible Inputs
- Very Low Steady-State Power Consumption

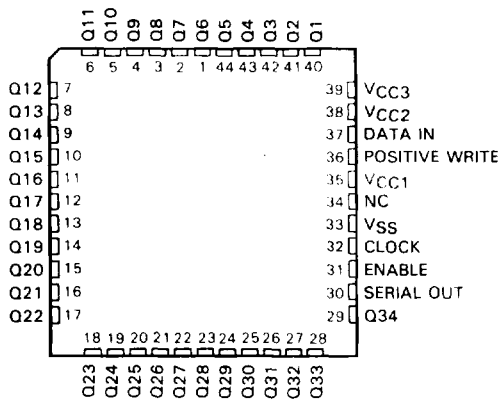
description

The SN65563A, SN65564A, SN75563A, and SN75564A are monolithic BIDFET[†] integrated circuits designed to drive the row electrodes of an electroluminescent display. All inputs are CMOS compatible. If POSITIVE WRITE is high, the Q outputs act like open-source outputs and output data is not inverted with respect to input data. If POSITIVE WRITE is low, the Q outputs act like open-drain outputs and output data is inverted with respect to input data. The SN65564A and SN75564A output sequences are reversed from the SN65563A and SN75563A for ease in printed circuit board layout.

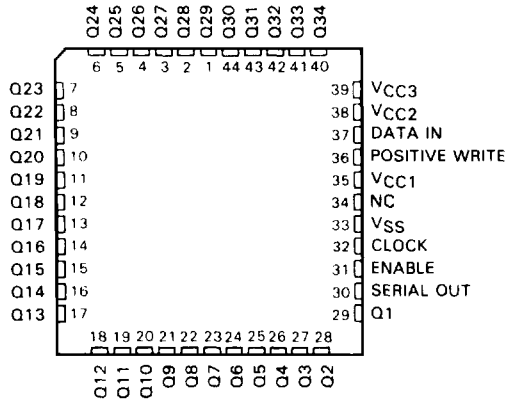
Typically, composite VCC2, VCC3, and ground signals are externally generated by a high-voltage switching circuit. Serial data is entered into the shift register on the high-to-low transition of CLOCK. A high at the ENABLE input allows those outputs with a high in their associated register to be turned on, causing the corresponding row to be connected to VCC2 when POSITIVE WRITE is high or to ground when POSITIVE WRITE is low. VCC3 may be tied to VCC2 or held 5 V to 15 V above VCC2 for better V_{OH} characteristics. SERIAL OUTPUT from the shift register may be used to cascade additional devices. This output is not affected by the ENABLE or POSITIVE WRITE inputs.

The SN65563A and SN65564A are characterized for operation over the full automotive operating temperature range of -40°C to 85°C. The SN75563A and SN75564A are characterized for operation from 0°C to 70°C.

SN65563A, SN75563A . . . FN PACKAGE
(TOP VIEW)



SN65564A, SN75564A . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

[†]BIDFET-Bipolar, double-diffused, N-channel and P-channel MOS transistors on the same chip — Patented Process

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SN65563A, SN65564A, SN75563A, SN75564A ELECTROLUMINESCENT ROW DRIVERS

LOAD FUNCTION TABLE

FUNCTION	CONTROL INPUTS			SHIFT REGISTER R1 THRU R34	OUTPUTS	
	CLOCK	ENABLE	POSITIVE WRITE		SERIAL	Q1 THRU Q34
LOAD	↓	X	X	Load and Shift [†]	R34	Determined by ENABLE and POSITIVE WRITE
	No _i	X	X	No Change	R34	Determined by ENABLE and POSITIVE WRITE

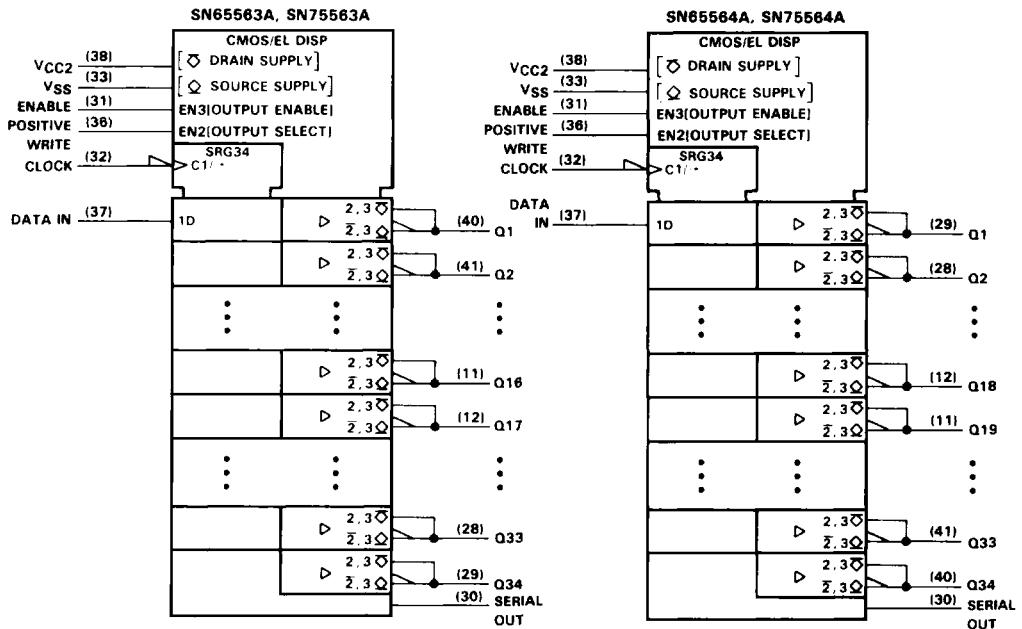
[†] Register R34 takes on the state of R33, R33 takes on the state of R32, . . . R2 takes on the state of R1, R1 takes on the state of the data input.

OUTPUT CONTROL FUNCTION TABLE

FUNCTION	CONTROL INPUTS			SHIFT REGISTER CONTENTS R _n FOR R1 THRU R34 (Determined Above)	OUTPUTS	
	CLOCK	ENABLE	POSITIVE WRITE		SERIAL	Q1 THRU Q34
OUTPUT CONTROL	X	L	X	X	R34	High-Impedance
	X	H	H	H	R34	H
	X	H	L	H	R34	L
	X	X	X	L	R34	High-Impedance

H = high, L = low, X = irrelevant, ↓ = high-to-low transition

schematics of inputs and outputs

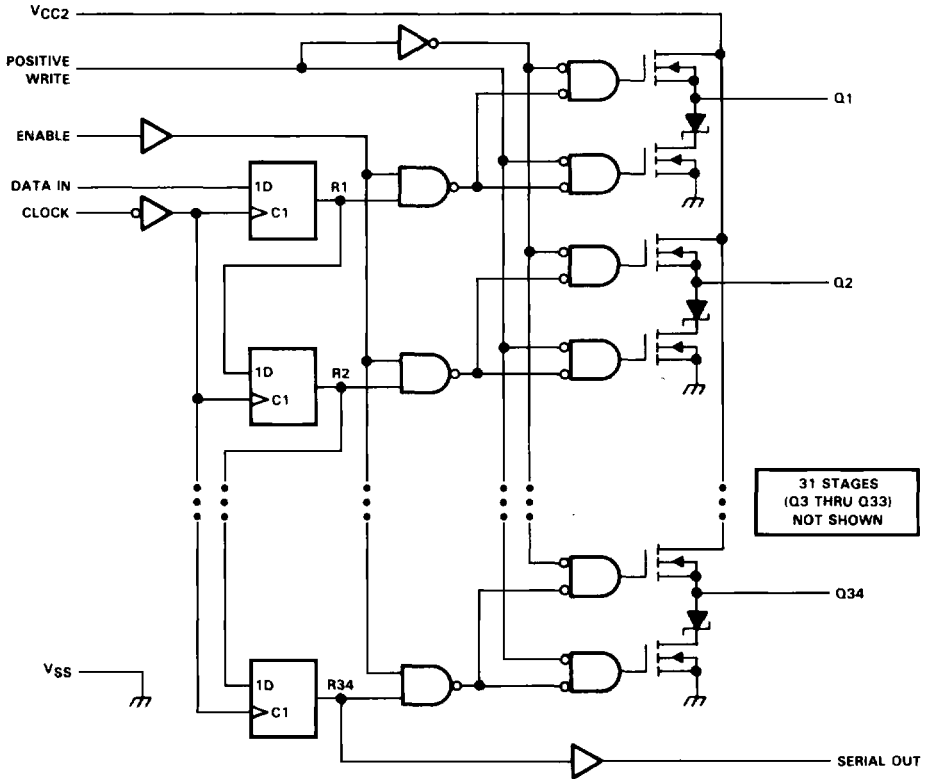


[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

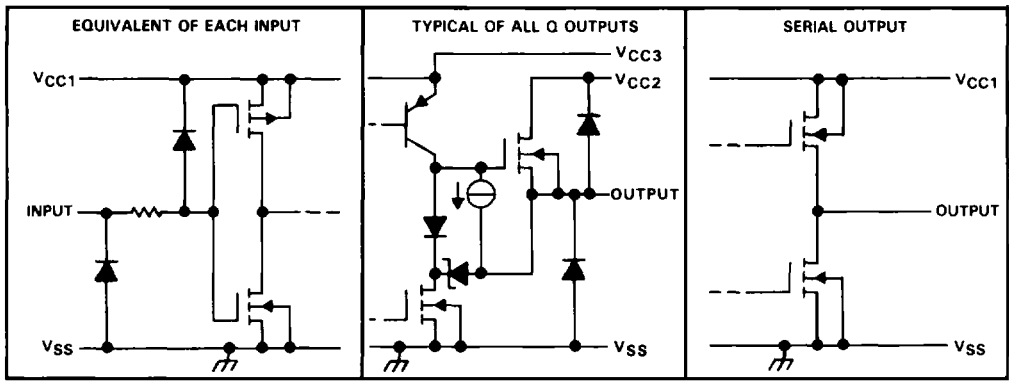
TEXAS
INSTRUMENTS

**SN65563A, SN65564A, SN75563A, SN75564A
ELECTROLUMINESCENT ROW DRIVERS**

logic diagram (positive logic)



schematics of inputs and outputs

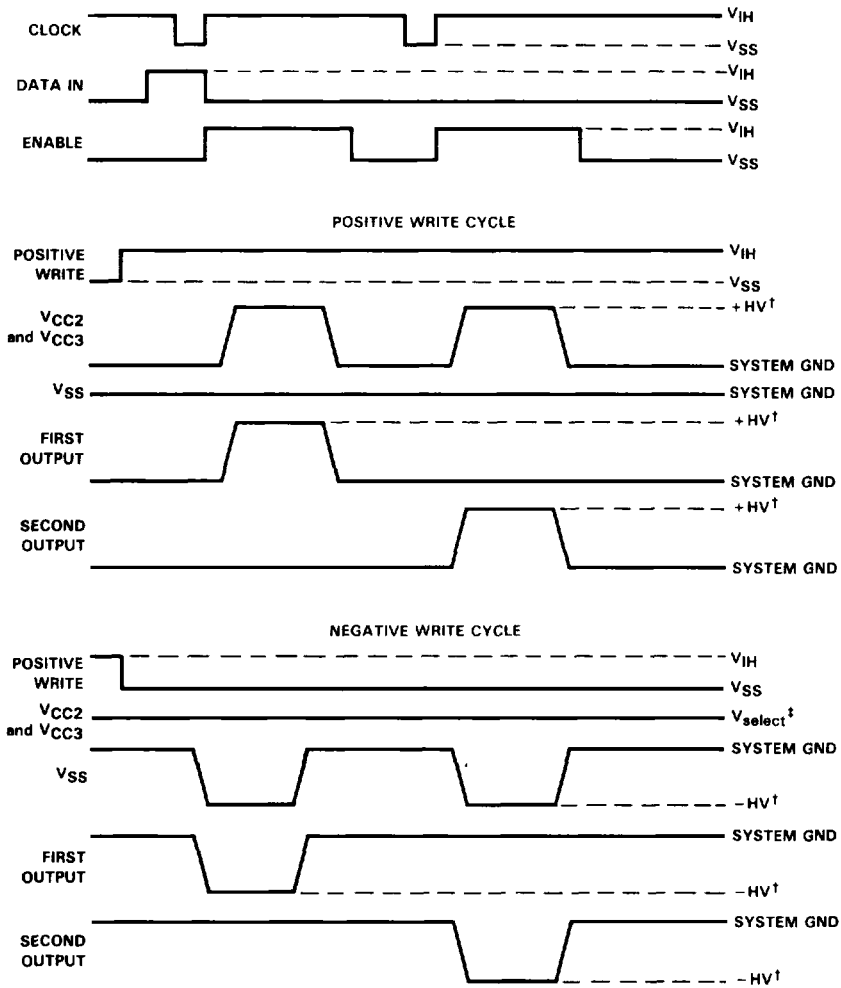


**TEXAS
INSTRUMENTS**

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SN65563A, SN65564A, SN75563A, SN75564A
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typical operating sequence



[†]HV = high voltage

[‡]During the negative write cycle, the VCC2 and VCC3 supplies are in a high-impedance state.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1)	15 V
Supply voltage, V_{CC2}	240 V
Supply voltage, V_{CC3}	240 V
Supply voltage, V_{SS}	-240 V
Input voltage	-0.3 V to $V_{CC1} + 0.3$ V
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2)	1700 mW
Operating free-air temperature range: SN65563A, SN65564A	-40°C to 85°C
SN75563A, SN75564A	0°C to 70°C
Storage temperature range	-40°C to 125°C
Case temperature for 10 seconds	260°C

NOTES: 1. Voltage values are with respect to V_{SS} .

2. For operation above 25°C free-air temperature, derate to 1088 mW at 70°C or 884 mW at 85°C at the rate of 13.6 mW/°C.

recommended operating conditions (see Note 1, Figure 1, and Figure 2)

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}		7.5	12	13.2	V
Supply voltage, V_{CC2}		$V_{CC3} - 15$		V_{CC3}	V
Supply voltage, V_{CC3}		0		235	V
Supply voltage, V_{SS}		0		-235	V
High-level input voltage, V_{IH}		$0.75V_{CC1}$		$V_{CC1} + 0.3$	V
Low-level input voltage, V_{IL}^{\dagger}		-0.3		$0.25V_{CC1}$	V
High-level output current, I_{OH}	SN65563A, SN65564A			-100	mA
	SN75563A, SN75564A			-120	
Low-level output current, I_{OL}				150	mA
Output clamp current, I_{OK}				± 150	mA
Clock frequency, f_{clock}				4	MHz
Pulse duration, CLOCK high or low, t_{wCLK}		125			ns
Setup time, DATA IN high or low before CLOCK † , t_{su1}		100			ns
Setup time, CLOCK low before V_{CC2}^{\dagger} or V_{SS}^{\dagger} , t_{su2}		300			ns
Setup time, ENABLE high before V_{CC2}^{\dagger} or V_{SS}^{\dagger} , t_{su3}		300			ns
Setup time, POSITIVE WRITE high or low before V_{CC2}^{\dagger} or V_{SS}^{\dagger} , t_{su4}		300			ns
Hold time, DATA IN high or low after CLOCK † , t_{h1}		100			ns
Hold time, CLOCK high after V_{CC2}^{\dagger} or V_{SS}^{\dagger} , t_{h2}		300			ns
Hold time, ENABLE high after V_{CC2}^{\dagger} or V_{SS}^{\dagger} , t_{h3}		0			ns
Hold time, POSITIVE WRITE after V_{CC2}^{\dagger} or V_{SS}^{\dagger} , t_{h4}		0			ns
Hold time, ENABLE low between successive V_{CC2}^{\dagger} , t_{h5}	SN65563A, SN65564A	12			μ s
	SN75563A, SN75564A	10			
Hold time, ENABLE low between successive V_{SS}^{\dagger} , t_{h6}		300			ns
Operating free-air temperature, T_A	SN65563A, SN65564A	-40		85	°C
	SN75563A, SN75564A	0		70	

† The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only.



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electrical characteristics over recommended operating ranges of V_{CC1} and free-air temperature range, $V_{CC2} = 235\text{ V}$, $V_{CC3} = 235\text{ V}$, $V_{SS} = 0$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$I_{O(off)}$	Off-state Q output current	$V_O = 235\text{ V}$			50	μA
		$V_O = 0$			-50	
V_{OH}	High-level output voltage	Q outputs	$I_O = -70\text{ mA}$	$V_{CC2} - 30$		V
		SERIAL OUT	$I_O = -100\ \mu\text{A}$, $V_{CC1} = 12\text{ V}$	10.5		
V_{OL}	Low-level output voltage	Q outputs	$I_O = 150\text{ mA}$	30		V
		SERIAL OUT	$I_O = 100\ \mu\text{A}$	1		
I_{IH}	High-level input current	$V_{IH} = V_{CC1}$			100	μA
I_{IL}	Low-level input current	$V_{IL} = 0$			-100	μA
I_{CC1}	Supply current from V_{CC1}	One Q output high			4	mA
		All Q outputs low or high impedance			2	
I_{CC3}	Supply current from V_{CC3}	One Q output high			10	mA
		All Q outputs low or high impedance			200	

switching characteristics operating range of V_{CC1} , $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level serial output from clock		400	ns
t_{PHL}	Propagation delay time, high-to-low level serial output from clock		400	ns

PARAMETER MEASUREMENT INFORMATION

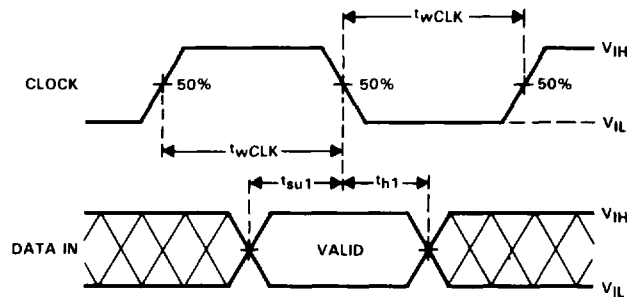
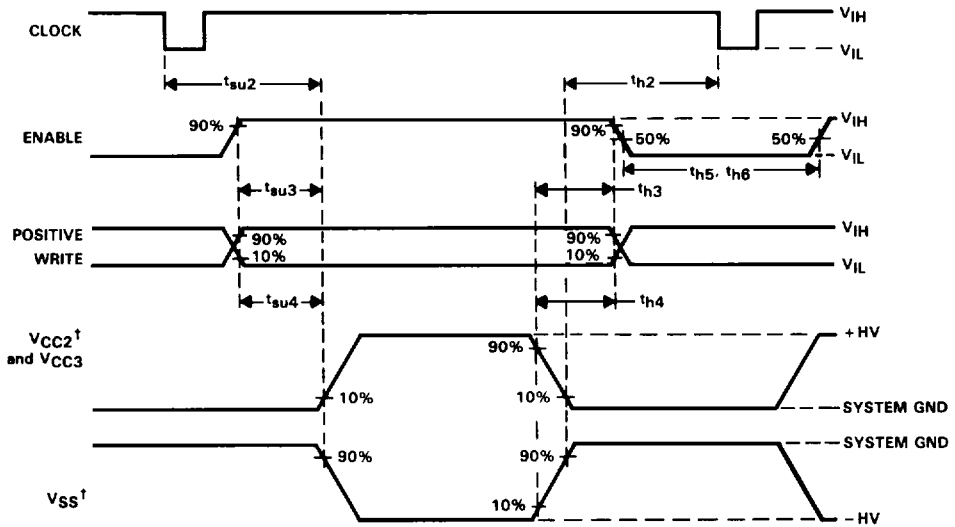


FIGURE 1. INPUT TIMING VOLTAGE WAVEFORMS

PARAMETER MEASUREMENT INFORMATION



[†]Timing waveforms are with respect to V_{CC2} or V_{SS} , as appropriate.

FIGURE 2. CONTROL INPUT TIMING VOLTAGE WAVEFORMS

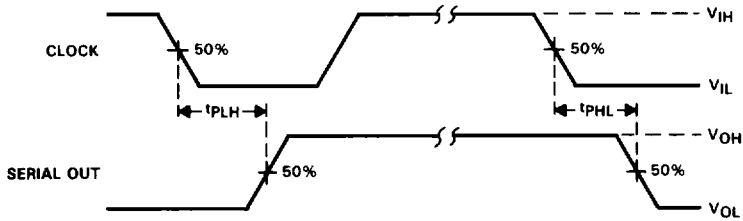


FIGURE 3. VOLTAGE WAVEFORMS FOR PROPAGATION DELAY TIMES, CLOCK TO DATA OUT

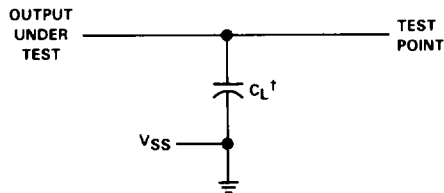


FIGURE 4. LOAD CIRCUIT

[†] C_L includes probe and jig capacitance.