

Fiber Optic "Light to Logic" Receiver

Technical Data

RGR1622

Features

- * "Light to Logic" 28-Pin DIP Receiver with ECL Outputs
- * High Sensitivity (<-32 dBm) at 622 Mbit/s
- * Hermetically Sealed Package
- * Overload > -7 dBm
- * Jitter Tolerance Compliant to CCITT G.958
- * Bellcore Compliant to TA-NWT-000983

Applications

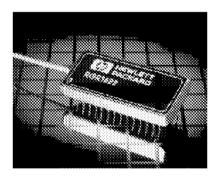
- * Telecommunications Networks
- * SONET OC-12
- * SDH STM-4
- Local Area and Metropolitan
 Area Networks
- * ATM Single Mode Public Network
- * Digital Cable TV Networks

Description

The RGR1622 is a high speed fiber optic receiver. It detects light in the 1200 - 1600 nm wavelength range and converts it to an electrical signal at data rates up to 622 Mbit/s.

The receiver includes an InGaAs PIN photodiode and a HEMT transimpedance amplifier. This is ac coupled to a PLL based clock recovery circuit. The data and clock outputs are retimed complementary ECL.

A TTL open collector low light alarm output is also provided.



Functional Description Design

The RGR1622 receiver contains an InGaAs photodetector and a HEMT transimpedance preamplifier. The preamplifier output is fed to a Phase Locked Loop (PLL) based clock recovery circuit. The output of the PLL clock recovery circuit is used to retime the preamplifier output. ECL interface circuits provide the complementary data and clock signals. The receiver incorporates a 50/125 micron fiber pigtail to allow use with both single mode and multimode fiber systems.

The clock recovery circuit is capacitivily coupled to the preamplifier circuit. The coupling capacitor values are large enough that no sensitivity degradation occurs with data containing a frequency content down to 50 kHz.

A level detect circuit provides an open collector output that will go low to indicate when loss of light has occured. For TTL and 5 Volt CMOS compatibility a 4.7 K pull-up resistor should be connected between the alarm output and +5 Volts

The status of the alarm output does not have any influence upon the clock or data outputs.

If the input falls below that which the receiver can detect the clock outputs will not remain at 622.08 MHz. The frequency will vary as the circuit "hunts" for a signal to lock to. The data outputs will randomly toggle until the input signal is restored to a normal operating level.

Noise Immunity

The RGR1622 receiver has internal components to filter power supply noise from the gain circuits.

To obtain maximum performance, it is highly recommended that external filter networks be utilized. The photodiode bias pin is especially sensitive to extraneous noise. A voltage supply for the PIN diode is provided on pin 3. This can be directly connected to the photodiode pin 1 or via a current monitor circuit for optical power monitoring. The current drain on pin 1 is directly proportional to the incoming optical signal. This current will range from approximately 500 nA on a small optical signal to 200 µA for a large optical

As a practical consideration, the majority of current drawn from the positive power supply is used in the preamplifier IC. The interface amplifier draws the majority of the current from the negative supply. The series RC networks attached to each pin are intended to insure maximum stability.

Terminating the Outputs

The data and clock outputs of the RGR1622 are 10 K ECL compatible.

Care should be taken to match termination impedances to the interconnect to minimize reflection effects.

More information on ECL interconnection, biasing and termination can be found in most ECL Electronic manufacturer's data hooks. The alarm output requires a pullup resistor to Vdd. A typical value is 4.7 K and results in a TTL compatible signal.

Circuit Layout

The RGR1622 uses very high bandwidth circuitry to achieve its high level of performance. Care must be taken to ensure stable operation. The use of ground planes and transmission line interconnects is required. The use of a standard evaluation board is highly recommended for those users who are not familiar with these techniques.

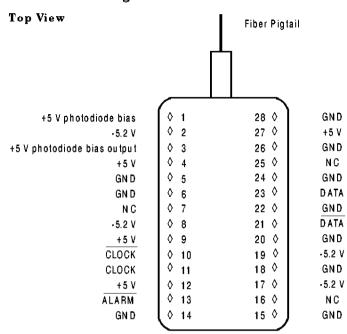
Evaluation boards for the RGR1622 are available. Please contact your representative for details.

Manufacturing

The RGR1622 is a fully hermetically sealed component. The fiber pigtail on the device requires normal fiber handling considerations. Care should be taken to avoid tight bends as well as excessive tension on the fiber pigtail.

The allowable temperature range for the RGR1622 is limited by the material used in the pigtail. Exposure to temperatures over 85°C is not recommended. Low profile sockets or hand soldering is recommended for this part.

Connection Diagram



Pin Descriptions

Pin 1 Photodiode Bias:

This pin is connected to the PIN photodiode cathode. It is normally reverse biased with +5 Volt through an appropriate decoupling network. Current drawn will be directly proportional to input optical signal level.

Pin 3 Photodiode Bias Output:

This pin provides a +5 Volt decoupled output for use as a photodiode bias. It can be connected to PIN 1 directly or via an external current monitoring circuit for optical power monitoring. It is not necesary to use this output, if it is not used it should be left open circuit and a separate +5 Volt bias provided for the photodiode.

Pins 2, 8, 17, 19 -5.2 Volt Supply:

These pins are connected to the -5.2 Volt supply. Each pin should be decoupled with a 100 nF capacitor.

Pins 4, 9, 12, 27 +5 Volt Supply: These pins are connected to the +5 Volt supply. Each pin should be decoupled with a 100 nF capacitor.

Pins 5, 6, 14, 15, 18, 20, 22, 24, 26, 28 GROUND:

These pins are connected to the circuit board ground plane.

Pins 7, 16, 25 N.C.:

These pins are not used in the present RGR1622 design. They should be left as an open circuit.

Pins 10, 11 CLOCK, CLOCK These pins provide complementary ECL CLOCK and CLOCK outputs. They must be correctly terminated even if not used.

Pin 13 ALARM:

This pin is the loss of light alarm output and will go low to indicate a low optical input. The open collector output requires a pull-up resistor to +5 Volts. A typical value is 4.7 K.

Pin 21 DATA OUTPUT:

This pin is the inverted data output. It is at ECL Logic LOW during an input optical pulse. It must be correctly terminated even if it is not used.

Pin 23 DATA OUTPUT:

This pin is the data output. It is at ECL Logic HIGH during an input optical pulse. It must be correctly terminated even if it is not used.

Figure 1 - Block Diagram

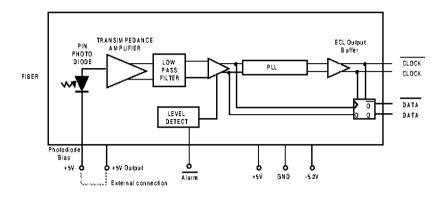
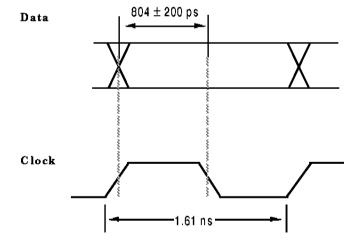


Figure 2 - Data/Clock Timing



Performance Specifications

Absolute Limiting Ratings

Parameter	Symbol	Minimum	Maximum	Units	Note
Operating Temperature	-	-40	+85	°C	
Storage Temperature	-	-40	+85	°C	
Supply Voltage	+ V	-0.5	7.0	V	
	-V	-7.0	0.5	V	

Electrical Parameters

Parameter	Minimum	Typical	Maximum	Units	Note
Digital Outputs	10 K ECL compatible				
Power Requirements					
-5.2 V	_	175	-	m A	1
5.0 V	-	50	-	m A	1
MTTF (at 40°C Case	-	500,000	-	Hrs	
Temperature)					

Optical Parameters (Note 2)

Parameter	Minimum	Typical	Maximum	Units	Note
Wavelength Range	1200	-	1600	nm	
Receiver Sensitivity 622 Mbit/s	•	-	-32	dBm	3
Maximum I/P Power 622 Mbit/s	-7.0	-	-	dBm	4
Clock and Data Timings (Fig 2)					
Alarm On	-40.5	-	-33.5	dBm	
Hysteresis	0.5	-	3.5	dB	
Jitter Tolerance	CCITT G.958 compliant				
Fiber Specifications	50/125 μm core/cladding (multimode)				
	900 μm OD silicone/nylon tight jacket				

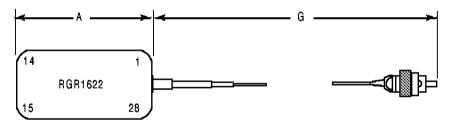
Notes:

- 1. With outputs un-terminated.
- $2. \ \, \hbox{Over operating temperature range unless noted otherwise}.$
- 3. At 1300 nm wavelength; NRZ; 10 $^{\cdot 10}$ BER; 100% modulation depth; 2 $^{\cdot 23}$ -1 pseudo-random pattern.
- 4. For 10 -10 BER.

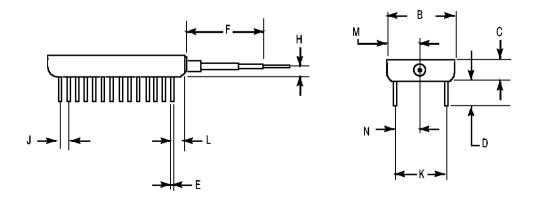
Drawing Dimensions

DIM	MIN	NOM	MAX
A	42.90		43.20
В	19.50		19.80
C	5.90	-	6.60
D	5.10	-	•
E	•	0.44	•
F	-	30.0	•
G	400	-	1200
Н	3.20		3.64
J	-	2.54	•
K	•	15.20	•
L	-	5.00	•
M	-	9.80	•
N	•	7.60	•

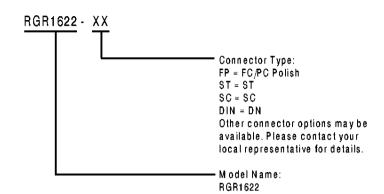
All dimensions in mm



TOP VIEW



Ordering Information



Allowable Part Numbers:

RGR1622-FP

RGR1622-ST

RGR1622-SC

RGR1622-DN



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