CRYSTAL Semiconductor Corporation

CS6453

Modem and Audio Analog Front End

Features

- Complete Voiceband DSP Front-End
  24-Bit A/D Converter
  18-Bit D/A Converter
- Minimum 84 dB Dynamic Range and 80 dB Signal-to-Distortion (at full scale)
- Supports telephone emulation
- Supports business audio
- On-chip speaker driver for modem monitoring
- Supports PCMCIA digital speaker signal
- 3.0 to 5.5V power supply range

General Description

The CS6453 is a high-resolution analog-to-digital and digital-to-analog converter for V.fast, V.32bis, V.32 and other high performance modems.

The CS6453 also supports telephone emulation. In telephone emulation, the CS6453 and external DSP collectively implement both modem and telephone set capabilities. This allows an end-user to connect a handset to the "modem" card, and alternatively use the telephone connection for voice and data.

The CS6453 has 5 kHz bandwidth for modem and telephone applications, and 10 kHz bandwidth for business audio applications. The business audio capability allows the modem to playback and input audio files.

The CS6453 also supports the digital speaker signal of the PCMCIA interface standard. The modem can transfer the modem monitor signal via PCMCIA to the system speaker.

ORDERING INFORMATION:
CS6453-CQ 44-Pin TQFP package

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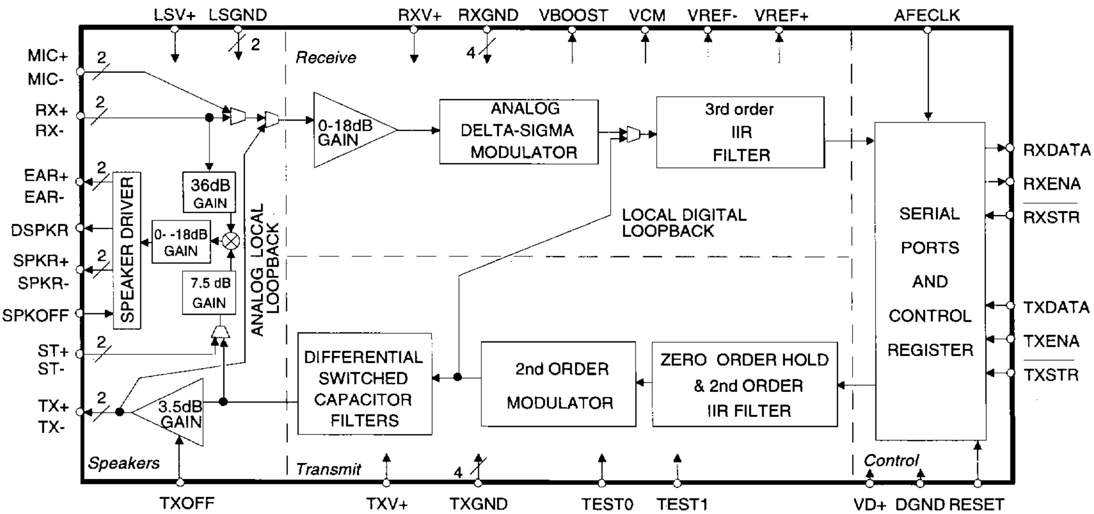

Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

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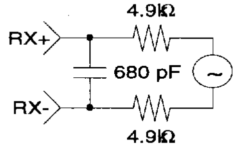
ANALOG RECEIVER CHARACTERISTICS (T_A = 25 °C; TXV+, RXV+, VD+ = 3.3V; AFECLK = 5.5296 MHz; 1 kHz Input sine wave at 3.0 Vp-p; Gain = 0dB; Output sampling rate of 19.2 kHz; Speaker drivers off; RX± inputs selected; with Test Circuit (antialiasing filter) as shown below; Note 1.)

Parameter	Min	Typ	Max	Units
Resolution	24	-	-	Bits
Dynamic Performance (Note 2)				
Dynamic Range (300 Hz to 3.3 kHz)				
gain=0dB; - with full scale input	84	91	-	dB
- with input 20dB below full scale	87	91	-	dB
- BAudio=1, Low_Power=0, with full scale input	-	80	-	dB
gain=6dB; - with full scale input	-	88	-	dB
gain=12dB; - with full scale input	-	85	-	dB
gain=18dB; - with full scale input	-	82	-	dB
Signal-to-Total Harmonic Distortion (300 Hz to 3.3 kHz)				
gain=0dB; - with full scale input	80	90	-	dB
- with input 20dB below full scale	83	90	-	dB
gain=6dB; - with full scale input	-	90	-	dB
gain=12dB; - with full scale input	-	90	-	dB
gain=18dB; - with full scale input	-	90	-	dB
Idle Channel Noise - with input at differential ground	-75	-90	-	dB
Total Absolute Gain Accuracy (300 Hz - 3.3 kHz)	-5	-	+5	%
Power Supply rejection: Passband (Note 3)	-	60	-	dB
dc Performance				
Offset Error	-	100	-	mV
Filter Characteristics				
Passband BAudio=0, Low_Power=1 (Note 4)	dc	-	2.5	kHz
BAudio=1, Low_Power=1 or BAudio=0, Low_Power=0	dc	-	5	kHz
BAudio=1, Low_Power=0	dc	-	10	kHz
Passband variation from ideal (ripple) (300 Hz - 3.3 kHz)	-0.125	-	+0.125	dB
Input Characteristics				
AC Input Impedance at 1 kHz	-	27	-	kΩ
Analog Input Full Scale Signal Level (RX+ to RX-)	-	±1.5	-	V
Gain Stage Performance				
Nominal step size	5.5	-	6.5	dB

Notes:
1. 5V operation is guaranteed by design
2. Unless stated otherwise, dynamic performance is relative to 0.707x of full scale. Receiver full scale defined as $2^{21}+2^{19}+2^{18}$ (hex 2C0000). Transmitter full scale defined as $(2^{17})/1.5$ (decimal 87831).
3. With 300 mVp-p, 1 kHz ripple applied to supply.
4. Passband bandwidth specifications for BAudio=0 and Low_Power=0 are tested. All other combinations of BAudio and Low-Power are guaranteed by characterization and design.



Test Circuit

ANALOG TRANSMITTER CHARACTERISTICS (T_A = 25 °C; TXV+, RXV+, VD+ = 3.3V; AFECLK = 5.5296 MHz; 1 kHz Input Digital sine wave with full scale $2^{17}/1.5$ input; Input sampling rate of 19.2 kHz; Speaker drivers off; with Analog Load as shown below; Note 1.)

Parameter	Min	Typ	Max	Units
Resolution	18	-	-	Bits
Dynamic Performance (Note 2)				
Dynamic Range (300 Hz - 3.3 kHz)				
- with full scale input	84	90	-	dB
- with input 12dB below full scale	87	90	-	dB
- BAudio=1, Low_Power=0, with full scale input	-	80	-	dB
Signal-to-Total Harmonic Distortion (300 Hz - 3.3 kHz)				
- with full scale input	80	90	-	dB
- with input 12dB below full scale	83	90	-	dB
Idle Channel Noise - with input code of 0	-75	-	-	dB
Total Absolute Gain Accuracy (300 Hz - 3.3 kHz)	-20	-	+20	%
Power Supply rejection: Passband (Note 3)	-	60	-	dB
dc Performance				
Monotonicity	-	16	-	Bits
Filter Characteristics				
Passband BAudio=0, Low_Power=1 (Note 4)	dc	-	2.5	kHz
BAudio=1, Low_Power=1 or BAudio=0, Low_Power=0	dc	-	5	kHz
BAudio=1, Low_Power=0	dc	-	10	kHz
Passband variation from ideal (ripple) (300 Hz - 3.3 kHz)	-0.125	-	+0.125	dB
Output Characteristics				
Maximum output swing (TX+ to TX-)	±2.5	-	-	V
AC Output Impedance at 1 kHz	-	0.3	-	Ω
Output Current	±4	-	-	mA

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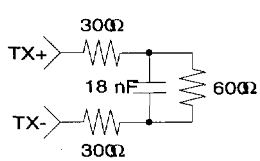


Analog Load

8-ohm SPEAKER CHARACTERISTICS (T_A = 25 °C; LSV+, TXV+, RXV+, VD+ = 3.3V; Analog receiver input of 50 mVp-p, 1 kHz sine wave; Digital transmitter input of 1 kHz sine wave with peak amplitude of 35132; Speaker driver load of 8Ω; Volume gain setting = high; 8-ohm Speaker selected [Ephone=0], Note 1.)

Parameter		Min	Typ	Max	Units
Smode1=0 and Smode0=0	TX-to-SPKR gain	-	off	-	-
	RX-to-SPKR gain	-	off	-	-
Smode1=0 and Smode0=1	TX-to-SPKR gain	-	+4	-	dB
	RX-to-SPKR gain	-	off	-	-
Smode1=1 and Smode0=0	TX-to-SPKR gain	-	off	-	-
	RX-to-SPKR gain	-	+36	-	dB
Smode1=1 and Smode0=1	TX-to-SPKR gain	-	+4	-	dB
	RX-to-SPKR gain	-	+36	-	dB
Signal-to-Noise plus Distortion		30	45	-	dB
Maximum differential Output voltage		±1.6	-	-	V
Passband	BAudio=0, Low_Power=1 (Note 4)	dc	-	2.5	kHz
	BAudio=1, Low_Power=1 or BAudio=0, Low_Power=0	dc	-	5	kHz
	BAudio=1, Low_Power=0	dc	-	10	kHz

EARPHONE CHARACTERISTICS (T_A = 25 °C; LSV+, TXV+, RXV+, VD+ = 3.3V; Analog receiver input of 40 mVp-p, 1 kHz sine wave; Digital transmitter input of 1 kHz sine wave with peak amplitude of 27447; Earphone driver load of 125Ω; Volume gain setting = high; Earphone selected [Ephone=1], Note 1.)

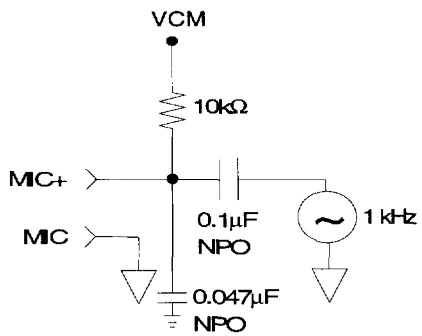
Parameter		Min	Typ	Max	Units
Smode1=0 and Smode0=0	TX-to-Ear gain	-	off	-	-
	RX-to-Ear gain	-	off	-	-
	ST-to-Ear (Note 5)		off		-
Smode1=0 and Smode0=1	TX-to-Ear gain	-	+4	-	dB
	RX-to-Ear gain	-	off	-	-
	ST-to-Ear (Note 5)		+7.5		dB
Smode1=1 and Smode0=0	TX-to-Ear gain	-	off	-	-
	RX-to-Ear gain	-	+36	-	dB
	ST-to-Ear (Note 5)		off		-
Smode1=1 and Smode0=1	TX-to-Ear gain	-	+4	-	dB
	RX-to-Ear gain	-	+36	-	dB
	ST-to-Ear (Note 5)		+7.5		dB
Signal-to-Noise plus Distortion		30	45	-	dB
Maximum differential Output voltage		±1.25	-	-	V
Passband	BAudio=0, Low_Power=1 (Note 4)	dc	-	2.5	kHz
	BAudio=1, Low_Power=1 or BAudio=0, Low_Power=0	dc	-	5	kHz
	BAudio=1, Low_Power=0	dc	-	10	kHz

Notes: 5. When the earphone output and microphone input are both enabled and TX± enabled (TXOFF=0), the sidetone path is selected instead of the transmit path.

MICROPHONE CHARACTERISTICS (T_A = 25 °C; LSV+, TXV+, RXV+, VD+ = 3.3V; AFECLK = 5.5296 MHz; 1 kHz Input sine wave at 187.5 mVp-p; Gain = 18dB; Output sampling rate of 19.2 kHz; Speaker drivers off; with Test Circuit as shown below.)

Parameter	Min	Typ	Max	Units
Signal-to-Noise plus Distortion				
BAudio=0, Low_Power=0	-	82	-	dB
BAudio=1, Low_Power=0	-	80	-	dB
Passband BAudio=0, Low_Power=1 (Note 4)	dc	-	2.5	kHz
BAudio=1, Low_Power=1 or BAudio=0, Low_Power=0	dc	-	5	kHz
BAudio=1, Low_Power=0	dc	-	10	kHz
Analog Input Maximum Swing	-	0.75	-	V

Test Circuit



DIGITAL CHARACTERISTICS (T_A = 25 °C; TXV+, RXV+, VD+ = 3.3V; All measurements performed under static conditions, Note 1.)

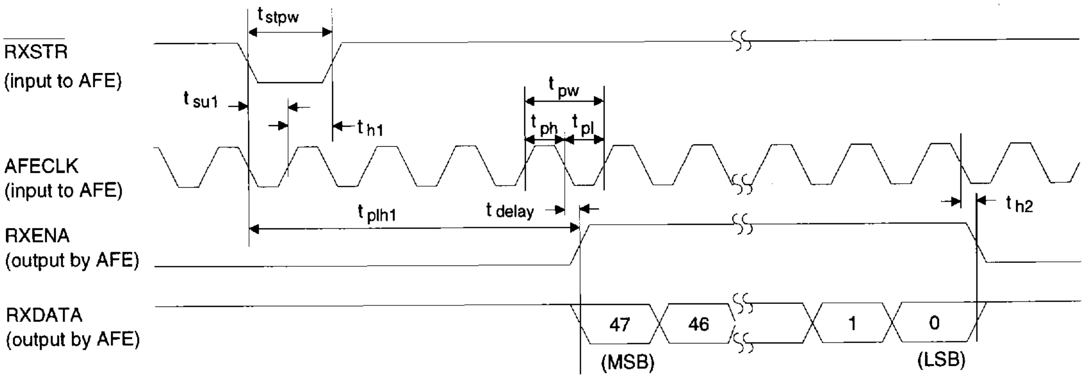
Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	(VD+)-0.5V	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.5	V
High-Level Output Voltage (Iout = -600 μA) (Note 6)	V_{OH}	(VD+)-0.3V	-	-	V
Low-Level Output Voltage (Iout = 800 μA) (Note 6)	V_{OL}	-	-	0.3	V
Input Leakage Current	I_{IN}	-	-	±10	μA
Digital Output Pin Capacitance	C_{OUT}	-	9	-	pF

Note: 6. The device is designed for low current drive. Only CMOS inputs may be connected to digital outputs.

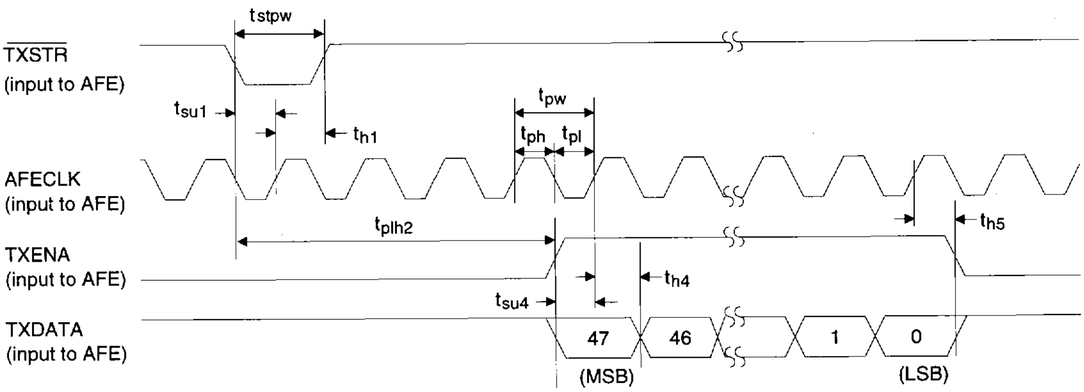
SWITCHING CHARACTERISTICS (T_A = 25 °C; CL = 50 pF; TXV+, RXV+, VD+ = 3.3V; All timing measurements performed at 50% level unless otherwise noted; Note 1.)

Parameter		Symbol	Min	Typ	Max	Units
AFECLK Clock Rate		f_{AFECLK}	1.0	5.5296	5.8	MHz
AFECLK Duty Cycle	Pulse Width Pulse Width High Pulse Width Low	t_{pw} t_{ph}/t_{pw} t_{pl}/t_{pw}	172 40 40	180.85 - -	- 60 60	ns % %
Strobe Pulse Width		t_{stpw}	t_{pw}	-	-	ns
$\overline{RXSTR}$ and $\overline{TXSTR}$ setup to AFECLK rising		t_{su1}	25	-	-	ns
$\overline{RXSTR}$ and $\overline{TXSTR}$ hold after AFECLK rising		t_{h1}	65	-	-	ns
Receiver Delay: $\overline{RXSTR}$ low to RXENA high		t_{plh1}	-	t_{pw} * 4	-	ns
RXDATA, RXENA delay from AFECLK falling	(Note 7)	t_{delay}	-	-	60	ns
RXENA and RXDATA hold from 52nd AFECLK falling		t_{h2}	10	-	-	ns
Transmitter Delay: $\overline{TXSTR}$ low to TXENA high	(Note 8)	t_{plh2}	t_{pw} * 4	-	-	ns
TXENA andTXDATA setup to AFECLK rising	(Note 8)	t_{su4}	25	-	-	ns
TXENA and TXDATA hold after AFECLK rising	(Note 8)	t_{h4}	65	-	-	ns
TXENA and TXDATA hold from AFECLK rising on LSB	(Note 9)	t_{h5}	65	-	-	ns
RESET deasserted to $\overline{TXSTR}$ or $\overline{RXSTR}$ falling	(Note 10)	t_{delay1}	t_{pw} * 2	-	-	ns
RESET low to AFECLK rising		t_{su6}	20	-	-	ns
RESET pulse width		t_{rspw}	t_{pw}	-	-	ns
Sleep delay: last AFECLK to start of sleep mode	(Note 11)	t_{delay4}	0.001	-	1	ms
Rise Times: (see figure)	Any Digital Input Any Digital Output	t_{risein} $t_{riseout}$	- -	20 15	- -	ns ns
Fall Times: (see figure)	Any Digital Input Any Digital Output	t_{fallin} $t_{fallout}$	- -	20 15	- -	ns ns
VBOOST Settling Time	(Note 12)	t_{vboost}	-	15	-	ms
VCM Settling Time	(Note 12)	t_{vcm}	-	5	-	ms
VREF Settling Time	(Note 12)	t_{vref}	-	5	-	ms

Note:
7. RXENA asserts on 4th falling edge of AFECLK after $\overline{RXSTR}$ is latched.
8. TXENA and TXDATA are ignored until the 4th AFECLK rising edge after $\overline{TXSTR}$ is latched.
9. If more than 48 bits are input, shift data into the CS6453.
10. Assert before t_{pw} * 2 after RESET is deasserted.
11. The device enters sleep mode 1 ms from the last AFECLK edge. AFECLK can idle either high or low.
12. This is the time required for the analog bias voltage to settle to its final value after power is applied, reset falls, or the clock is restored. Operation of the device before this time may yield incorrect results. The control bit FReset (see Table 2) may be asserted after the settling time for 1 sample to ensure a consistent starting state. All zero input data should be written on bits 6-23 and 30-47 when removing FRESET (falling) to avoid a race condition between the new data and reset being removed. The control bits 0-5 and 24-29 may be high or low as needed.



Serial Data Output Timing



Serial Data Input Timing

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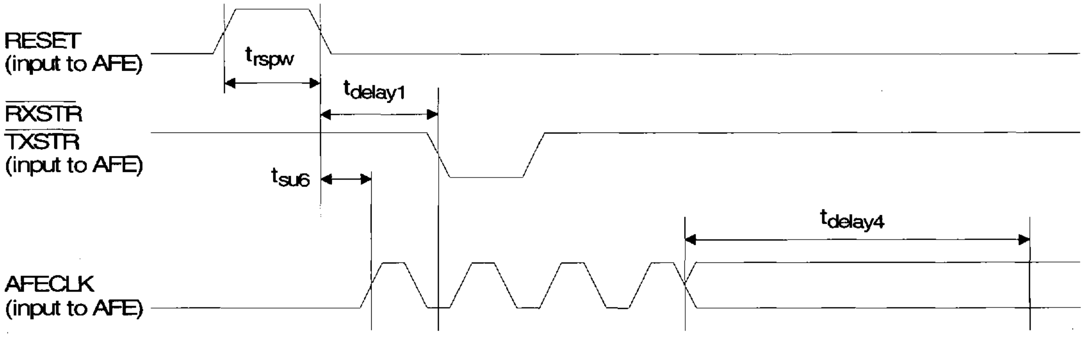
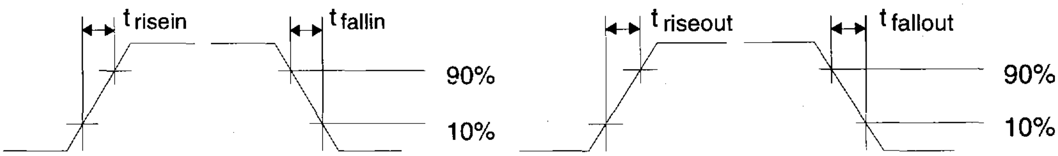


Reset and Power-down Timing



Rise and Fall Times

RECOMMENDED OPERATING CONDITIONS

(TXGND, RXGND, DGND, LSGND = 0V, Note1.)

Parameter	Symbol	Min	Typ	Max	Units
DC Supply (Note 13)	TXV+, RXV+, VD+, LSV+	3.0	3.3	5.5	V
Analog Current Consumption (TXV+ plus RXV+) (Note 14)					
Low_Power = 0, TXOFF = 0		-	20	TBD	mA
Low_Power = 0, TXOFF = 1		-	11	TBD	mA
Low_Power = 1, TXOFF = 0		-	12	TBD	mA
Low_Power = 1, TXOFF = 1		-	7	TBD	mA
(power-down mode)		-	25	150	µA
Digital Current (VD+) Power = 0	I_d	-	1.5	-	mA
Speaker driver current (no load)					
8-ohm Speaker selected		-	6.5	-	mA
Earphone selected		-	2.5	-	mA
RX+/RX- Source impedance		-	-	5	kΩ
8-ohm Speaker current (SPKR+, SPKR-)	I_{lds}	-	-	250	mA
Earphone current (Ear+, Ear-)	I_{ear}	-	-	10	mA

Note: 13. All voltages with respect to ground.

14. Speaker drivers off; current consumption applies to 3 and 5V operation.

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ABSOLUTE MAXIMUM RATINGS

(TXGND, RXGND, DGND, LSGND = 0V; all voltages with respect to ground.)

Parameter	Symbol	Min	Max	Units
DC Power Supply	TXV+, RXV+, VD+, LSV+	-0.3	6.0	V
Input Current (Note 14) Any pin except supplies and SPKR±	I_{IN}	-	±10	mA
Analog Input Voltage	V_{INA}	-0.3	0.3 + RXV+	V
Digital Input Voltage	V_{IND}	-0.3	0.3 + VD+	V
Ambient Operating Temperature	T_A	0	70	°C
Storage Temperature	T_{stg}	-65	150	°C

Note: 15. Transient currents up to 200 mA will not cause SCR latch-up.

WARNING: Operating this device at or beyond these extremes may result in permanent damage to the device. Normal operation of the part is not guaranteed at these extremes.

GENERAL DESCRIPTION

The CS6453 functions as an analog front end to a DSP, allowing the DSP to send and receive modem, telephone and business audio signals. The CS6453 provides a complete data conversion subsystem for voice band signal processing. The A/D converter (including sample/hold and much of the antialiasing filtering), D/A converter, and voltage reference are on-chip.

As shown in Figure 1, for modem applications, the TX± and RX± pins connect to the modem Data Access Arrangement. To support the monitoring of modem call progress, the CS6453 can drive a 8-ohm loud speaker via pins SPKR±, and drive a personal computer speaker via pin DSPKR. For telephone and business audio applications, the EAR± output pins connect to the earphone speaker, and the MIC± input pins connect to the microphone.

The CS6453 is a single channel device, and supports modem and voice communications on an non-simultaneous basis. Either the RX± inputs or the MIC± signals may be multiplexed into the A/D channel.

A 5.5296 MHz clock must be supplied to the CS6453 pin AFECLK. The CS6453 divides AFECLK input signal by two or four to generate an oversampling clock.

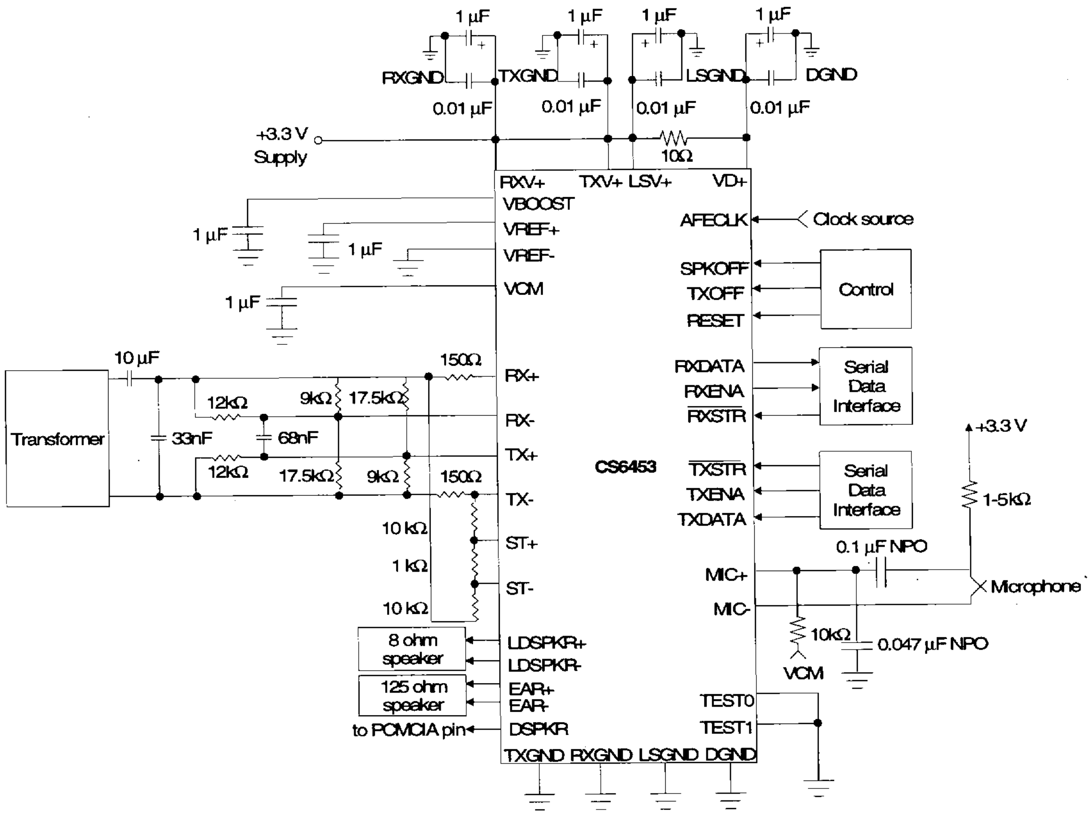


Figure 1. Recommended Connection Diagram

SUPPORT OF MODEM STANDARDS

The CS6453 dynamic range is designed for V.32 and higher-performance standards. For V.22 and lower performance standards, the CS6453 has better analog performance than is required. For these lower performance modems, the CS6453's power requirements can be reduced by approximately 50%. The power reduction will result in reduced analog specifications, as shown in the specification tables.

To place the CS6453 in the low-power V.22 mode, set control bits Low_Power and BAudio to 1. With bit Low_Power enabled (low-power mode), the internal sampling clock is reduced by one-half, cutting the filter bandwidth in half. This allows certain analog sections to be throttled back in power. The selection of business audio doubles the digital filter bandwidth. The net effect is retaining the 5 kHz bandwidth. Note that in this V.22 mode, the filter update rate is $f_{AFECLK}/4$ instead of $f_{AFECLK}/2$. The serial port operation is unchanged in this mode.

RECEIVER

The full scale input range of the CS6453 is nominally ±1.5 V differential. The CS6453 is production tested with a 50 ohm source impedance. However, the receiver can be used with higher source impedances. When the source impedance exceeds 5k ohms, the linearity of the ADC may be degraded.

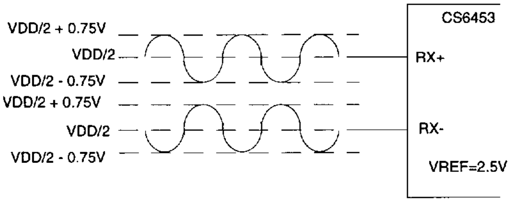


Figure 2. Full Signal Input Voltage

A programmable gain block precedes the ADC. Four gain options (0 dB, 6 dB, 12 dB, 18 dB) are selectable via the control register.

The 3rd-order modulator has an oscillation detection circuit. When oscillation is detected, the modulator is collapsed to a 1st-order modulator for 32 AFECLK clock cycles. After that interval, the modulator returns to third order. It is expected that certain input signals, such as busy tones, will cause the reduction to 1st order. While operating as a 1st-order loop, noise performance is degraded.

The converter's serial output appears MSB-first in 2's complement format (see Table 1). A digital 24-bit output of $2^{21} + 2^{19} + 2^{18}$ (hex "2C0000") corresponds to a full scale, 3.0 V peak-to-peak differential, input (see Figure 2).

The receiver creates 24-bit samples, which are available at a 2.7648 MHz rate (1.3824 MHz for Power = 1). The DSP will request samples at a rate of approximately 19.2 kHz. Each request results in the two most-recent samples being transferred to the DSP.

Bits	Mnemonic	Function
(MSB) 47-24	RXSAMP1	RX Sample #1, MSB first
(LSB) 23-0	RXSAMP2	RX Sample #2, MSB first

Table 1. Receive Serial Data Output Word

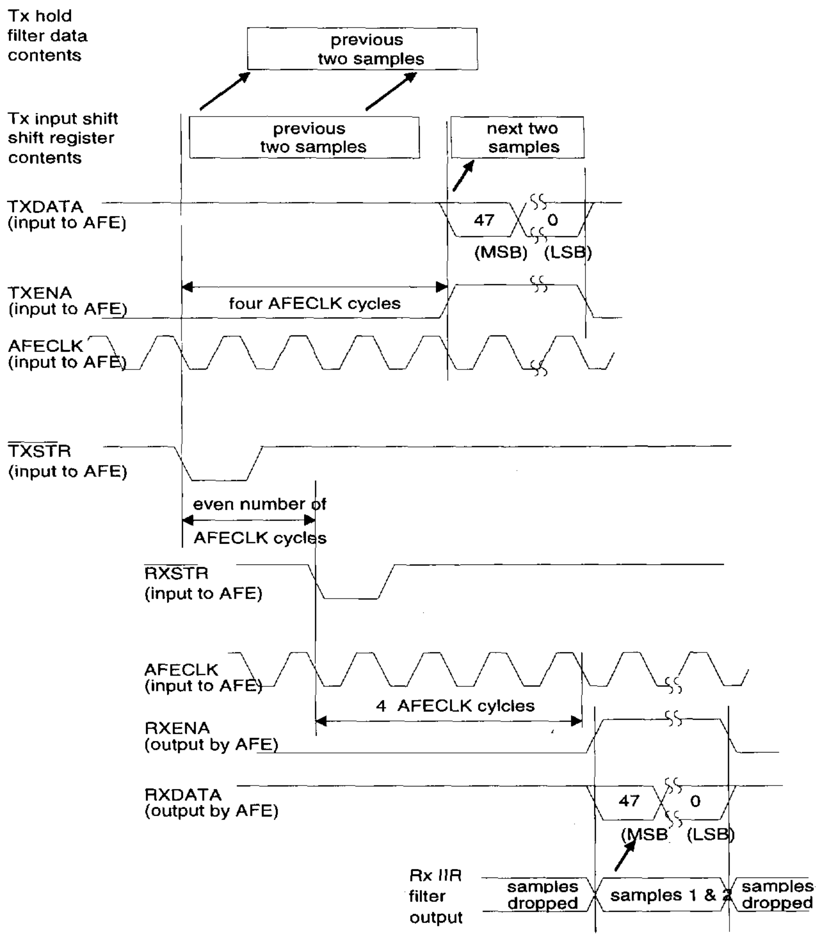


Figure 3. Receive and Transmit Signal Timing (Power=0)

Serial Data Out: AFE to DSP

The serial output port is used to output data words from the receiver. Output consists of 48 bits, written MSB first, on pin RXDATA. The DSP requests to receive 48 bits from the CS6453 by strobing $\overline{\text{RXSTR}}$ low (see Figure 3). The falling edge of $\overline{\text{RXSTR}}$ must be synchronous with the falling edge of AFECLK. $\overline{\text{RXSTR}}$ signal must also be properly phased with the $\overline{\text{TXSTR}}$ signal. If not, the $\overline{\text{RXSTR}}$ will be ignored, that is to say, $\overline{\text{RXSTR}}$ is sampled internally with the sampling clock whose phase is determined by $\overline{\text{TXSTR}}$. A properly phased $\overline{\text{RXSTR}}$ signal is a multiple of 2 or 4 AFECLK cycles from the latest $\overline{\text{TXSTR}}$ signal. When the CS6453 senses that $\overline{\text{RXSTR}}$ is low, then four AFECLK cycles later, the CS6453 sets RXENA high, and transfers 48 bits to the DSP using AFECLK. RXDATA is valid, and may be sampled, on the rising edge of AFECLK.

Receiver Filtering Considerations

The digital filtering is located after the A/D conversion and can thus reject noise injected during the conversion process (i.e. power supply ripple, voltage reference noise, or noise in the ADC itself).

In contrast, analog filtering removes the noise before it ever reaches the converter. To address this issue, the CS6453's analog modulator and digital filter reserve headroom such that the device can process signals with amplitude approaching ±2 V, and still output accurately converted and filtered data.

In applying the CS6453, aliasing occurs during both the initial sampling of the analog input at $f_{s_{in}}$ (2.7648 MHz for Low_Power=0, 1.3824 MHz for Low_Power = 1), and during the digital decimation process. Like any sampled-data filter, though, the digital filter's passband spectrum repeats around integer multiples of the sample rate, $f_{s_{in}}$. That is, any noise within ± 5 kHz bands around $f_{s_{in}}$, 2 $f_{s_{in}}$, 3 $f_{s_{in}}$, etc. will pass unfiltered and alias into the baseband. Such noise can only be filtered by analog filtering *before the signal is sampled.*

Since the signal is heavily oversampled (144:1), a single-pole passive RC filter can typically be used as shown in Figure 1. Any nonlinearities contributed by this filter will be encoded as distortion by the CS6453. Therefore low distortion, high frequency capacitors such as NPO (or COG) ceramic are recommended.

TRANSMITTER

The CS6453 utilizes the delta-sigma technique of executing low-cost, high-resolution D/A conversions. A delta-sigma D/A converter consists of three basic blocks: an interpolator, a 2nd-order digital modulator and an analog filter.

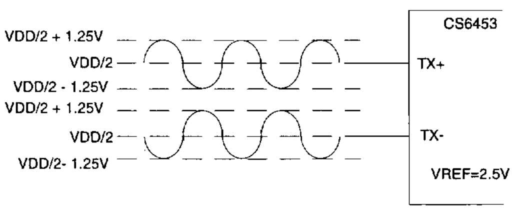
The analog output is driven differentially from TX+/TX-. An analog output amplitude of ± 2.5 V corresponds to a full scale input (87381 decimal which equals $(2^{17})/1.5$, after analog loopback calibration. Refer to Figure 4 and the System Calibration section. The transmitter driver can be powered down using pin TXOFF.

Serial Data In: DSP to AFE

The converter's serial input appears MSB-first in 2's complement format (Table 2). Upon each strobe to the CS6453 from the DSP, two events occur. (Figure 3). First, the old data words, received following the previous strobe, are input to the filter. The first of the old words is input to the DAC for one clock cycle (2.7648 MHz for Low_Power = 0, 1.3824 MHz for Low_Power = 1).
The second of the old words is input to the DAC continuously until the next strobe occurs.

The second event is that two new words are received by the CS6453, and are stored in a shift register until the next strobe occurs.

Data is transferred using four input pins: $\overline{\text{TXSTR}}$, AFECLK, TXENA and TXDATA. Input consists of 48 bits, written MSB first, on pin TXDATA. The DSP indicates that it desires to transfer 48 bits to the CS6453 by strobing $\overline{\text{TXSTR}}$ low.



Full Scale Output level= (TX+) - (TX-)= 2.5 Vp or 5 Vpp

Figure 4. Full Scale Output Signal Level

6

	Bits	Mnemonic	Function
(MSB)	47-30	TXSamp1	TX Sample #1, MSB first
	29	Smode1	Speaker source control.
	28	Smode0	

Smode1	Smode0	Mode
0	0	speaker off
0	1	TX/ST only (Note 1)
1	0	RX only
1	1	TX/ST and RX (Note 1)

Bits	Mnemonic	Function
27	Sp1	Speaker level control.
26	Sp0	

Sp1	Sp0	Level
0	0	Mute
0	1	Low (-18 dB)
1	0	Medium (-6 dB)
1	1	High (0 dB)

Bits	Mnemonic	Function
25	RXGain1	Receiver Modulator Gain control
24	RXGain0	

RXGain1	RXGain0	Gain
0	0	0 dB
0	1	+6 dB
1	0	+12 dB
1	1	+18 dB

Bits	Mnemonic	Function
23-6	TXSamp2	TX Sample #2, MSB first
5	BAudio	Enable Business Audio filters (1=filter bandwidth of 10 kHz; adjusts filter coefficients).
4	FReset	Filter reset enable (1=clear the filter contents).
3	Cntl1	Source for ADC Channel
2	Cntl0	

Cntl1	Cntl0	Function
0	0	RX±
0	1	Digital Local Loopback
1	0	Analog Local Loopback
1	1	Microphone

Bits	Mnemonic	Function
1	Low_Power	Power control. (0=full power & performance; 1= reduce power & performance; adjusts bias currents).
0	Speaker Selection	

EPHONE	Output Selected
0	8-ohm Speaker (SPKR±) & Digital speaker (DSPKR)
1	Earphone (EAR±)

Notes: 1. The sidetone path is selected over the transmit path when the earphone output, microphone input, and TX± output (TXOFF=0) are all enabled.

Table 2. Transmit Serial Data Input Word

The falling edge of $\overline{\text{TXSTR}}$ should be synchronous with the falling edge of AFECLK. The $\overline{\text{TXSTR}}$ determines the phase of the AFE's internal sampling clock (AFECLK divided by 2 for POWER=0, and AFECLK divided by 4 for POWER=1). If the $\overline{\text{TXSTR}}$'s phase is inconsistent, noise/distortion is introduced into the converters.

Four AFECLK cycles after $\overline{\text{TXSTR}}$ goes low, the CS6453 is prepared to receive data on TXDATA under control of TXENA. During these first four clock cycles, the previous data samples are being shifted into a zero order hold. Therefore, if TXENA goes high prior to four clock cycles, the new input samples are ignored until the completion of the first four clock cycles.

When TXENA goes high, 48 bits are transferred to the CS6453 using AFECLK. TXDATA is sampled on the rising edge of AFECLK.

SPEAKER DRIVERS

Three speaker outputs are provided: an 8-ohm speaker driver, a 125-ohm earphone driver, and a 1-bit digital speaker out. The 8-ohm speaker output pins allow end-users to monitor the progress of modem call set-up. The CS6453 can drive an 8-ohm speaker directly, via pins SPKR±. The digital speaker signal, output on pin DSPKR, can be connected to an external speaker driver, as might be supported in a PCMCIA application. The DSPKR signal has hysteresis to avoid chatter.

Speaker Output Enable

The desired speaker output signal is selected via bit EPHONE of the control register, and pin SPKOFF. Four configurations are available as shown in Table 3. Non-selected analog outputs are high impedance.

Selection		Output Status		
Speaker Selection bit (EPHONE)	SPKOFF Pin	Speaker	Ear-phone	Digital Speaker
0	0	on	off	on
0	1	off	off	on
1	0	off	on	off
1	1	off	off	off

Table 3. Speaker Output Enable

Speaker Output Level Control

The speaker driver outputs are controlled via the control register. The volume levels can be set with the Sp1 and Sp0 control bits (see Table 2). The relative volume levels are 0 dB (High), -6 dB (Medium), -18 dB (Low), and mute. Note that all of the speakers can be turned off by either setting Sp0 and Sp1 to 0, or by setting pin SPKOFF to logic high and bit EPHONE to 1. Using the former approach is recommended since it achieves the lowest power consumption.

Speaker Source Selection

The signal source for the speaker drivers is selected via the Smode1 and Smode0 control bits. The speaker can be driven with the transmit signal only (Smode1=0, Smode0=1), the receive signal only (Smode1=1,Smode0=0) or a combination of the transmit and receive signals (Smode1=1, Smode0=1). Typically, the "RX only" 8-ohm speaker configuration is used to monitor the modem call in progress. For applications where the hybrid completely cancels the transmit signal, the "TX and RX" configuration can be used.

For telephone emulation applications, the sidetone inputs are selected instead of the transmit outputs when the earphone output, TX± output, and microphone input are all enabled.

MICROPHONE INPUT

The microphone input is selected via the control register (bits Cntl0 & Cntl1). When selected, the MIC± pins are multiplexed into the analog receiver. The MIC+ pin must be AC coupled as shown in Figure 1. The MIC- pin provides the ground for the electret microphone. The RXgain control bits can also be used to select the microphone gain. If the microphone input is not selected then the MIC± pins are high impedance, and the external microphone circuitry is powered down.

LOOPBACKS

Two local loopbacks are provided as shown in the block diagram on the data sheet cover.

The *analog local loopback* connects the output of the transmitter to the input of the receiver's delta-sigma modulator. During analog loopback, the TX± outputs are still active.

The *digital local loopback* connects the 1-bit output of the transmitter's 2nd-order modulator to the input of the receiver's decimation filter. During digital loopback, the TX± outputs are still active.

CONTROL REGISTER

The control register is updated, once per strobe, via the TXDATA input pin. Just as is the case with the input data words, the control words are buffered for one $\overline{\text{TXSTR}}$ period. Therefore the sequence of events is the following: upon the falling edge of TXENA, the contents of the control register is updated with the "old" control bits which were input to the CS6453 following the previous strobe. Several clock periods after the $\overline{\text{TXSTR}}$ transition, "new" control bits are input on TXDATA using AFECLK and TXENA. These new bits are held temporarily in a shift register until the next strobe occurs. The control information input to the CS6453 is shown in Table 2.

The FReset control bit clears all registers in the digital modulator and filters without affecting the control bits. An asserted FReset will cause the transmitter analog outputs to tend toward the supply rails.

RESET

Taking the RESET pin high will reset the internal logic of the CS6453 and set all contents of the control register to 0. Although the rising edge of RESET asynchronously resets all internal logic, the internal reset state is not exited until the first rising edge of AFECLK after RESET is de-asserted. Analog bias voltage settling time must be allowed to elapse before full device operation is ensured (see Switching Characteristics).

The power-up reset also clears the control register. It is recommended however, that the RESET pin be brought high, then low, at least 1 ms after power is applied.

The digital filter's contents can be reset to zero via the FReset bit, located in the control register. The input data should be all zero when removing the FReset condition (FRESET falling to 0) to avoid race conditions between the data and the removal of reset. The control bits may be any value as needed.

POWER DOWN MODE

The CS6453 can be placed in a power-down standby mode by holding AFECLK static for 1 ms. The CS6453 senses the idle AFECLK and stops A/D and D/A conversions, and shuts down the serial I/O ports. Toggling the AFECLK will wake up the CS6453. Analog bias voltage settling must be allowed to elapse before full device operation is ensured (see Switching Characteristics).

SYSTEM CALIBRATION

This section describes how system calibration of receiver gain can be performed. The receiver absolute gain accuracy, before system calibration, is ±5% for the 0 dB gain setting. During calibration, the DSP uses analog loopback to send a signal from the DSP through the transmitter, and then the receiver, and back to the DSP. The transmit gain accuracy is measured. Once the transmit gain is known, the other receiver gains can be calibrated.

More specifically, a transmit gain system calibration can be performed as follows. Select the 0 dB receiver gain setting. Select analog local loopback. While in analog loopback, the DSP transmits a reference signal. The DSP measures the transmit gain by comparing the loopback receive signal to the transmitted reference signal. Once the transmit gain is known, the receive gain for the +6 dB, + 12 dB, and +18 dB gain setting can be measured in a similar manner.

APPLICATION NOTES

Table 4 summarizes the operating modes.

Telephone Emulation

The CS6453 can connect the DSP to both a telephone handset and a telephone line. In this application, the DSP can emulate the functions of a telephone set, including generating DTMF tones, and recognizing telephony signaling and supervision.

The telephone line is connected via TX±, ST±, and RX± to the Data Access Arrangement. See Figure 5. The handset earphone is connected to EAR±. The handset mouthpiece is connected to MIC±.

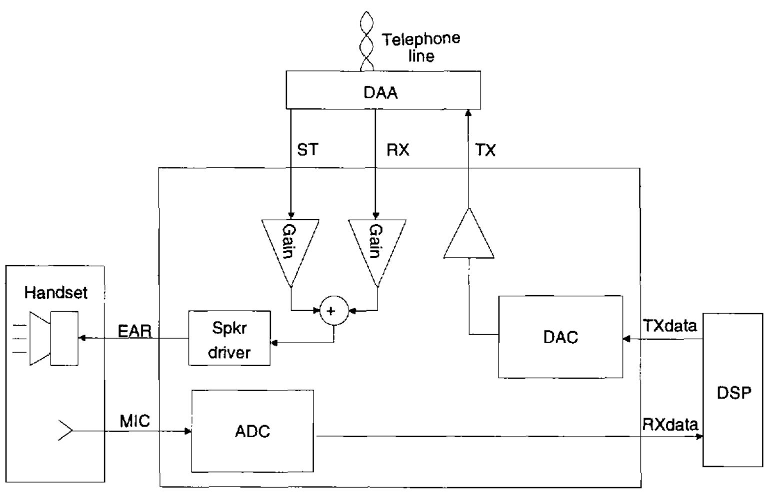


Figure 5. Telephone Emulation

Mode	Active External Interfaces	Control Selections: ADC Source (Cntl1, Cntl0)	Control Selections: Speaker Source (Smode1, Smode0)	Control Selections: Trans-mitter off (TXOFF)	Control Selections: Speaker off (SPKOFF)	Control Selections: Speaker Selection (EPHONE)	Input Status: Micro-phone (MIC±)	Input Status: Receiver (RX±)	Output Status: Speaker (SPK±)	Output Status: Earphone (EAR±)	Output Status: Digital Speaker (DSKPR)	Output Status: Trans-mitter (TX±)	Output Status: Source of Handset Sidetone
Modem	DSP DAA	RX: 0,0	off: 0,0	0	1	1	off	to DAA	off	off	off	to DAA	NA
Modem with call Monitor	DSP DAA Speaker	RX: 0,0	RX only or TX & RX 1,0/1	0	0	0	off	to DAA	on; to 8-ohm speaker	off	on; not used	to DAA	NA
PCMCIA Modem	DSP DAA DSPKR	RX: 0,0	RX only or TX & RX 1,0/1	0	1	0	off	to DAA	off	off	on: to PCMCIA pin	to DAA	NA
Telephone Emulation	DSP DAA Handset	MIC: 1,1	ST & RX: 1,1	0	0	1	to handset micro-phone	to DAA	off	on: to 125-ohm earphone	off	to DAA	ST±, RX±
Speaker-phone	DSP DAA Speaker	MIC: 1,1	RX only: 1,0	0	0	0	to micro-phone	to DAA	on to 8-ohm speaker	off	on; not used	to DAA	NA
Mobile Handset	DSP Handset	MIC: 1,1	TX only: 0,1	1	0	1	to micro-phone	off	off	on: to 125-ohm earphone	off	off	TX±
Answer. Machine: Record	DSP DAA	RX: 0,0	off: 0,0	1	1	1	off	to DAA	off	off	off	off	NA
Answer. Machine: Playback	DSP Speaker	DC: ignored by DSP	TX only 0,1	1	0	0	DC	DC	on; to 8-ohm speaker	off	on; not used	off	NA
Business Audio	DSP Speaker Micro-phone	MIC: 1,1	TX only: 0,1	1	0	0	to micro-phone	off	on; to 8-ohm speaker	off	on; not used	off	NA

Table 4. Application Suggestions (NA=not applicable; DC=don't care)

The following control options are selected via the control register. The microphone input is enabled (Cntrl=1, Cntl0=1). The earphone drive is enabled (EPHONE=1). Side tone is provided by the speaker configuration of "ST and RX" (Smode1=1 and Smode0=1).

The sidetone signal is derived from the transmit signal via an external resistor divider. The resistor divider is external so that the sidetone signal strength can be adjusted to a particular level.

Handset Support

When the DSP needs to connect to the handset and not to a DAA (for example, in a portable radio), the transmit driver can be powered down by setting TXOFF high, cutting power dissipation by 50% (see Figure 6).

Answering Machine Application

The CS6453 can be used to playback recorded messages or screen incoming telephone calls. The audio output is provided over the 8 Ω speaker pins (SPKR±). For the answering machine playback mode, the "TX only" (Smode1=0, Smode0=1) 8 Ω speaker configuration is used. For the call screening option the "TX and RX" (Smode1=1, Smode0=1) configuration is used.

Business Audio Application

The CS6453 supports business audio application. Because of the bandwidth requirements of business audio, it is necessary to change the filter bandwidths to 10 kHz (set control bit BAudio=1), and use input/output sample rates of 38.4 kHz (which is twice the normal sample rate) on pins $\overline{TXSTR}$ and $\overline{RXSTR}$.

Typically, the audio input is received on MIC±, and the audio is output via pins SPKR± or EAR±.

POWER SUPPLY AND GROUNDING

The CS6453 can operate over the entire 3V to 5.5V power supply range.

The CS6453, along with associated analog circuitry, should be positioned in an isolated section of the circuit board, and have its own, separate, ground plane. The best solution is to place the

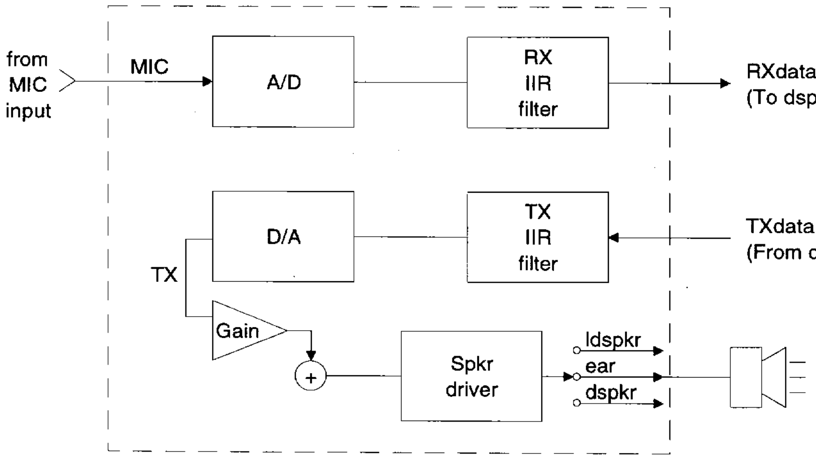


Figure 6. Mobile Handset

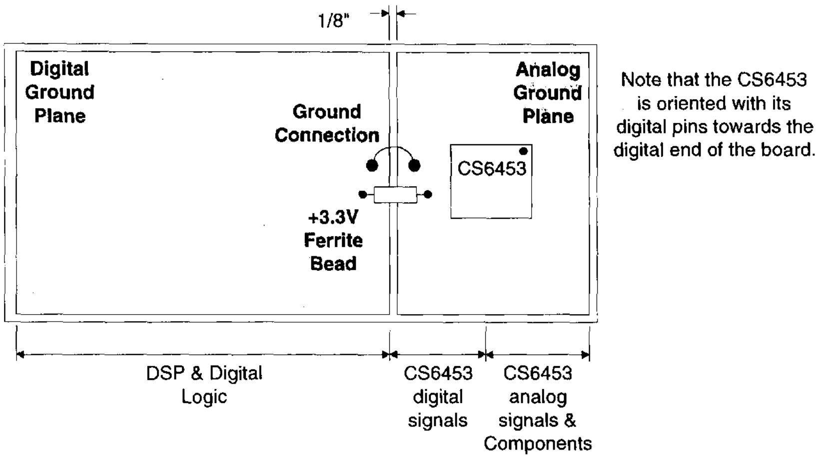


Figure 7. Suggested Layout Guidelines

entire chip on a solid ground plane as shown in Figure 7. A single connection between the CS6453 analog ground and the board digital ground should be positioned as shown in Figure 7. The TXGND, RXGND, LSGND and DGND pins must be externally connected with zero impedance between them.

Preferably, the CS6453 should also have its own power plane, isolated from the power plane for the rest of the board by a ferrite bead, as shown in Figure 7. The VD+ power supply can be derived from the TXV+, RXV+ and LSV+ supplies using the 10 ohm resistor shown in Figure 1. However, the VD+, TXV+, RXV+ and LSV+ supplies must stay within a diode drop of each other, or the chip could be permanently damaged.

Alternatively, a separate +3.3V analog supply may be used for TXV+, RXV+, LSV+.

The supply pins should be decoupled to their respective grounds as shown in Figure 1. Decoupling should be accomplished with 0.01 µF ceramic and 1.0 µF capacitors.

There are no power supply sequencing requirements.

Layout of through-hole boards

This section assumes: a surface-mount socket, leaded decoupling capacitors, and a fairly solid ground plane in either the bottom or inter-layer.

There should be a solid ground plane under the CS6453 on the same layer as the CS6453 and it should connect all ground pins with thick traces providing the absolute lowest impedance between ground pins. The decoupling capacitors should be placed as close as possible to the device which, in this case, is the socket boundary. The lowest value capacitor should be placed closest to the CS6453. Vias should be placed near the TXGND, RXGND, LSGND and DGND pins, under the IC, and should attach to the solid ground plane on another layer. The negative side of the decoupling capacitors should also attach to the same solid ground plane. Traces and vias bringing power to the CS6453 should be large, which minimizes the impedance.

The trace layer (top layer) should have ground plane fill in-between the traces to minimize coupling into the analog section.

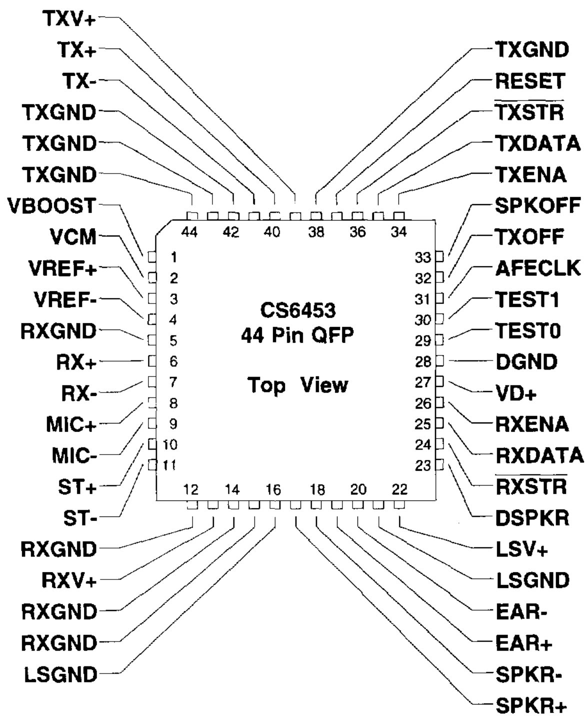
If using a through-hole socket, effort should be made to find a socket with minimum height, which will minimize the socket impedance.

Layout of surface-mount boards

If using all surface-mount components, the decoupling capacitors should be placed on the same layer as the CS6453. The vias should attach to the appropriate power and ground layers. Traces and vias bringing power to the CS6453 should be as large as possible to minimize the impedance.

Crystal publishes an Application Note entitled "Layout Rules for Analog-to-Digital and Digital-to-Analog Converters It is reprinted in the application note section of this book.

PIN DESCRIPTIONS



Power Supplies

VD+ - Digital Power, PIN 27.
Digital supply voltage. Nominally 3.3 volts.

DGND - Digital Ground, PIN 28.
Digital ground reference.

TXV+ - Transmitter Power, PIN 39.
Transmitter analog supply voltage. Nominally 3.3 volts.

TXGND - Transmitter Ground, PINS 38, 42, 43 and 44.
Transmitter analog ground reference.

RXV+ - Receiver Power, PIN 13.
Receiver analog supply voltage. Nominally 3.3 volts.

RXGND - Receiver Ground, PINS 5, 12, 14 and 15.
Receiver analog ground reference.

LSV+ - 8 Ω Speaker Power, PIN 22.
8 Ω Speaker supply voltage. Nominally 3.3 volts.

LSGND - 8 Ω Speaker Ground, PINS 16 and 21.
8 Ω speaker ground reference.

Clock

AFECLK - AFE Clock Input, PIN 31.
Must be driven by a 5.5296 MHz CMOS clock signal.

Inputs

ST+, ST- - Sidetone Inputs, PINS 10 and 11.
Sidetone differential inputs. Used by the CS6453 when earphone outputs, microphone inputs, and transmitter outputs are all enabled.

RX+, RX- - Analog Inputs, PINS 6 and 7.
Analog receiver differential inputs.

MIC+, MIC- - Microphone Inputs, PINS 8 and 9.
Microphone differential inputs.

$\overline{\text{TXSTR}}$ - Transmitter Data Input Strobe, PIN 36.
Control for transmitter serial input interface. A transition to low is a request for the CS6453 to receive two 24-bit words on TXDATA.

TXDATA - Transmitter Data Input, PIN 35.
Serial data input pin. Data is sampled on the rising edge of AFECLK. Includes two's complement format data to be transmitted plus update for the control register. See Table 1 for the format of this data.

TXENA - Transmitter Data Input Enable, PIN 34.
The rising edge indicates the start of serial data input on the TXDATA pin. The falling edge indicates the end of serial data input.

$\overline{\text{RXSTR}}$ - Receiver Data Input Strobe, PIN 24.
Control for receiver serial output interface. A transition to low is a request for the CS6453 to output two 24-bit words on RXDATA.

RESET - Reset, PIN 37.
Resets the CS6453, and clears of the control register.

TXOFF -Transmitter Off Select, PIN 32.
If set to logic high, the CS6453 powers down the TX± transmit driver.

TEST0, TEST1 - Factory Test Select, PIN 29, 30.
These pins must be held low for normal operation.

SPKOFF-SPEAKER DRIVER OFF, PIN 33.
If set to logic high, the CS6453 powers down the speaker driver.

Outputs

TX+, TX- - Transmitter Analog Outputs, PINS 40 and 41.
Analog transmitter differential outputs.

RXENA - Receiver Digital Output Enable, PIN 26.
The rising edge indicates the start of serial data output on the RXDATA pin. The falling edge indicates the end of serial data output.

RXDATA - Data Output, PIN 25.
Receiver serial data output pin. Converted data is clocked out on this pin by the falling edge of AFECLK. Data is sent MSB first in two's complement format.

SPKR+, SPKR- - 8-ohm Speaker Outputs, PINS 17 and 18.
Differential output driver pins for external 8-ohm speaker.

EAR+, EAR- - Earpiece Outputs, PINS 19 and 20.
Differential output driver pins for external 125-ohm telephone handset speaker.

DSPKR - Digital Speaker Drive Output, PIN 23.
This pin is a quantized (1-bit) representation of the speaker drive first stage output.

VREF+, VREF- - Voltage Reference Buffer, PINS 3 and 4.
The voltage references provide an internal reference. VREF+ allows the reference to be bypassed using an external 1.0 µF capacitor. VREF- should be connected to ground.

VCM - Voltage Common Mode, PIN 2.
The common mode voltage provides an external mid-scale reference for the external differential analog circuitry, and should be used, for example, as a reference for the external microphone.

VBOOST - Voltage Boost, PIN 1.
This pin is part of the internal 3V-to-5V charge pump circuit, and should be bypassed to ground with an external 1 µF cap. The nominal voltage on this pin is two times VREF. This pin should be connected only to the specified capacitor.

PARAMETER DEFINITIONS

Resolution

The number of bits in the input words to the DACs, and in the output words from the ADCs.

Dynamic Range

Dynamic Range is the ratio of the rms value of a full scale signal to the lowest obtainable noise floor. It is measured by comparing a full scale signal to the noise floor with grounded inputs. Units in dB.

Total Harmonic Distortion

THD is the ratio of a rms full-scale signal to the rms sum of the first five harmonic components. 1 kHz is used for testing. Units in dB.

Offset Error

For the ADC, the deviation from the zero-voltage differential input voltage needed to produce an ideal mid-scale output code. For the DAC, the deviation of the output from differential zero with mid-scale input code. Units in volts for the DAC and the ADC.

Monoticity

The DAC is monotonic if every increasing input code produces a continuously increasing analog output (i.e, a differential linearity error < ±1LSB).