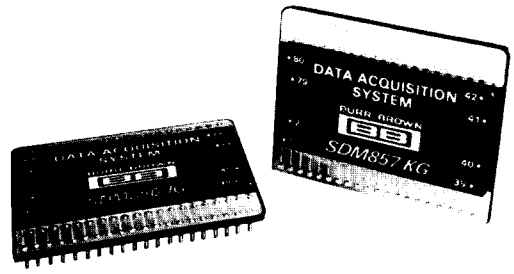
BURR-BROWN®



SDM856
SDM857

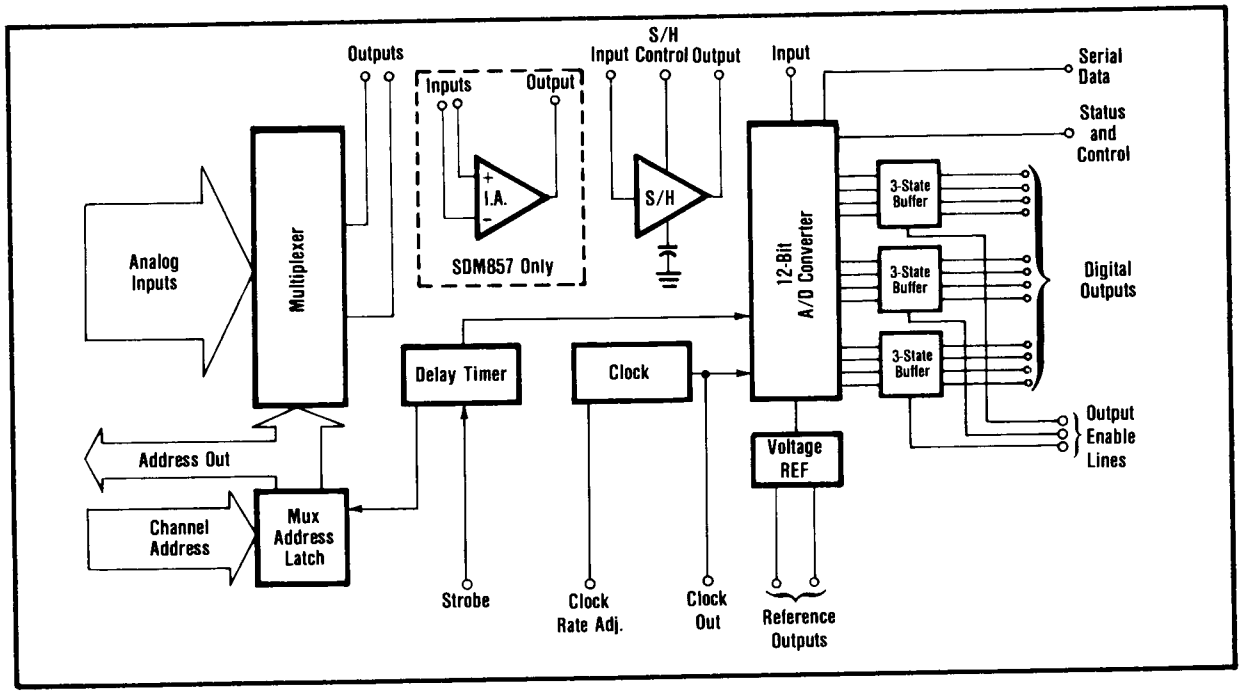
HYBRID DATA ACQUISITION SYSTEM

FEATURES

- MINIATURE SIZE
- LOW COST
- 12-BIT, ±0.012% LINEARITY ERROR
- INSTRUMENT AMP OPTION
- LOW LEVEL INPUTS (SDM857)
- SELECTABLE 16 SINGLE, 8 DIFFERENTIAL INPUTS
- THREE-STATE OUTPUT BUFFERS
- THROUGHPUT RATES (SDM857 Overlap Mode)
  - 8-Bit Accuracy: 70kHz
  - 10-Bit Accuracy: 32kHz
  - 12-Bit Accuracy: 29kHz

DESCRIPTION

The SDM856 and SDM857 are complete data acquisition systems contained in a miniature 2.2" x 1.7" x 0.22" ceramic package. These systems offer all the functions available in large modular data acquisition systems and are available with an optional internal instrumentation amplifier (SDM857). Inputs as low as ±10mV can be accepted by the SDM857; thermocouples, strain gages, and other low level signal sensors don't require external signal conditioning. Both models are fully expandable from the basic 16 channel single-ended or 8 channel differential input capability. Digital resolution is 12 bits with accuracy of ±0.024% at a throughput rate of 29kHz (SDM856KG).



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PDS-402C

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SYSTEM DESCRIPTION

SDM857 contains all components necessary to multiplex and convert analog signals as low as ±10mV and as high as ±5V into equivalent digital outputs. Throughput sampling rates are from 29kHz (12-bit resolution) to 70kHz (8-bit resolution) in the overlap mode of operation. A complete low drift instrumentation amplifier allows selection of gains from 2 to 500 with one external resistor. SDM856 is identical to SDM857, but does not include the instrumentation amplifier. This provides the option of adding an external instrumentation amplifier for specific requirements such as high speed, digital programming, etc. Both models can be configured to accept either 8-channel differential or 16-channel single-ended signals and can be expanded almost without limit with external multiplexers. Three-state outputs are provided for easy interface to microprocessor and other bus-structured systems. Figure 1 illustrates all system components which are described in the following paragraphs.

ANALOG MULTIPLEXER

The analog multiplexer consists of two CMOS integrated circuits. Pin interconnects are used to select 16-channel single-ended or 8-channel differential operation. In single-ended operation the multiplexer can be used in a pseudo-differential mode by connecting the amplifier inverting input to common remote signal ground. Channel selection is made by an internally latched 3- or 4-bit binary word, for differential or single-ended operation respectively.

INSTRUMENTATION AMPLIFIER (SDM857 only)

Offering low drift and high accuracy, the internal instrumentation amplifier may be programmed by a single external resistor for gains from 2 to 500. With gain programming pins open, the gain is 2.

SAMPLE/HOLD

A complete stand-alone circuit, the sample/hold amplifier features buffered output, 10μsec acquisition time, and 100nsec aperture time.

Input, output, and mode control lines are brought out to separate pins. This allows maximum system flexibility for performing functions, such as automatic gain ranging, with no loss of aperture time.

ANALOG-TO-DIGITAL CONVERTER

The ADC is a 12-bit, 25μsec converter with 0.01% linearity error. Its features include positive and negative reference voltage outputs, external gain and offset adjustments, straight binary or two's complement output, serial data and clock outputs, status output, a short cycle feature, and a clock rate control for higher throughput rates at lower resolution or accuracy.

THREE-STATE OUTPUT BUFFERS

Digital outputs of the ADC are internally buffered by LSTTL three-state buffers. Three separate enable lines are brought out for easy interfacing to 4-, 8- or 16-bit data buses. $\overline{\text{MSB}}$ and BUSY are also buffered by separate three-state devices, each with its own enable line.

ADDRESS LATCH

Outputs of the 4-bit LSTTL register latch are connected to the address inputs of the multiplexer. This latch serves as an address storage register for the selected analog input. It may be loaded through 4 address inputs. Other inputs are LOAD and $\overline{\text{CLEAR}}$. The 3 least significant bits are used for 8-channel differential mode addressing.

DELAY TIMER

A delay timer allows settling time for the multiplexer, amplifier, and sample/hold circuits before conversion begins. The delay is adjustable over a wide range by use of an external resistor or capacitor. This allows for longer settling time of the instrumentation amplifier when operating at high gains, or shorter settling time for lower resolution operation.

CHANNEL EXPANSION

The number of analog input channels of the SDM856 and SDM857 can be easily increased by using Burr-Brown's MPC8D (8-channel differential) and MPC16S (16-channel single-ended) multiplexers. These are latch-free devices which contain internal binary decoding at TTL or MOS levels and may be integrated into a system with minimal external logic.

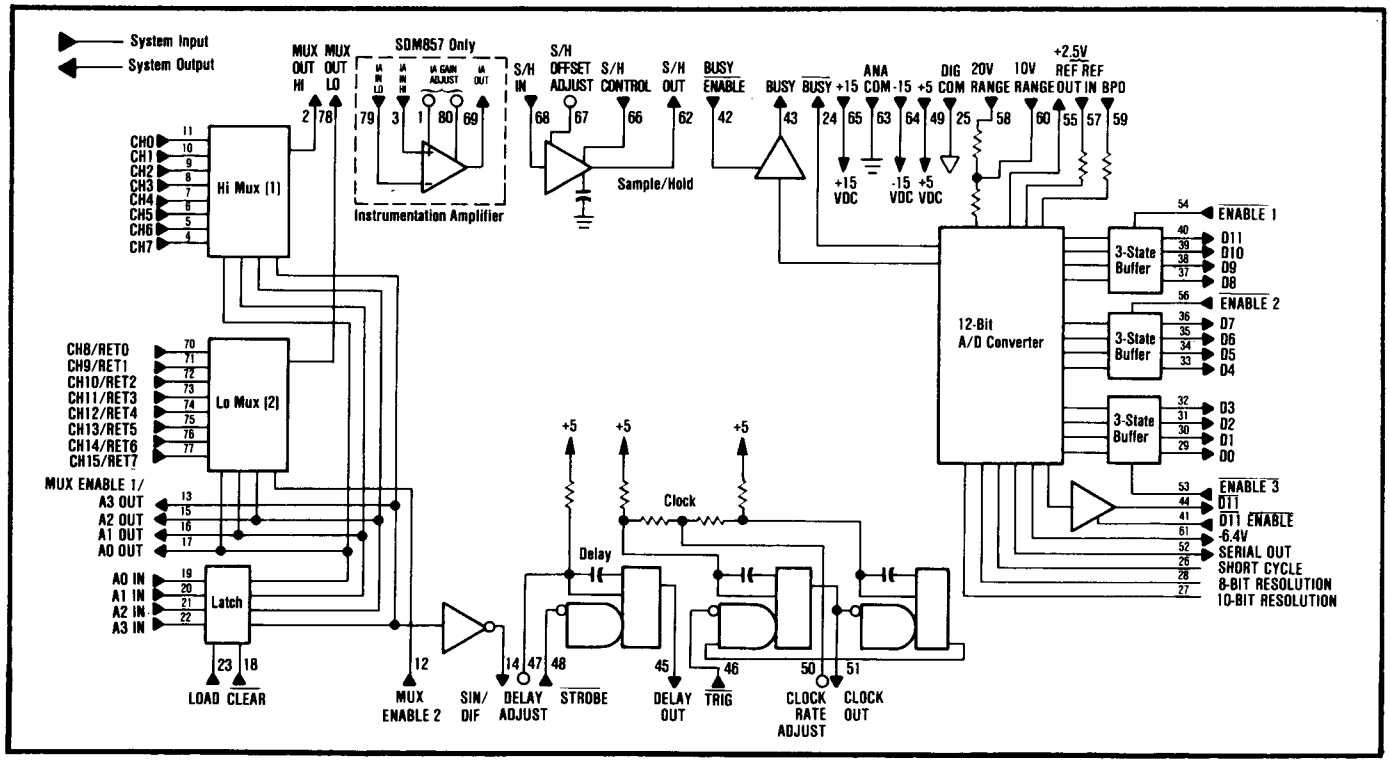


FIGURE 1. SDM856/857 Block Diagram.

SYSTEM PERFORMANCE

SDM856 and SDM857 are configured for random channel selection. With the addition of an external counter they can be configured to continuously sequence through all analog channels or sequence through all analog channels on command from an external trigger.

With the appropriate 4-bit (single-ended) or 3-bit (differential) channel address on the latch inputs, and DELAY OUT (pin 45) tied to the LOAD input (pin 23), a negative going edge is applied to the $\overline{\text{STROBE}}$ input (pin 48). This starts the delay timer, latches the multiplexer address, and allows the input signal to pass through the multiplexer, instrumentation amplifier and sample/hold and settle to its final value before starting the A/D conversion. The DELAY OUT signal (pin 45) is also connected to the $\overline{\text{TRIG}}$ input (pin 46) and the A/D conversion is initiated on the negative-going edge. The S/H CONTROL input (pin 66) is connected to $\overline{\text{BUSY}}$ (pin 24) so that the sample/hold is in the HOLD mode during the A/D conversion.

By using overlap programming the settling time effects of the analog multiplexer and instrumentation amplifier can be reduced, extending throughput sampling rates up to 29kHz for 12-bit and 70kHz for 8-bit resolution (ADC short-cycled). This mode of operation is most useful when converting low level inputs to accommodate the increased settling time of the instrumentation amplifier. Overlap programming is accomplished by connecting $\overline{\text{BUSY}}$ to $\overline{\text{STROBE}}$ and S/H CONTROL; DELAY OUT to LOAD and $\overline{\text{TRIG}}$. In this mode of operation the address of the next channel to be converted is latched and the output of the instrumentation amplifier allowed to settle to a new value during the present conversion.

DIGITAL INPUT SPECIFICATIONS

Address Inputs (A0 - A3)	One standard LSTTL load, positive true
Address Coding	4-bit binary
LOAD	One standard LSTTL load, positive true, address loaded on positive edge.
$\overline{\text{CLEAR}}$	One standard LSTTL load, negative true, low level clears address latch.
$\overline{\text{STROBE}}$	One standard LSTTL load, high-to-low transition triggers the delay timer.
$\overline{\text{TRIG}}$	One standard LSTTL load, a negative going edge initiates the A/D conversion.
SHORT CYCLE	One standard LSTTL load, logic 1 for 12-bit resolution. Connect to "8-bit" or "10-bit" for 8- or 10-bit resolution.
$\overline{\text{ENABLE 1}}$, $\overline{\text{ENABLE 2}}$, $\overline{\text{ENABLE 3}}$, $\overline{\text{D11 ENABLE}}$, BUSY $\overline{\text{ENABLE}}$	One standard LSTTL load, a low level enables the 3-state output.
S/H CONTROL	TTL compatible, 10μA maximum input current. Logic 0 = Hold mode, Logic 1 = Sample (track) mode.
MUX ENABLE 2	TTL compatible, 2μA input current, Logic 0 enables multiplexer 2 (channels 8-15).

DIGITAL OUTPUT SPECIFICATIONS

Parallel Data Outputs	5 standard TTL loads, positive true, 3-state.
Serial Output	2 standard TTL loads, positive true, NRZ, time serial data output beginning with D11 (see Timing Diagram).
$\overline{\text{D11}}$	5 standard TTL loads, positive true, 3-state.
$\overline{\text{BUSY}}$	5 standard TTL loads, low during A/D conversion.
BUSY	5 standard TTL loads, high during A/D conversion, 3-state
CLOCK OUT	5 standard TTL loads, for synchronizing serial out data (see Timing Diagram).
Address Outputs (A0 - A3)	5 LSTTL loads, positive true
DELAY OUT	5 standard TTL loads, high during delay period, triggered by Strobe input.
SIN/DIF	5 LSTTL loads, high while addressing channels 0-7, low while addressing channels 8-15.

SPECIFICATIONS

ELECTRICAL

Typical at T_A = +25°C and rated power supplies unless otherwise noted.

MODEL	SDM856/SDM857			
TRANSFER CHARACTERISTICS	**MIN**	**TYP**	**MAX**	**UNITS**
Resolution	12			Bits
Number of Analog Channels		16SIN/8DIF		
Throughput Rate (Normal Mode)				
SDM856JG	33	35		kHz
SDM856KG	25	27		kHz
SDM857JG	22	24		kHz
SDM857KG	18	20		kHz
Throughput Rate (Overlap mode)				
SDM856JG	38	40		kHz
SDM856KG	27	29		kHz
SDM857JG	38	40		kHz
SDM857KG	27	29		kHz
ANALOG INPUTS				
SDM Input Voltage Range		±5		V
Mux Input Voltage Range				
Absolute max without damage			±20	V
For linear operation			±6	V
Mux Input Impedance, OFF Channel		$5 \times 10^9 \| 10$		Ω||pF
Mux Input Impedance, ON Channel		1800||7		Ω||pF
Amplifier Characteristics				
(SDM857 only)				
Input Impedance		$5 \times 10^9 \| 3$		Ω||pF
Gain Range	2		500	
Gain Equation		$G = 2 + (20k\Omega/R_{EXT}$[1]$)$		
Input Bias Current at +25°C			±50	nA
0°C to +70°C		±1.1		nA/°C
Offset Current at +25°C			±20	nA
0°C to +70°C		±0.6		nA/°C
Input Offset Voltage		±0.1		mV
Input Offset Voltage Drift (G > 100)		±4	±6	µV/°C
Output Noise (10Hz – 10kHz)				
G = 100, R_S – 500Ω		400		µV, rms
Common-mode Rejection (DC)				
G = 2		90		dB
G = 1000		97		dB
Sample/Hold DC Characteristics				
Input Impedance		$10^{10} \| 3$		Ω||pF
Bias Current		50		nA
Output Offset Voltage		7		mV
REFERENCE VOLTAGES				
Output Voltage: Positive	+2.490	+2.500	+2.510	V
Negative	−6.0	−6.4	−6.8	V
Temperature Coefficient				
(each output)		±5	±10	ppm/°C
Current available for External Loads				
Positive[2]	0			µA
Negative	−200			µA
ACCURACY				
Throughput Accuracy				
0 to +5V, ±5V ranges JG			±0.048	% of FSR[2]
0 to +5V, ±5V ranges KG			±0.024	% of FSR
0 to +20mV, ±10mV JG				
(SDM857 only)			±0.11	% of FSR
0 to +20mV, ±10mV KG				
(SDM857 only)			±0.08	% of FSR
Linearity (G = 1): JG			±0.024	% of FSR
KG			±0.012	% of FSR
Differential Linearity (G = 1): JG		±0.024	±0.048	% of FSR
KG		±0.012	±0.024	% of FSR
Quantizing Error			±0.012	% of FSR
System Gain Error[4]		±0.1	±0.3	%
System Offset Error[4]		±0.1	±0.3	% of FSR
Power Supply Sensitivity: +15V		±0.0007		%/%ΔV
−15V		±0.0007		%/%ΔV
+5V		±0.001		%/%ΔV

MODEL	SDM856/SDM857			
TEMPERATURE STABILITY	**MIN**	**TYP**	**MAX**	**UNITS**
System Accuracy Drift[5]: Unipolar			±25	ppm/°C
Bipolar			±20	ppm/°C
Linearity Drift			±2	ppm of FSR/°C
DYNAMIC ACCURACY				
Sample/Hold Characteristics				
Aperture Time		100		nsec
Acquisition Time		10		µsec
Feedthrough (10V step)		±1.4		mV
Amplifier Characteristics				
(SDM857 only)				
Amplifier CMRR at 60Hz, G = 2		90		dB
G = 500		95		dB
Amplifier Overload Recovery Time		200		µsec
OUTPUTS				
Digital Output Coding		Binary, Offset Binary, Two's Complement		
Serial Output Coding		Non-return to zero (NRZ)		
ADC Conversion Time[6]		25	30	µsec
Clock Frequency[6]		520		kHz
Delay[7]: SDM856		15		µsec
SDM857		30		µsec
POWER REQUIREMENTS				
Rated Voltage for Specified Accuracy	±14.5	±15	±15.5	
	+4.75	+5	+5.25	V
Quiescent Current				
SDM856, +15VDC		+10	+20	mA
SDM856, −15VDC		−35	−50	mA
SDM856, +5VDC		+120	+140	mA
SDM857, +15VDC		+15	+25	mA
SDM857, −15VDC		−40	−55	mA
SDM857, +5VDC		+120	+140	mA
Power Dissipation: SDM856		1300	1750	mW
SDM857		1400	1900	mW
ENVIRONMENTAL				
Specification Temperature Range	0		+70	°C
Storage Temperature Range	−55		+100	°C

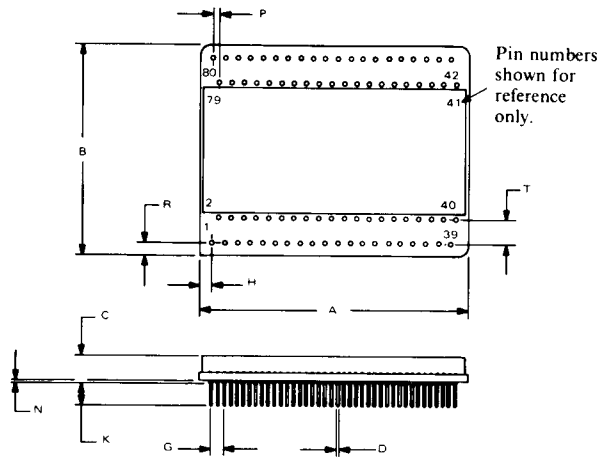
NOTES:
1. R_{EXT} is the external gain-setting resistor. (Connect between pins 1 and 80.)
2. External loading of the +2.5V reference output is not recommended.
3. FSR means Full Scale Range, e.g., FSR is 10V for ±5V range.
4. Adjustable to zero.
5. Includes gain, offset, and linearity drifts.
6. Conversion time and clock frequency can be exteranlly adjusted from 13µsec (f_{clock} = 1.0MHz) to 110µsec (f_{clock} = 118kHz). Conversion times are for 12-bit resolution.)
7. Can be externally adjusted from 3µsec to 300µsec.

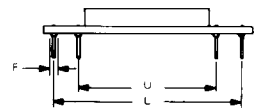
PIN DESIGNATIONS

IA GAIN ADJUST	*1	*80	IA GAIN ADJUST
MUX OUT HI	2	*79	IA IN LO
IA IN HI	*3	78	MUX OUT LO
CH7	4	77	CH15 RET 7
CH6	5	76	CH14 RET6
CH5	6	75	CH13 RET5
CH4	7	74	CH12 RET4
CH3	8	73	CH11 RET3
CH2	9	72	CH10 RET2
CH1	10	71	CH9 RET1
CH0	11	70	CH8 RET0
MUX ENABLE 2	12	*69	IA OUT
MUX ENABLE 1/A3 OUT	13	68	S/H IN
SIN/DIF	14	67	S/H OFFSET ADJUST
A2 OUT	15	66	S/H CONTROL
A1 OUT	16	65	+15VDC
A0 OUT	17	64	-15VDC
$\overline{\text{CLEAR}}$	18	63	ANA COM
A0 IN	19	62	S/H OUT
A1 IN	20	61	-6.4V REF OUT
A2 IN	21	60	10V RANGE
A3 IN	22	59	BPO
LOAD	23	58	20V RANGE
$\overline{\text{BUSY}}$	24	57	+2.5V REF IN
DIG COM	25	56	$\overline{\text{ENABLE 2}}$
SHORT CYCLE	26	55	+2.5V REF OUT
10-BIT RESOLUTION	27	54	$\overline{\text{ENABLE 1}}$
8-BIT RESOLUTION	28	53	$\overline{\text{ENABLE 3}}$
D0 (LSB)	29	52	SERIAL OUT
D1	30	51	CLOCK OUT
D2	31	50	CLOCK RATE ADJUST
D3	32	49	+5VDC
D4	33	48	$\overline{\text{STROBE}}$
D5	34	47	DELAY ADJUST
D6	35	46	$\overline{\text{TRIG}}$
D7	36	45	DELAY OUT
D8	37	44	$\overline{\text{D11}}$
D9	38	43	BUSY
D10	39	42	BUSY $\overline{\text{ENABLE}}$
D11 (MSB)	40	41	$\overline{\text{D11}}$ $\overline{\text{ENABLE}}$

*For SDM857 only. Make no connection in SDM856.

MECHANICAL





NOTE:
Leads in true position within .015" (.38mm)R at MMC at seating plane.

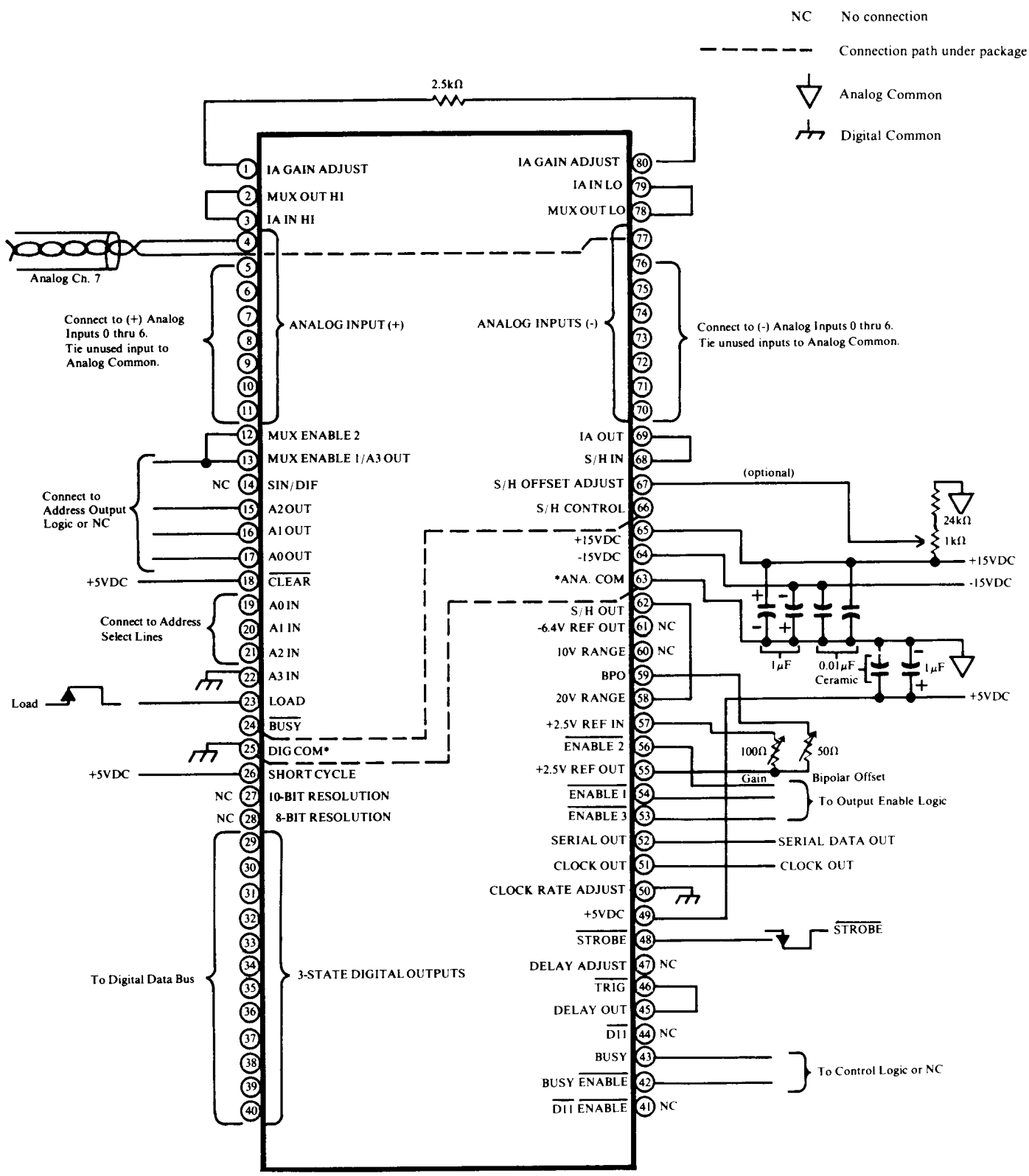
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	2.120	2.180	53.85	55.37
B	1.670	1.720	42.42	43.69
C	.170	.230	4.32	5.84
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.100 BASIC		2.54 BASIC	
K	.150	.250	3.81	6.35
L	1.500 BASIC		38.1 BASIC	
N	.002	.010	0.05	0.25
P	.050 BASIC		1.27 BASIC	
R	.100 BASIC		2.54 BASIC	
T	.200 BASIC		5.08 BASIC	
U	1.100 BASIC		27.94 BASIC	

MATERIAL: Ceramic
WEIGHT: 32 grams (1.2 oz.)
PINS: Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2)
MATING CONNECTOR: 2350MC (Set of four 20-pin strips) or 0422MC (assembled unit).

DESCRIPTION OF PIN FUNCTIONS

NUMBER	DESIGNATION	DESCRIPTION
Pin 1	IA GAIN ADJUST	(SDM857 only). By connecting a resistor between pin 1 and pin 80 the gain of the internal instrumentation amplifier can be varied as follows: $\text{Gain} = 2 + (20\text{k}\Omega/R_{EXT})$ where R_{EXT} is the gain setting resistor. The IA is factory adjusted for a gain of 2 without any external resistor. Important: If a gain greater than 10 is required an external capacitor must be connected from "DELAY ADJ." (pin 47) to +5VDC. This increases an internal delay to allow for the increased settling time of the instrumentation amplifier (see page 12). For SDM856 make no connection.
Pin 2	MUX OUT HI	High output of the analog input multiplexer. Connect to pin 3 (IA IN HI) for differential operation. Connect to pin 78 (MUX OUT LO) and pin 3 (SDM857) or (S/H IN) pin 68 (SDM856) for single-ended input operation.
Pin 3	IA IN HI	(SDM857 only). Positive input of the internal instrumentation amplifier. Connect to pin 2 (MUX OUT HI) for normal operation. For SDM856 make no connection.
Pins 4 thru 11	CH7-CH0	The first 8 (of 16) analog inputs for single-ended operation or the 8 positive inputs for 8-channel differential input operation.
Pin 12	MUX ENABLE 2	Connect to pin 14 (SIN/DIF) for single-ended input operation. Connect to pin 13 (MUX ENABLE 1) for differential input operation.
Pin 13	MUX ENABLE 1/ A3 OUT	Leave open for single-ended input operation. Connect to pin 12 (MUX ENABLE 2) for differential input operation. Also, A3 output line.
Pin 14	SIN/DIF	Single/Differential input operation. Connect to pin 12 (MUX ENABLE 2) for single-ended operation. Leave open for differential input operation.
Pins 15, 16, 17	A0 OUT - A2 OUT	Output lines from input channel address latch (A3 OUT is on pin 13).
Pin 18	$\overline{\text{CLEAR}}$	A low on this line clears the address latch causing the SDM856/857 to address channel 0 regardless of the information present on AO IN - A3 IN. Connect to +5VDC or to user logic circuitry.
Pins 19, 20, 21, 22	AO IN - A3 IN	Address lines that select one of 16 analog input signals (CH0-CH15). 0000 selects channels 0 and 1111 selects channel 15. Connect A3 to ground for 8-channel differential operation. The address is latched with a positive TTL edge on the LOAD (pin 23).

Pin 23	LOAD	A positive TTL edge on this pin latches the input channel address present on A0 IN - A3 IN (pins 19, 20, 21, 22).
Pin 24	$\overline{\text{BUSY}}$	This signal will be low during the A/D conversion (≈25μsec). Output data is not valid while this signal is low. Connect to S/H CONTROL (pin 66).
Pin 25	DIG COM	Digital common. Connect to ANA COM (pin 63) as close to the SDM856/857 as possible.
Pin 26	SHORT CYCLE	Ths pin allows short cycling the A/D converter for lower resolutions thereby obtaining faster conversion times. Connect to +5VDC (pin 49) for 12-bit resolution, (pin 27) for 10-bit resolution, or (pin 28) for 8-bit resolution.
Pin 27	10-BIT RESOLUTION	To short cycle to 10-bit resolution connect to pin 26. Otherwise, make no connection.
Pin 28	8-BIT RESOLUTION	To short cycle to 8-bit resolution, connect to pin 26. Otherwise, make no connection.
Pins 29 thru 40	D0-D11	12-bit data bus. 3-state low power Schottky TTL-compatible.
Pin 41	$\overline{\text{D11}}$ $\overline{\text{ENABLE}}$	$\overline{\text{D11}}$ (pin 44) is enabled when $\overline{\text{D11}}$ $\overline{\text{ENABLE}}$ is low.
Pin 42	BUSY $\overline{\text{ENABLE}}$	BUSY (pin 43) is enabled when BUSY $\overline{\text{ENABLE}}$ is low.
Pin 43	BUSY	3-state output that will be high only while an A/D conversion is in process. Output data is not valid while this signal is high.
Pin 44	$\overline{\text{D11}}$	$\overline{\text{MSB}}$. Use instead of D11 when two's complement output is required.
Pin 45	DELAY OUT	This pulse is used to delay the beginning of the A/D conversion to allow for the settling of the multiplexer, instrumentation amplifier, and sample/hold.
Pin 46	$\overline{\text{TRIG}}$	A negative TTL edge on this pin initiates the A/D conversion. Connect to DELAY OUT (pin 45).
Pin 47	DELAY ADJUST	When the SDM856/857 is addressed, an internal delay of approximately 30μsec (SDM857) or 15μsec (SDM856) is initiated to allow for multiplexer, instrumentation amplifier, and sample/hold settling time. When the IA is operated with gain > 10 this delay must be increased to allow for the increased settling time of the IA. (see Table IV and page 14. The delay can also be shortened for faster lower-resolution operation.
Pin 48	$\overline{\text{STROBE}}$	A negative TTL edge on this pin initiates the DELAY OUT pulse.
Pin 49	+5VDC	+5VDC at 140mA maximum, 120mA typical.
Pin 50	CLOCK RATE ADJUST	Varying the voltage at this pin changes the clock frequency and thereby changes the conversion speed of the A/D converter. Connect to DIG COM (pin 25) for 12-bit operation (25μsec A/D conversion time). Connect to +5VDC for 10-bit operation and connect to +15VDC for 8-bit operation. (see page 13).
Pin 51	CLOCK OUT	A/D converter clock output. Output is present only during A/D conversion. N + 1TTL pulses are output at a 520kHz rate where N is the resolution.
Pin 52	SERIAL OUT	Serial output data in NRZ format is synchronous with CLOCK OUT (pin 51) signal. Use negative edge of CLOCK OUT to strobe each bit.
Pins 53, 54, 56	$\overline{\text{ENABLE 3}}$/ $\overline{\text{ENABLE 1}}$/ $\overline{\text{ENABLE 2}}$	3-state enable lines for data bus D11 - D0 (MSB = D11). $\overline{\text{ENABLE 1}}$ (pin 54) enables D11 - D8; $\overline{\text{ENABLE 2}}$ (pin 56) enables D7 - D4; $\overline{\text{ENABLE 3}}$ (pin 53) enables D3 - D0. A low on the enable line enables data outputs.
Pin 55	+2.5V REF OUT	Positive voltage reference output. Connect to REF IN (pin 57) (through 50Ω) for unipolar or bipolar operation (unless an external reference is used). Also connect to BPO (pin 59) (through 25Ω) for bipolar operation.
Pin 57	+2.5V REF IN	Reference voltage input. Connect to +2.5V REF OUT (pin 55) (through 50Ω resistor or 100Ω pot) or use external +2.5V reference. (+2.5V ±10mV at 0.5mA required).
Pin 58	20V RANGE	A/D converter input resistor. Using SDM857: connect to S/H OUT (pin 62) for ±5V operation. Leave open for other input ranges. Using SDM856: leave open unless an external IA with a gain greater than 2 is used. (Input multiplexers are limited to ±6V maximum input voltage.)
Pin 59	BPO	A/D converter bipolar offset. Connect to REF OUT (pin 55) through a 25Ω resistor or a 50Ω pot for bipolar operation. Leave open for unipolar operation.
Pin 60	10V RANGE	A/D converter input resistor. Using SDM857 with internal instrumentation amplifier with a minimum gain of 2: connect to S/H OUT (pin 62) for 0 to +5V mux input unipolar operation or ±2.5V mux input bipolar operation. Leave open for ±5V input bipolar operation. Using SDM856 without IA: connect to S/H OUT (pin 62) for ±5V mux input operation.
Pin 61	-6.4V REF OUT	Negative voltage reference output. Maximum current drain from this point without degradation of specifications is 200μA.
Pin 62	S/H OUT	Sample/hold output. Connect to 10V RANGE (pin 60) or 20V RANGE (pin 58) for normal operations.
Pin 63	ANA COM	Analog common. Connect to DIG COM (pin 25) as close to the SDM856/857 as possible.
Pin 64	-15VDC	-15VDC at 30mA typical.
Pin 65	+15VDC	+15VDC at 30mA typical.
Pin 66	S/H CONTROL	A low signal on this line causes the sample/hold to enter the hold mode. Connect to $\overline{\text{BUSY}}$ (pin 24).
Pin 67	S/H OFFSET ADJUST	Offset adjust for sample/hold (see Figure 10).
Pin 68	S/H IN	Input to sample/hold amplifier. Connect to IA OUT (pin 69 - SDM857) or MUX OUT HI (pin 2) and MUX OUT LO (pin 78 - SDM856).
Pin 69	IA OUT	(SDM857 only). Instrumentation amplifier output. Connect to S/H IN (pin 68) for normal operation. For SDM856 make no connection.
Pins 70 thru 77	CH8-CH15 RET0 - RET7	Analog inputs 8 through 15 for single-ended operation or analog returns 0 through 7 for differential input operation.
Pin 78	MUX OUT LO	Multiplexer output for CH8-CH15 (single-ended) or RET0-RET7 (differential). Connect to MUX OUT HI (pin 2) and IA IN HI (pin 3 - SDM857) or S/H IN (pin 68 - SDM856) for single-ended input operation or connect to IA IN LO (pin 79) for differential input operation.
Pin 79	IA IN LO	(SDM857 only). Negative input of instrumentation amplifier. Connect to ANA COM (pin 63) for single-ended input operation or MUX OUT LO (pin 78) for differential input operation. For SDM856 make no connection.
Pin 80	IA GAIN ADJUST	See pin 1 description.

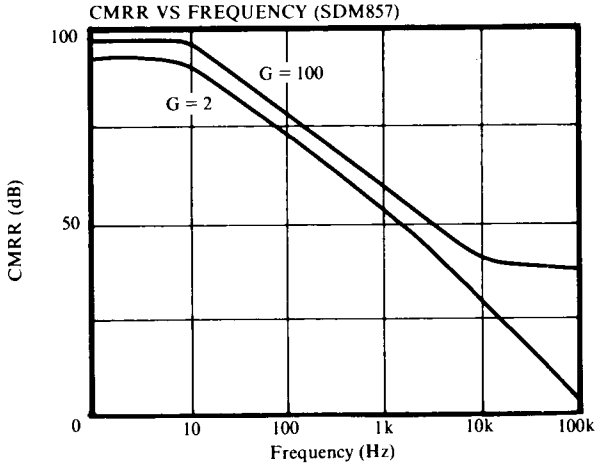


*Analog and Digital Common should be connected together close to the unit.

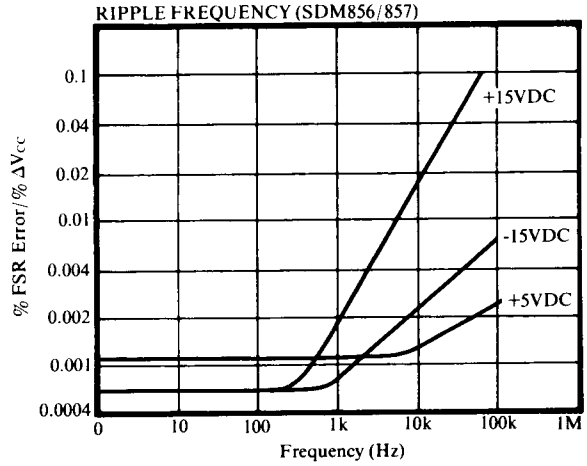
FIGURE 2. Connection Diagram for SDM857 Operating Under These Conditions:
IA Gain = 10
Analog Input: Bipolar, differential
Reference Voltage: Internal
Resolution: 12-bits
Mode: Normal
Digital Output: Binary

TYPICAL PERFORMANCE CURVES

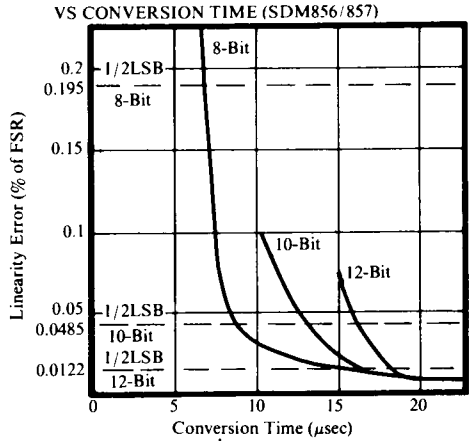
INSTRUMENTATION AMPLIFIER/MULTIPLEXER CMRR VS FREQUENCY (SDM857)



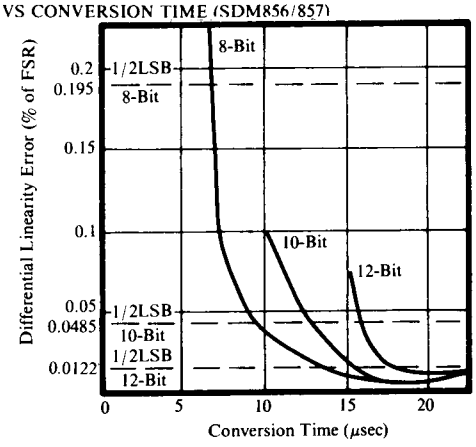
POWER SUPPLY REJECTION VS POWER SUPPLY RIPPLE FREQUENCY (SDM856/857)



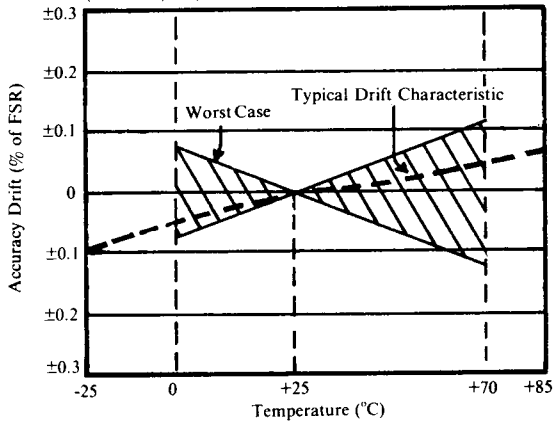
A/D CONVERTER LINEARITY ERROR VS CONVERSION TIME (SDM856/857)



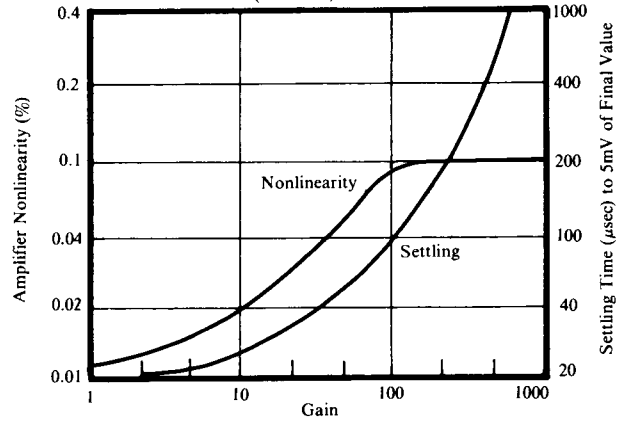
A/D CONVERTER DIFFERENTIAL LINEARITY ERROR VS CONVERSION TIME (SDM856/857)



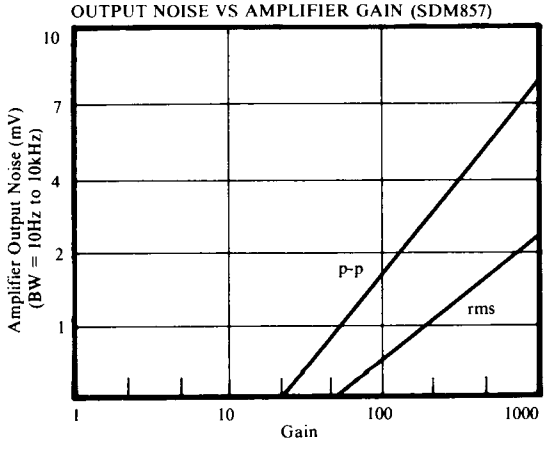
ACCURACY DRIFT VS TEMPERATURE (SDM856/857)



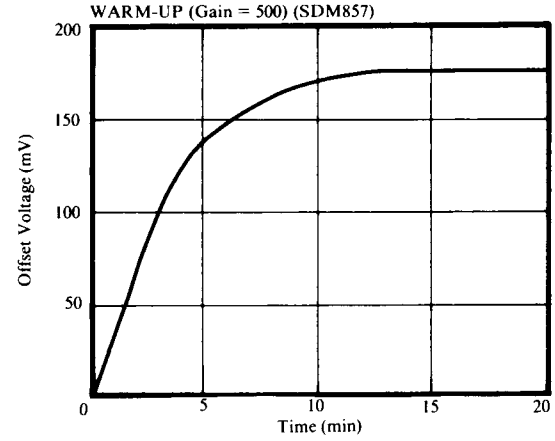
NONLINEARITY AND SETTLING TIME VS AMPLIFIER GAIN (SDM857)



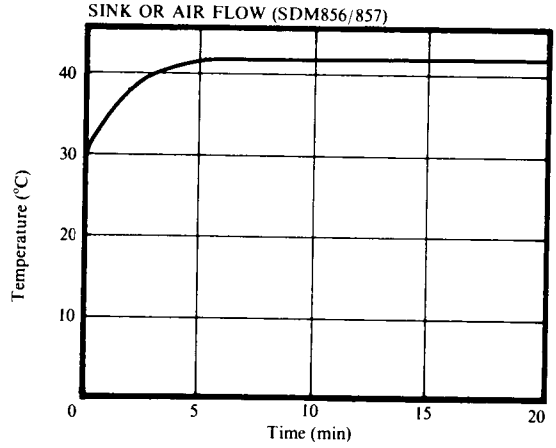
OUTPUT NOISE VS AMPLIFIER GAIN (SDM857)



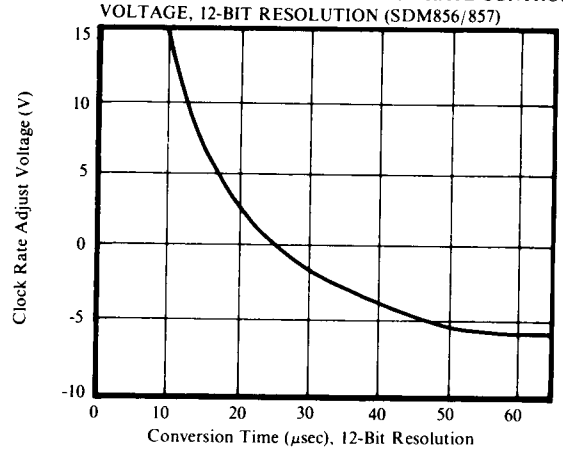
INSTRUMENTATION AMPLIFIER OFFSET WARM-UP (Gain = 500) (SDM857)



CASE TEMPERATURE VS TIME WITH NO HEAT SINK OR AIR FLOW (SDM856/857)



A/D CONVERSION TIME VS CLOCK RATE CONTROL VOLTAGE, 12-BIT RESOLUTION (SDM856/857)



SETUP PROCEDURE

INPUT CONNECTIONS

Unused analog inputs must be connected to ANA COM, pin 63. When long leads are connected to the inputs, care must be taken that leads do not pick up excessive noise from external equipment and wiring. When low level applications are undertaken, it is usually advisable to operate the system as an 8-channel, differential input system (the SDM856 requires an external differential amplifier to operate in this mode). In this way any noise will be common to both input wires, and will be rejected by the instrumentation amplifier. For best noise rejection use twisted shielded pair cable. The inputs of the SDM856/857 are protected from damage by voltage as high as 15.5 volts and from short spikes well in excess of this for a few microseconds; however, careful wiring and cable routing practices are recommended

Single-Ended Inputs

Two configurations may be used with 16 single-ended channels. They are single-ended with local ground or remote signal ground.

Local Ground:	Connect pins 2 and 78 to 3 (SDM857) or 68 (SDM856), 79 to 63, unused inputs to 63, and all signal returns to 63.
Remote Ground:	Same as local ground except connect 79 to remote signal ground. (SDM857 only).

Differential Inputs (SDM857)

Connect the signal inputs to pins 4 through 11, and their returns to 77 through 70. Connect pin 12 to 13, 2 to 3, 78 to 79, and 69 to 68.

Differential Inputs (SDM856 With External Instrumentation Amplifier)

Connect the signal inputs to pins 4 through 11, and their returns to 77 through 70. Connect pin 12 to 13. Connect pins 2 and 78 to the noninverting and inverting input of the amplifier respectively. The output of the amplifier is connected to pin 68.

AMPLIFIER GAIN (SDM857)

The instrumentation amplifier gain may be set to any value between 2 and 500 by connecting an external gain resistor between pins 1 and 80. The gain is determined by the formula: $G = 2 + (20k\Omega/R_{EXT})$. Internal gain determining resistors have an accuracy of ±0.1% and a maximum temperature coefficient of ±10ppm/°C. In normal operation IA OUT, pin 69 is connected to S/H IN, pin 68.

SAMPLE/HOLD

Connect S/H CONTROL, pin 66, to the ADC $\overline{BUSY}$ output, pin 24.

ANALOG-TO-DIGITAL CONVERTER INPUT VOLTAGE RANGE

The analog-to-digital converter is essentially a current input device having a current input range of 0 to 2mA. The input may be considered a virtual ground summing point. To convert voltage to current, a center tapped 10kΩ resistor is internally connected to this summing point. This is illustrated in Figure 3.

The interconnections of the ADC pins and the S/H OUT, pin 62, are shown in Table I.

TABLE I. ADC Range Jumpers.

Input Range (V)	Jumper
0 to +10	59 Open, 60 to 62, 58 Open
-5 to +5	59 to 55, 60 to 62, 58 Open
-10 to +10	59 to 55, 58 to 62, 60 Open

NOTE: Input ranges in Table I apply to ADC only. The input multiplexer is limited to ±6V maximum.

OUTPUT CODE

For unipolar binary and offset binary use D11 (pin 40) for the most significant bit. Two's complement binary is obtained by using pin 44, $\overline{D11}$, as the most significant bit. One's complement code may be obtained by a different offset adjustment in the calibration procedure. Two's complement and one's complement codes are usually used only for bipolar signal ranges. For 12-bit resolution, SHORT CYCLE (pin 26) is left open or taken to +5VDC. Connect pin 26 to pin 27 (10-bit) or pin 28 (8-bit) to

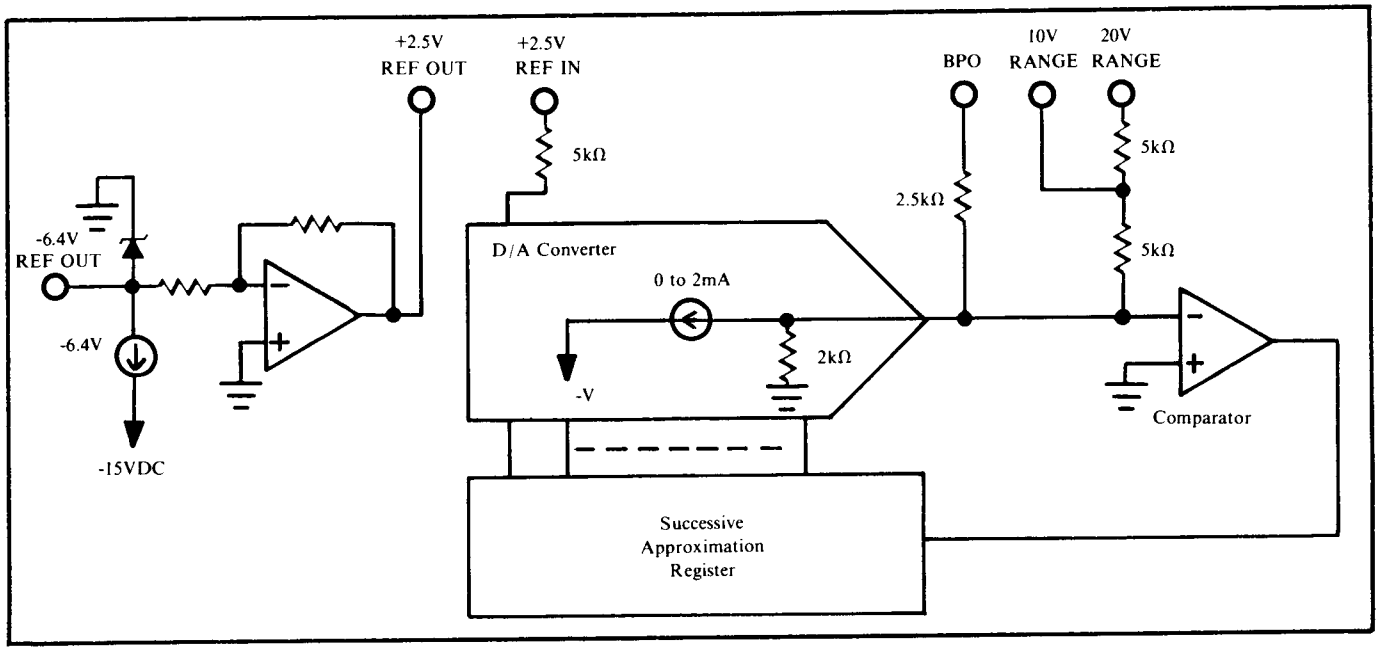


FIGURE 3. Analog-to-Digital Converter.

obtain lower resolution. The conversion time will be shortened by the following formula:

(Conversion Time) = (25μsec) x [1 - (12-R/13)]
Where R is the resolution desired.

NORMAL AND OVERLAP MODE

The two basic modes of system operation are normal and overlap. In normal operation the channel address, N, is loaded or clocked into the address latch. The addressed channel will remain selected during its analog-to-digital conversion. In overlap mode channel N + 1 is selected while channel N is being converted. This can be used to increase the system throughput rate by allowing the multiplexer and instrumentation amplifier to settle while a conversion is being made. In this way the throughput rate is limited by the sample/hold acquisition time and the analog-to-digital converter conversion time. This will be true except for low level operation where the instrumentation amplifier's settling time has been increased to a value greater than that required for the sample/hold and converter. For this reason, the overlap mode is more desirable for low level signals. Table II and Figures 4 and 5 provide additional timing details. At high signal levels a high source resistance may increase the multiplexer settling time to an extent which also makes the overlap mode desirable.

Normal Mode Connections

Connect DELAY OUT, pin 45 to $\overline{\text{TRIG}}$, pin 46.

Overlap Mode Connections

Connect $\overline{\text{BUSY}}$, pin 24 to $\overline{\text{STROBE}}$, pin 48, and to S/H CONTROL, pin 66. Connect DELAY OUT, pin 45 to

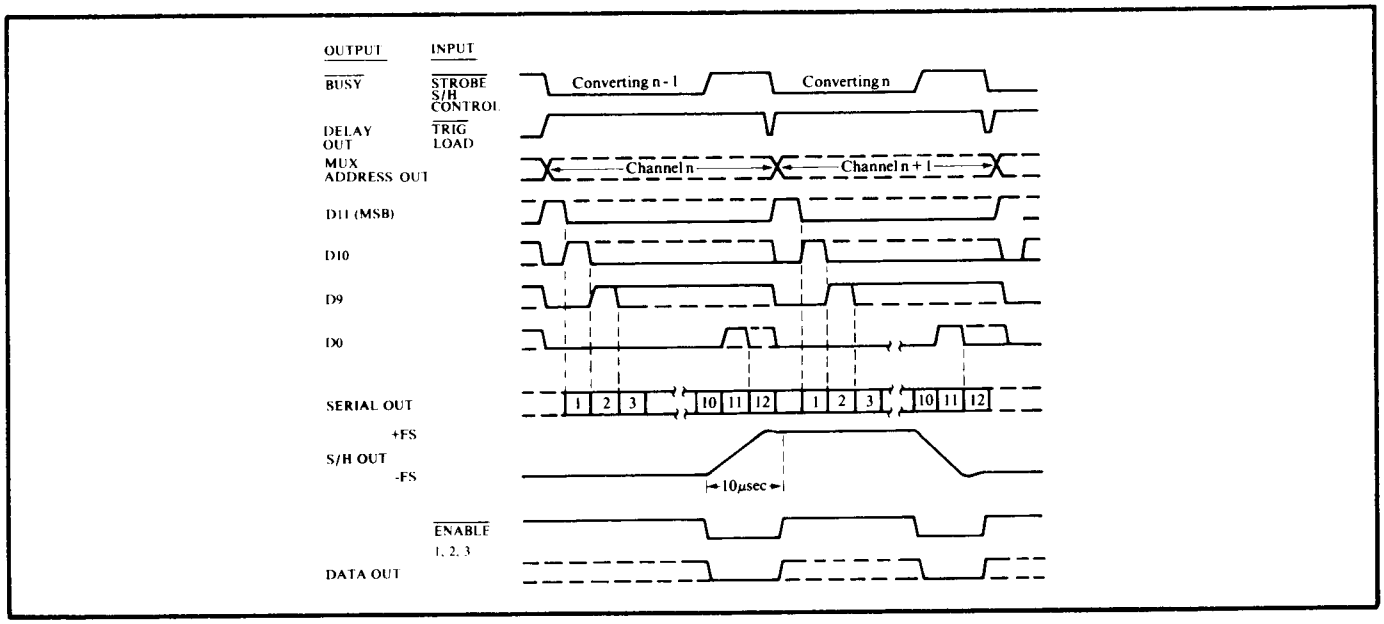


FIGURE 4. System Timing for Overlap Operation.

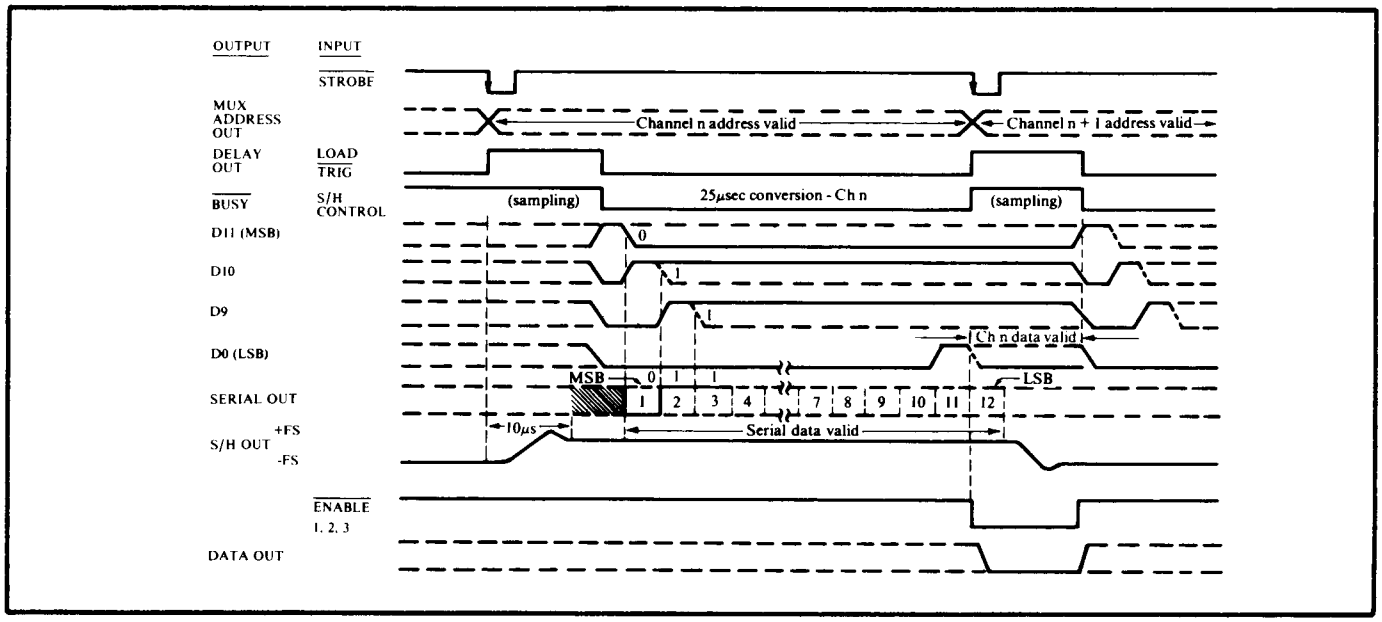


FIGURE 5. System Timing for Normal Operation.

$\overline{\text{TRIG}}$, pin 46 and to LOAD, pin 23. Adjust the delay as shown in Table II and described in the following paragraph.

DELAY ADJUSTMENT

The delay timer may be adjusted with an external capacitor or resistor from DELAY ADJUST (pin 47) to +5VDC. A capacitor will increase the delay to allow for the increased settling time of the instrumentation amplifier at high gains while a resistor will decrease the delay to allow for increased throughput rate with an external high speed instrumentation amplifier or lower resolution operation.

The values of R and C versus delay for both the SDM856 and SDM857 are shown in Figures 6, 7, 8 and 9.

TABLE II. Throughput Rate and Delay Time vs Gain for Normal and Overlap Modes.

System Gain		System Accuracy		Throughput Rate (min) (Channels/sec)				Delay Time (μsec)		
				Normal		Overlap		Normal	Overlap	
V/V		KG	JG	JG	KG	JG	KG	JG and KG	JG	KG
1	856 only	±0.024%	±0.048%	33k	25k	38k	27k	15	26	35
2	857 only	±0.024%	±0.048%	22k	18k	38k	27k	30	26	35
10	857 only	±0.035%	±0.06%	22k	18k	38k	27k	30	26	35
100	857 only	±0.08%	±0.11%	10k	9k	11k	11k	90	90	
500	857 only	±0.1%	±0.15%	2.5k	2.4k	2.6k	2.6k	390	390	

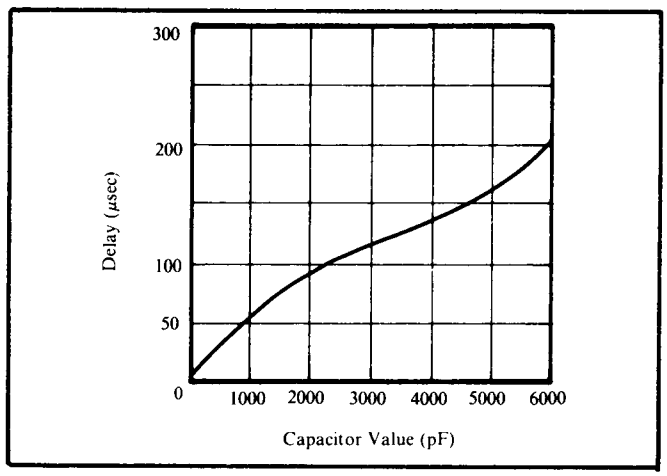


FIGURE 6. Typical Capacitor Value to Increase Delay Time (SDM857).*

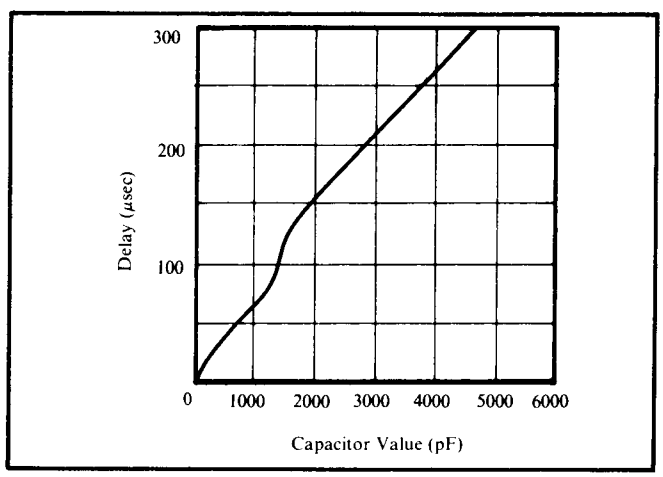


FIGURE 7. Typical Capacitor Value to Increase Delay Time (SDM856). *

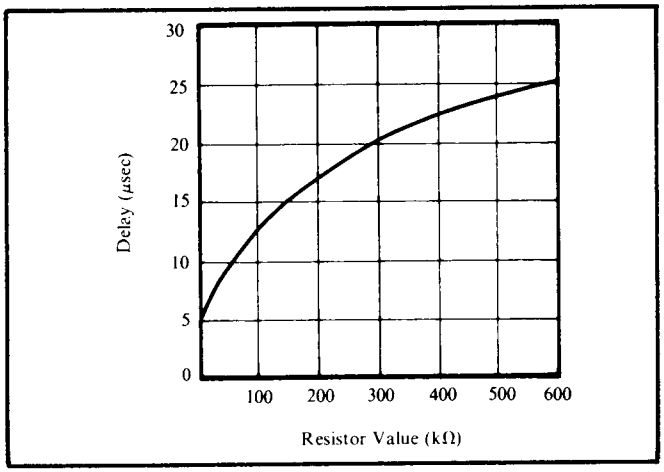


FIGURE 8. Typical Resistor Value to Decrease Delay Time (SDM857). *

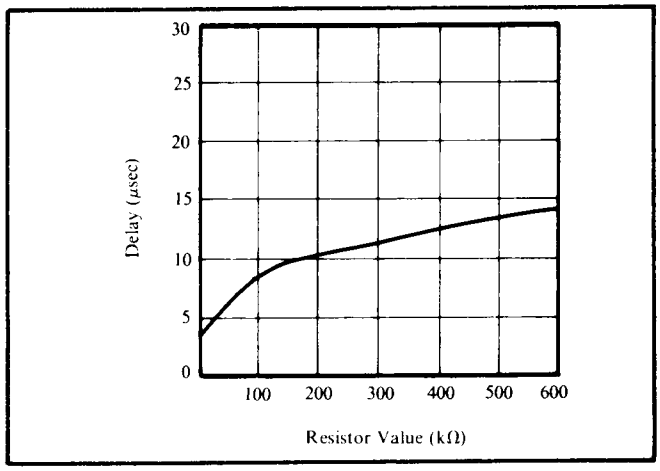


FIGURE 9. Typical Resistor Value to Decrease Delay Time (SDM856). *

*Capacitor or resistor is connected from pin 47 to +5V supply.

CONVERTER INITIALIZATION

On power-up, the state of the ADC internal circuitry is indeterminate. One conversion cycle is required to initialize the converter after power is applied.

GROUNDING CONSIDERATIONS

The circuit configuration of a high speed successive approximation A/D converter is such that low level analog and digital signals are in close proximity. In fact the two circuits are actually interconnected; for this reason no AC noise voltage should be allowed to exist between digital and analog ground. Digital and analog ground should be connected as close to the unit as possible. In a typical application an SDM module will be used near a computer. For best results the SDM digital ground should be connected to the computer's +5VDC supply ground at the supply terminal. The ±15VDC supply ground should be connected to the +5VDC supply ground of the SDM only. The Model 546 +5VDC to ±15VDC DC/DC converter is a convenient way to do this. For single-ended systems, signal returns are connected to analog ground; or if a common remote signal ground is available, the inverting input of the differential amplifier (SDM857) should be used for the signal return.

CALIBRATION PROCEDURE

GAIN AND OFFSET ADJUSTMENT

External gain and offset adjust potentiometers are shown in Figure 10. Cermet pots with a T.C.R. of ±100ppm/°C or less should be used. The adjustments shown each have a range of ±0.3% of the Full Scale Range.

If adjustment of gain and offset is not required R1 and R2 should be replaced with 25Ω and 50Ω resistors respectively. These resistors should be low T.C. (<±100ppm/°C) metal film or equivalent.

The S/H OFFSET ADJUST (pin 67) may be used as a fine offset adjustment.

The easiest way to calibrate the device is to connect a voltage source to multiplexer input CH0 (either differential or single-ended input operation may be used).

Channel zero will be addressed by simply connecting $\overline{\text{CLEAR}}$ to DIG COM.

After the CH0 voltage source has been addressed, set it to the most negative value of the input range being used plus 1/2LSB. Twelve-bit LSB voltage values are given in Table III. Connect a triggering source to $\overline{\text{STROBE}}$ and adjust the offset potentiometer until all output bits are logic zero with bit DØ dithering between logic zero and one. Change the source voltage to the most positive value of the input range minus 3/2LSB. Adjust the gain potentiometer until all output bits are logic one with bit

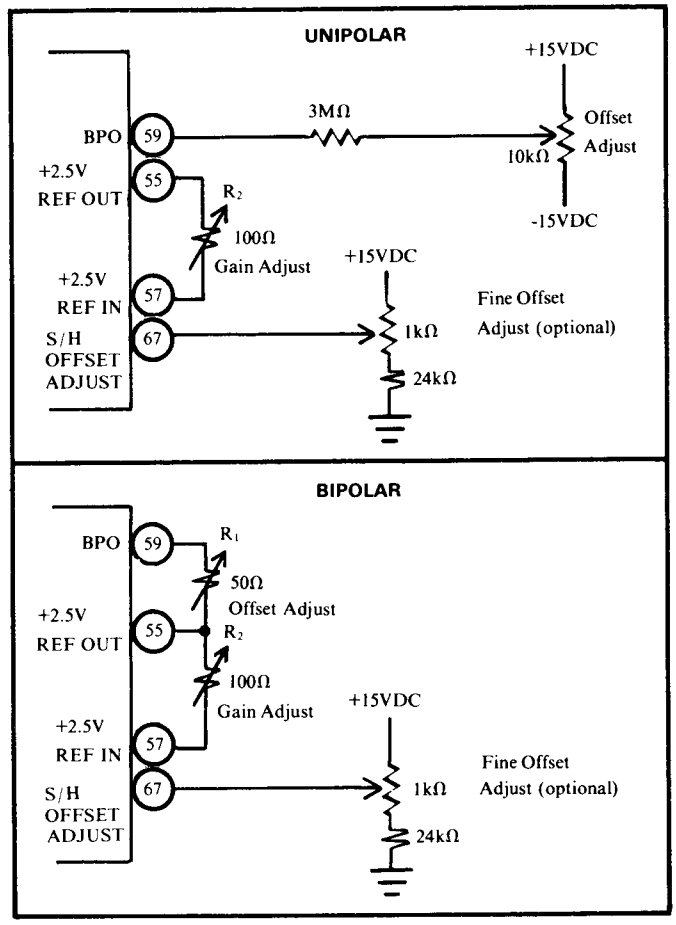


FIGURE 10. External Gain and Offset Adjustment.

D0 dithering between logic one and zero. When a resolution less than 12 bits is used, the LSB voltage is given by the formula in Table III where N is the number of output bits. One's complement coding is obtained by shifting the previous adjustments up by 1/2LSB using the offset potentiometer.

TABLE III. LSB Values for 12-Bit Resolution.

LSB (Volts) = (Range)/(2^N)

Range	LSB Voltage (12-Bits)
5V	1.22mV
10V	2.44mV

CLOCK RATE ADJUSTMENT

To obtain higher throughput rates at lower accuracy the A/D clock rate can be adjusted by varying the voltage on the clock rate adjust pin. This point should be connected to digital common for 12-bit accuracy, +5VDC for 10-bit accuracy, or +15VDC for 8-bit accuracy giving conversion times of 25μsec, 15μsec and 10μsec respectively. The conversion speed can also be continuously varied from about 13μsec to 110μsec (12-bit resolution) with a potentiometer as shown in Figure 11.

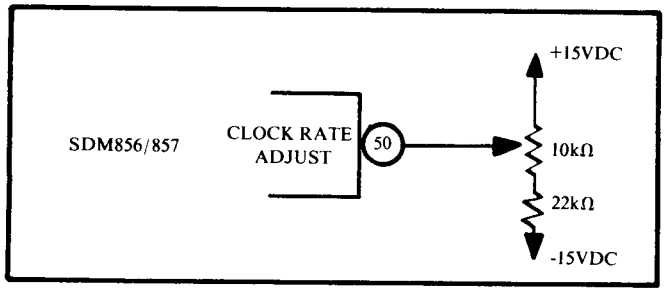


FIGURE 11. Clock Rate Adjustment.

CHECKOUT PROCEDURE

Checkout is essentially accomplished by the calibration procedure. Before the unit is plugged into a new installation, it is well to go over the pin connection list to be sure that all 80 pins have been properly connected in the setup. Linearity and monotonicity may be verified by varying the input voltage over the complete range during the calibration procedure.

LATCH

Latch operation can be verified by connecting a pulse generator to the LOAD input. The address inputs (A0 IN - A3 IN) should appear at the address outputs (A0 OUT - A3 OUT).

AMPLIFIER AND MULTIPLEXER

To check amplifier operation, connect a voltmeter to IA OUT (pin 69) and observe that the output follows the input voltage as in the calibration procedure. Check the multiplexer in the same way noting that the output changes when the address is changed.

SAMPLE/HOLD

The sample/hold circuit can be checked during the calibration procedure by observing the output of the S/H OUT (pin 62) with an oscilloscope. The waveform should be approximately as in Figure 12.

The charge offset will vary in a linear manner from about 10mV for -10V to 30mV for +10V. This is compensated for by the offset and gain adjustments of the A/D converter. The spikes during conversion are normal noise caused by the converter operation.

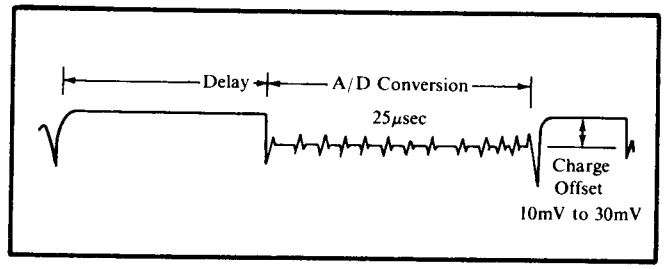


FIGURE 12. Sample/Hold Output Waveform.

ANALOG-TO-DIGITAL CONVERTER

The ADC can be checked out as an individual circuit element. Connect a fixed voltage to either 20V RANGE (pin 58) or 10V RANGE (pin 60). After adjusting the gain and offset errors as described on page 13, the digital output should represent the analog input as shown in Table IV. To enable the three-state buffers, pins 53, 54 and 56 should be connected to logic 0.

In overlap, when the amplifier/multiplexer settling time is less than the ADC conversion time, set the delay timer for the ADC conversion time plus the sample/hold acquisition time (30μsec plus 10μsec). When the amplifier/multiplexer settling time exceeds the ADC conversion time plus the S/H acquisition time, set the delay timer for the amplifier/multiplexer settling time.

TABLE IV. Delay Timer Settings for Specified Settling Time Accuracies of the Instrumentation Amplifier.

Full Scale Input Range	ADC Range	Amplifier Gain	Resolution	Amplifier/Multiplexer Settling Time (μsec)		
				To ±0.2%	To ±0.05%	To ±0.01%
10V	-10 to +10	2	2.44mV	8	10	20
1V	0 to +10	10	244μV	12	14	24
0.1V	0 to +10	100	24.4μV	65	80	90
20mV	0 to +10	500	4.88μV	320	390	450

APPLICATION NOTES

CHANNEL CAPACITY EXPANSION

The SDM856/857 may be easily expanded to any number of channels by using Burr-Brown Models

MPC8D and MPC16S. The MPC8D is an 8-channel double-ended multiplexer, and the MPC16S is a 16-channel single-ended multiplexer. These devices are CMOS FET units which can operate from supply voltages up to ±20VDC. They feature latch-free operation with full input protection. Binary decoding and level shifting circuits are included. Logic levels are jumper selectable for TTL or CMOS. Packaging is a 28-pin DIP.

There are two methods for using these devices for channel capacity expansion. The SDM856/857 multiplexer may be expanded by shunt or series connected multiplexers. Shunt connection refers to connecting the output of several multiplexers together and enabling each in sequence. The disabled devices present a very high resistance to the common output line. The disadvantages to this scheme are increased leakage current and output capacitance. For these reasons shunt connections are usually used only when it is desired to expand the capacity by a factor of two or three. A shunt connected system logic diagram is shown in Figure 13. Forty-eight single-ended channels are indicated; however 24 double-ended channels could easily be realized by using two MPC8D's and connecting the two-sided outputs appropriately. For large systems series connected expansion is usually used. In this method the outputs of a second tier of multiplexers are connected to the inputs of the SDM856/857 multiplexer. This allows up to 256 single-ended or 128 double-ended channels to be addressed. A third tier can be used for 4096 single or 2048 double-ended channels. A logic diagram of a series system is shown in Figure 14. Double-ended operation can be obtained by using the MPC8D instead of the MPC16S and connecting the SDM856/857 for double-ended operation.

SEQUENTIAL ADDRESSING

Simply adding an external counter will allow sequential addressing of all 16 input channels (see Figure 15).

MULTIPLEXER CIRCUIT OPERATION

At the address and enable inputs a voltage is interpreted as a logic "1" if it is greater than 2.4 volts; and "0" if less than 0.8 volts.

When an input channel has been selected the "on resistance" from input to output is approximately 1.8kΩ. The input capacitance for each channel is approximately 7pF; while the output capacitance is approximately 25pF for each 8-channel multiplexer. A circuit model of an ON channel is shown in Figure 16.

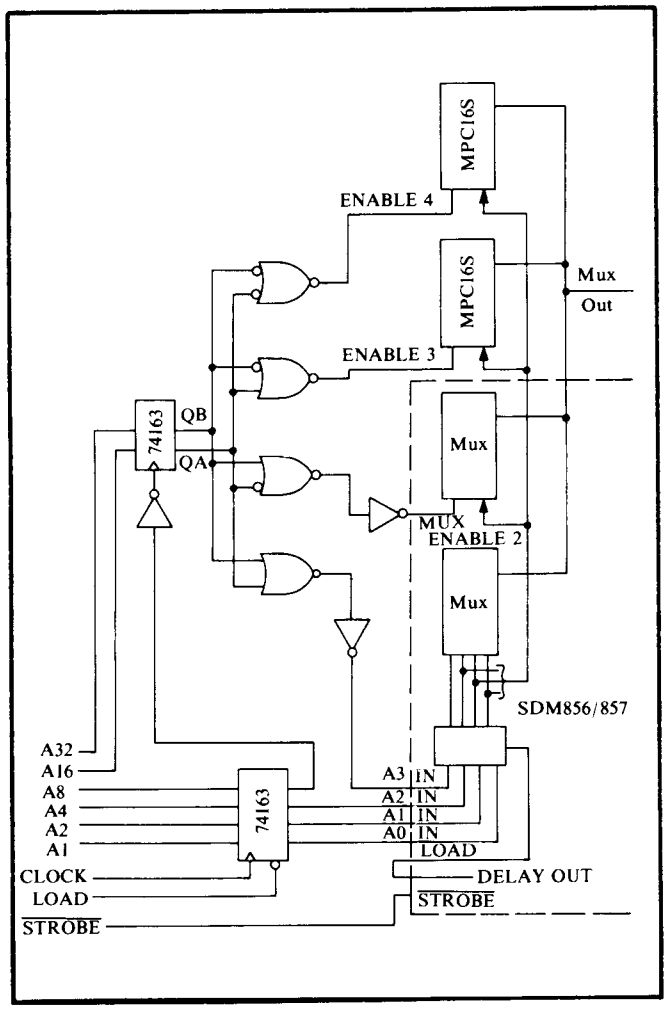


FIGURE 13. Shunt Connected Multiplexer System 32 Single-Ended Channels.

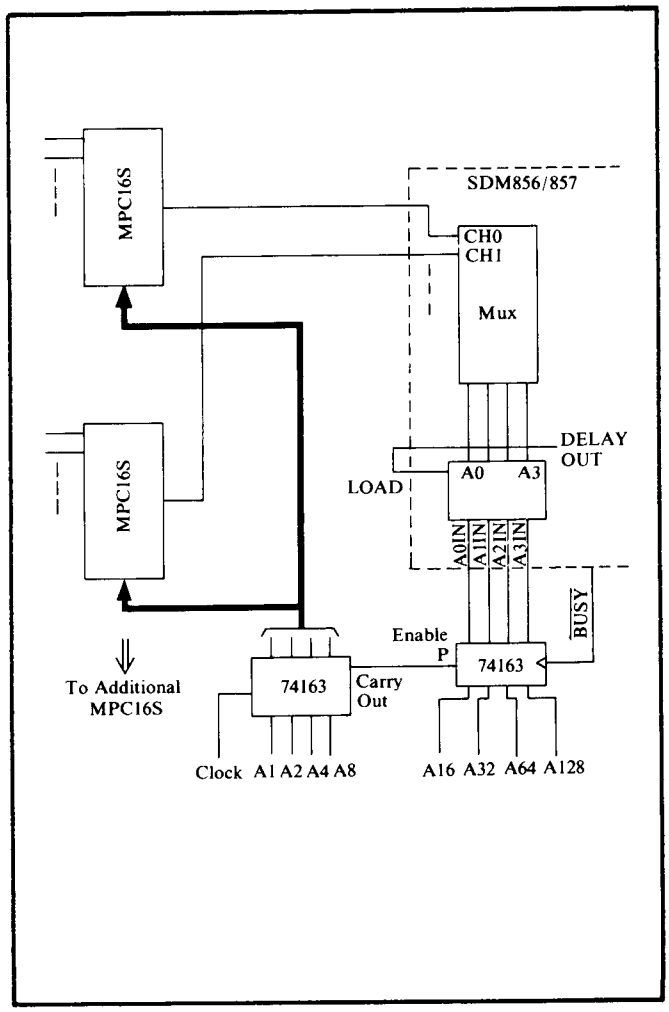


FIGURE 14. Series Connected Multiplexers, 256 Single-Ended Channels. Sequential Addressing.

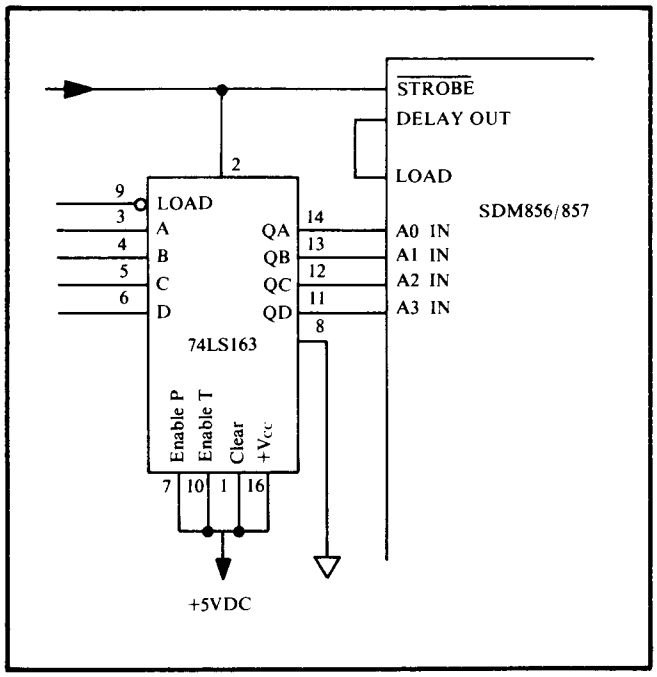


FIGURE 15. Sequential Addressing.

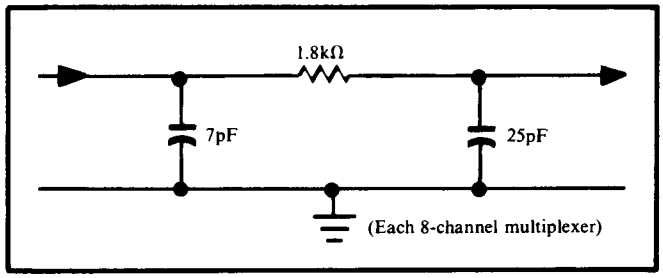


FIGURE 16. ON Channel Circuit Model.

This model is very important when high speed switching of high output impedance sources is required. For example, if the full accuracy and resolution of the system is required, the signal at the output of the multiplexer must be allowed to settle to about 0.01%. If the source impedance is 1kΩ, the 7pF can be neglected and the multiplexer has a time constant of 2.8kΩ x 50pF = 140nsec. It requires approximately 9 time constants to settle to 0.01%; 1.26μsec is well within the 30μsec (SDM857) or 15μsec (SDM856) of the delay timer. However, if the source impedance had been 10kΩ, the 0.01% settling time would have approached 6μsec. For high speed multiplexing of higher impedance sources, it will usually be desirable to parallel the 7pF input capacitor with a large capacitor; however, this could limit the source bandwidth. In any case there is no point in making it any larger than 10^4 times the output capacitance, or 0.5μF. When this size storage capacitor is used, the output time contant is 1.8kΩ x 50pF = 90nsec. This means that the system settling time is essentially determined by the settling time of the differential amplifier and sample/hold circuit. For switching of large signals it must be remembered that the ON resistance is the channel resistance of a FET, and, as such, it is a nonlinear function of the applied voltages. Any FET will current limit at its I_{DSS} value. As a result, the previous calculations are only an approximation derived from a linearized model. The settling time to 0.01% for a 20V step is approximately 4.0μsec for source impedance less than 1kΩ.

The analog and digital inputs have reverse biased diode circuits which prevent damage from discharge of static electricity. However, it is still wise to take reasonable precaution against static discharge.

BINARY SCALING

Binary scaling of the A/D converter provides LSB voltages of 2.5mV, 2.5mV, and 5.0mV for voltage ranges of 0 to 10.24V, -5.12V to +5.12V, and -10.24V to +10.24 respectively. These may be obtained by adding external resistors in series with input resistors of the A/D converter. Metal film resistors with temperature coefficients of less than 100ppm/°C are recommended. This is shown in Figure 17.

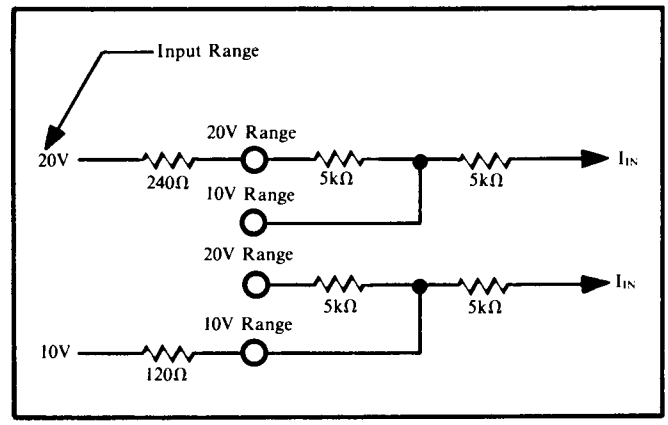


FIGURE 17. Binary Scaling.

THERMOCOUPLE TEMPERATURE ACQUISITION

Thermocouples are often used as temperature sensors for process control systems. Thermocouples are characterized by temperature coefficients of 10 to 70μV/°C and operating ranges of minus hundreds to plus thousands of degrees centigrade. When the SDM857 is operated with a instrumentation amplifier gain of 100 to 500, it may be connected directly to these devices. However, electronic instrumentation is usually mounted in a temperature controlled environment with long runs of thermocouple wire to the actual point of temperature measurement. These long wire runs often pick up large common-mode noise signals of 60Hz or higher frequencies. When the SDM857 is used as an 8-channel differential input system, the high common-mode rejection of the instrument amplifier will reject common-mode noise. To minimize differential mode noise, signal wires should be twisted and possibly shielded. As a rule, an open twisted pair is better than a coax, and a shielded, twisted pair better still. In applications where these wiring practices cannot always be observed, a differential RC filter may be used (see Figure 19).

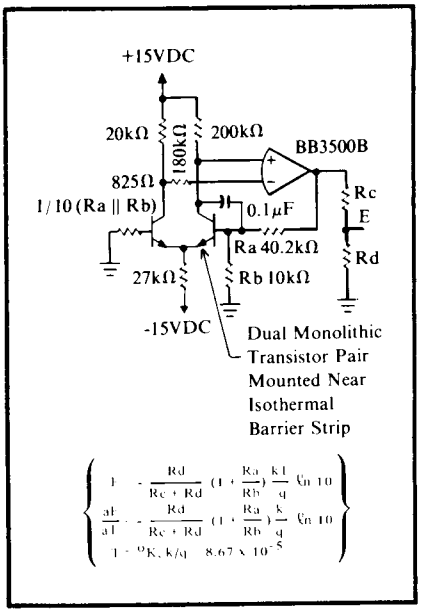


FIGURE 18. Ambient Temperature Sensor.

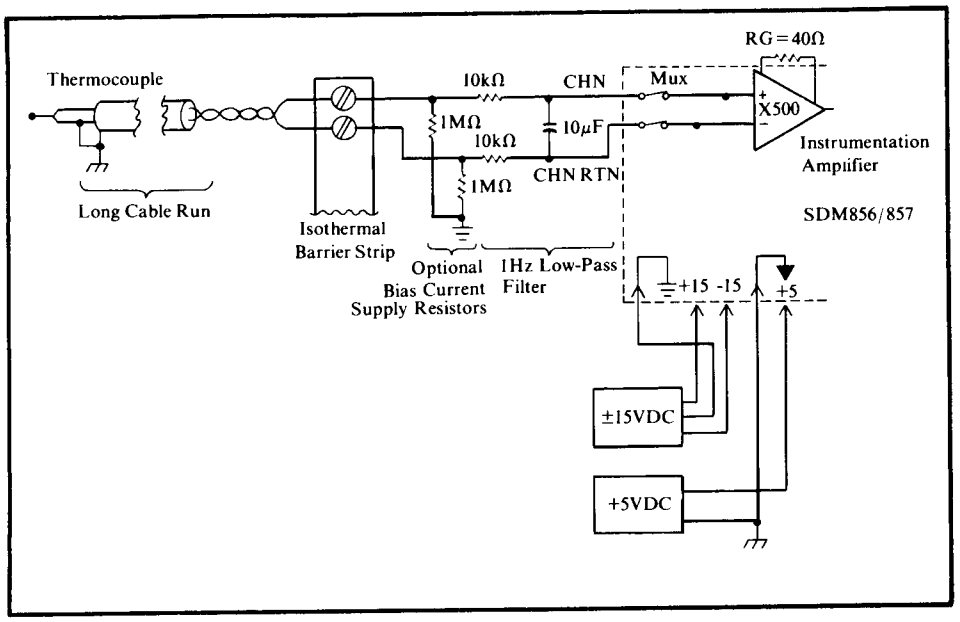


FIGURE 19. Thermocouple Inputs.

The 10kΩ resistors and a 10μF capacitor provide low-pass filtering ($f_c = 0.8$Hz) while the 1MΩ resistors supply bias current to the instrumentation amplifier. The remote sensor should be earth grounded to prevent common-mode voltages from exceeding the ±10V range of the multiplexer. This will usually supply bias current; however, the resistors provide a back up. It is not obvious what resistance the bias currents of the amplifiers will see. The 1MΩ resistors do not enter into an error calculation for input drift because the low resistance of the sensor shorts any differential voltage that might be caused by the offset or difference current of the amplifier. Offset or difference current is merely the difference between the bias currents of each input. See page 17 for a worst case error analysis of the input filter for multiplexed data acquisition systems. The 1MΩ resistors could have been put on the output side of the multiplexer eliminating the need for repeating them for each input; however, this would have loaded the 10kΩ resistors of the filter causing a possible 1% error for static conditions.

To complete a thermocouple system it is necessary to terminate all thermocouple wire pairs at an isothermal box or connector strip of some type. An ordinary barrier strip in an enclosed cabinet with even air circulation is usually adequate. The temperature of this barrier strip must be monitored to allow the observed thermocouple emf to be cold junction compensated. Figure 18 shows an excellent circuit for this purpose. Its output is connected to one of the input channels to supply ambient temperature data to the system computer.

INPUT FILTER DESIGN FOR LOW LEVEL SYSTEMS

When the SDM856/857 is used to acquire low level sensor data, it is often desired to place a low-pass, passive filter on each input. This is usually done to reduce any differential mode, power line frequency pickup. Figure 20 shows such a circuit.

This circuit is deceptive in its simplicity. Actually four errors sources should be considered in its design. They are loading, offset current, charge transfer, and pump out current.

The static loading error is simply the resistive divider created by the filter resistors and the 100MΩ input resistance. For low level sensors, 0.1% system accuracy is usually adequate. Thus R should be less than 10^{-3} x (100MΩ) = 100kΩ. However, if the inputs are scanned at a high speed, and between scans the multiplexer can be addressed to a unique channel having a lower resistance, higher filter resistances can be tolerated because the large filter capacitor will act as a voltage source during the 30μsec to 100μsec period required to read each channel. The filter capacitors will then recharge between scans.

The input offset current caused by the bias currents of the instrument amplifier as well as any leakage current of the multiplexer will cause an error voltage proportional to the size of the filter resistors ($E = I_{OS}$ x 2R). Of course, this is a static error and as for loading error, may not be important for some operating conditions. If all channels have the same resistance most of this error may be corrected by the offset adjustment of the analog-to-digital converter. If the offset current drift is 0.1nA/°C

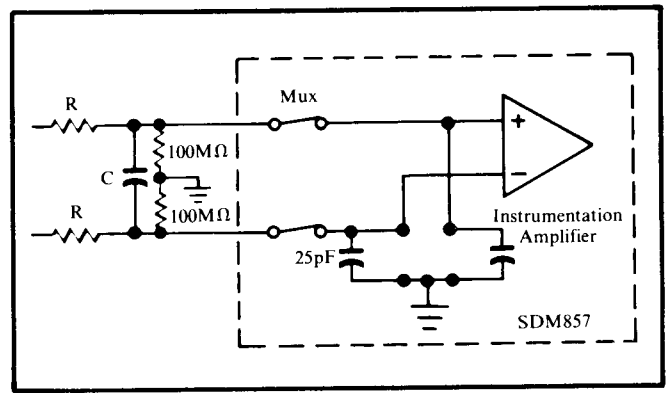


FIGURE 20. Input Filter Design for Low Level System.

the error is 2R x 0.1nV/°C. For 10kΩ resistors this would be 2μV/°C.

When the multiplexer scans, charge will be transferred from the filter capacitor to the 25pF output capacitance of the multiplexer. For less than 0.1% of full scale error, the filter capacitor must be larger than 25000pF. This assumes that adjacent channels may differ by the full scale voltage.

Pumpout current refers to charge being transferred from the filter capacitor to the multiplexer capacitance at time intervals short enough that the filter capacitor does not have time to recharge between scans. At high scan rates this may be considered a DC current which may add to the offset current. Assume a 10μF capacitor sampled once per millisecond. For a 20mV full scale range, the maximum effective current is (20mV x 25pF)/1msec = 0.5nA. If the filter resistors are 10kΩ, a 0.5nA x 20kΩ = 10μV error is created.

When no input filter is used, the signal source must be able to charge the multiplexers and any cable capacitance during the channel acquisition time of the multiplexer and amplifier. This is discussed on page 16. When all of these errors as well as the basic 2.0μV/°C input offset voltage drift of the amplifier are considered, the overall system accuracy may be estimated.

INSTRUMENTATION AMPLIFIER OVERLOAD RECOVERY

If an analog input channel is left open or is opened due to a sensor failure it is possible for the instrumentation amplifier to saturate when that channel is addressed. Since the overload recovery time of the IA is usually much longer than the settling time specification, this can cause an error on the NEXT channel that is addressed. One way to avoid this problem is to connect 100MΩ resistors from the instrumentation amplifier inputs to analog common as shown in Figure 21. This technique will generally work for high level input (gain ≤ 10). With low-level inputs the offset current of the IA will usually cause saturation to occur anyway.

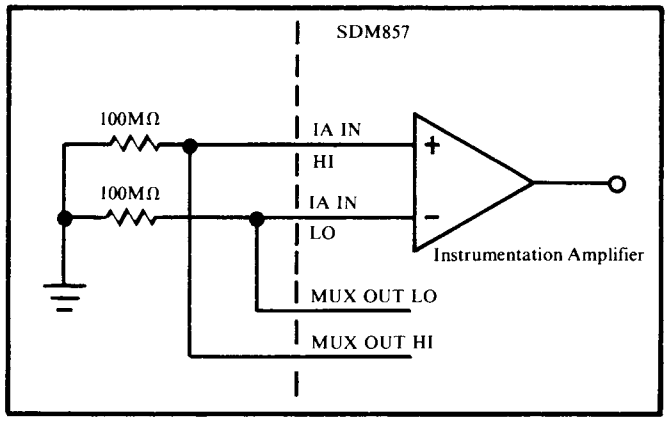


FIGURE 21. Circuit to Prevent High Level Saturation.

The SDM856 and SDM857 can be readily interfaced to operate with microprocessors. The following circuit diagrams illustrate several typical applications. The logic functions are all TTL.

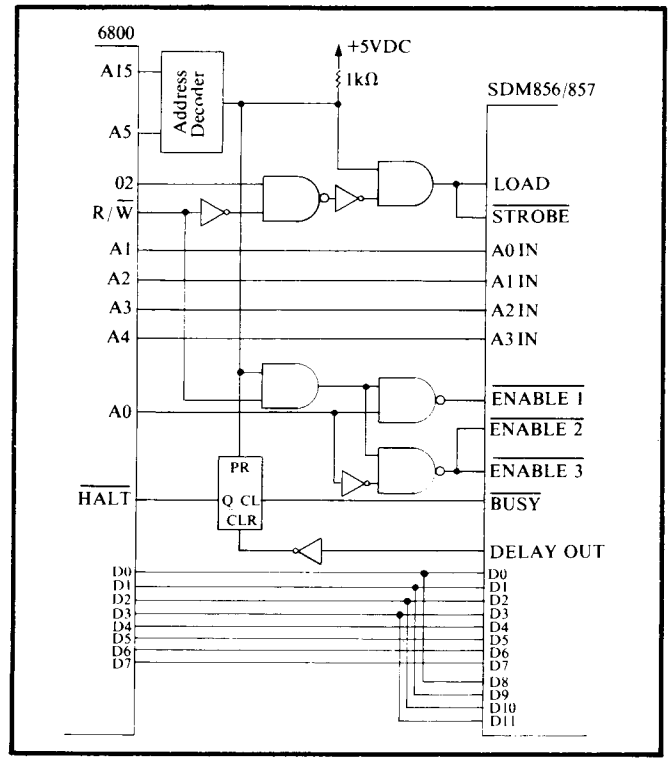


FIGURE 22. SDM856/857 Interfaced to 6800 Microprocessor.

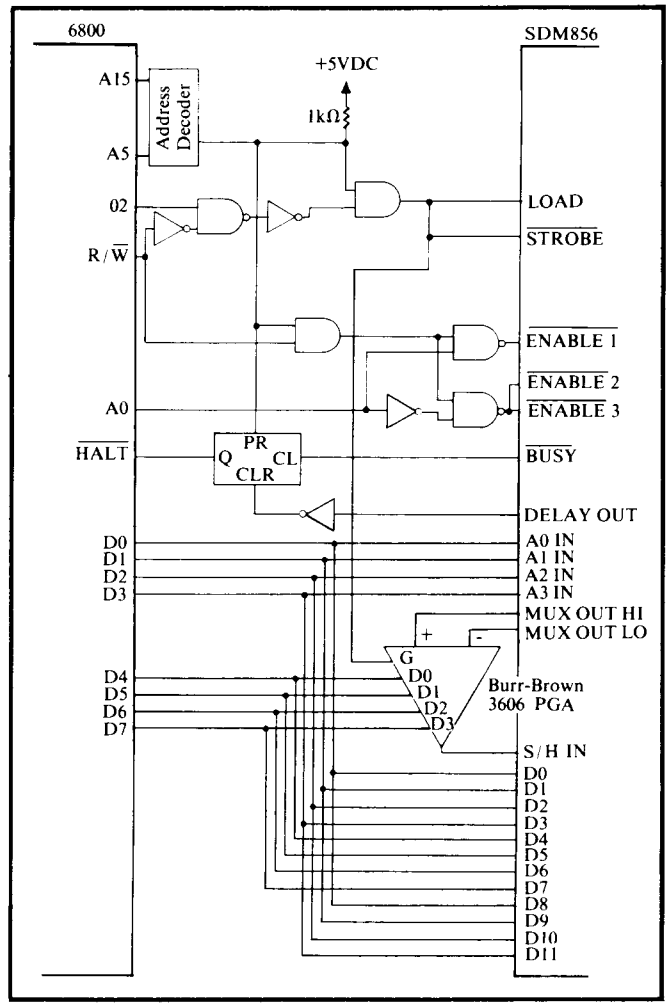


FIGURE 23. SDM856 and 3606 PGA Interfaced to 6800.

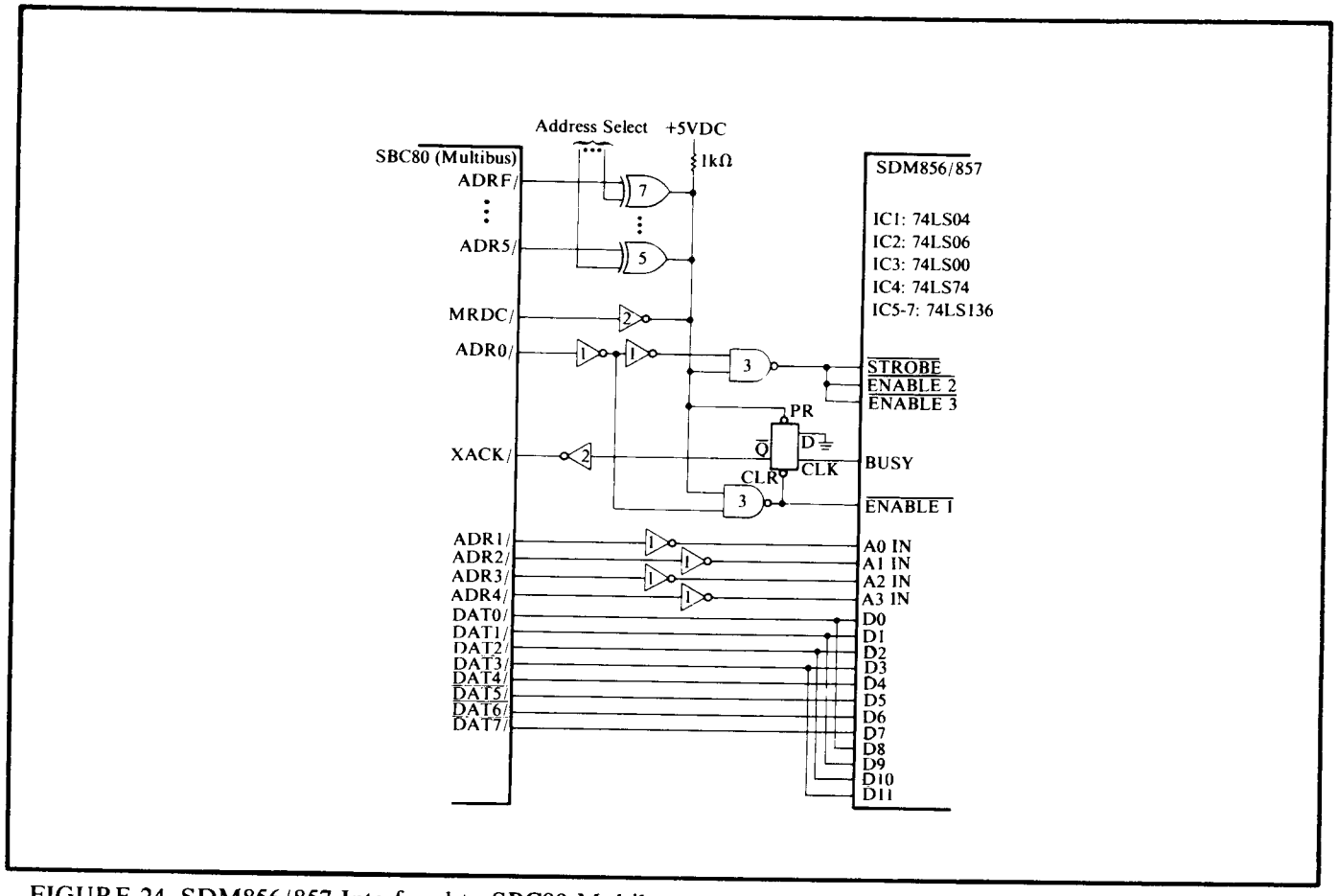


FIGURE 24. SDM856/857 Interfaced to SBC80 Multibus.

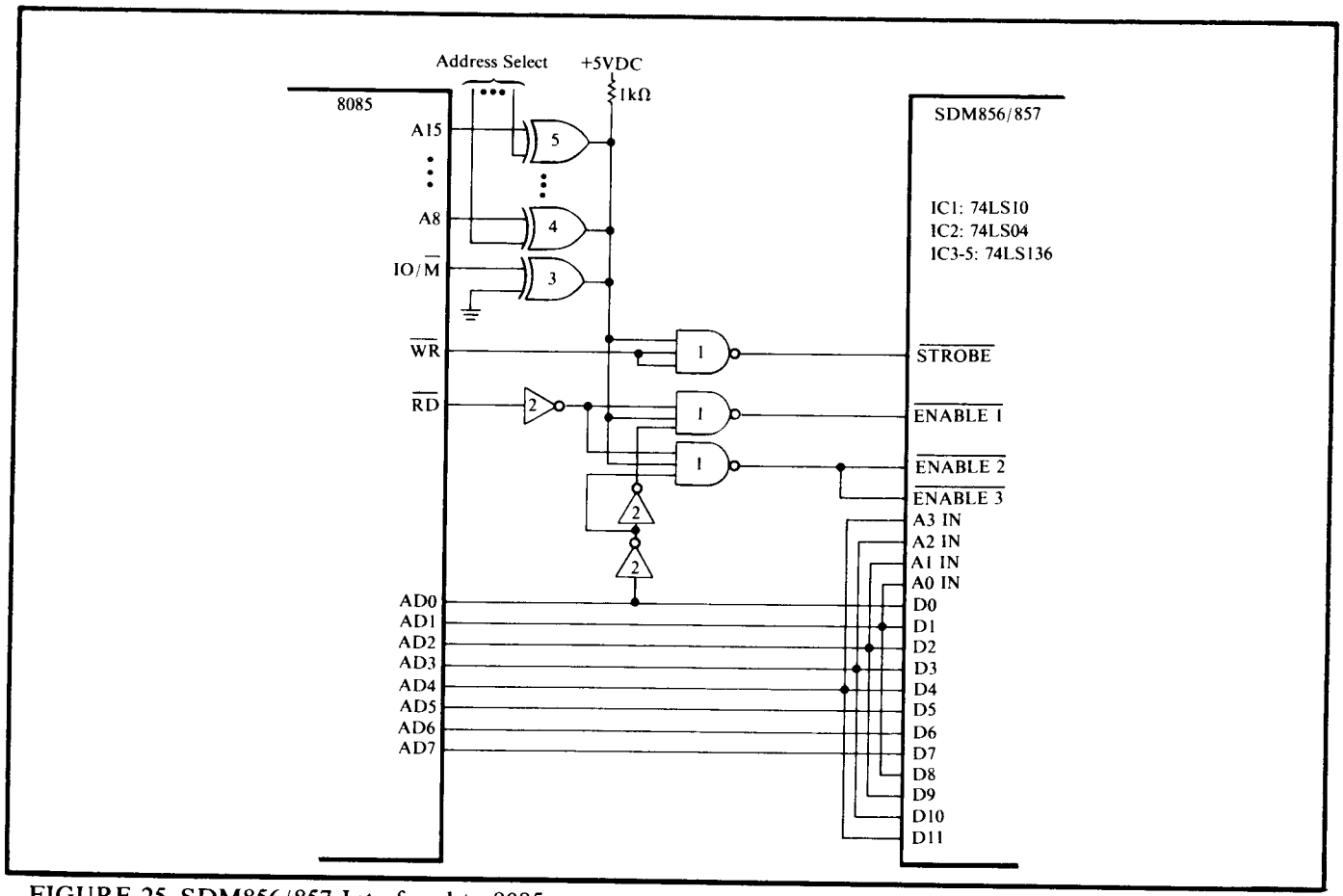


FIGURE 25. SDM856/857 Interfaced to 8085.

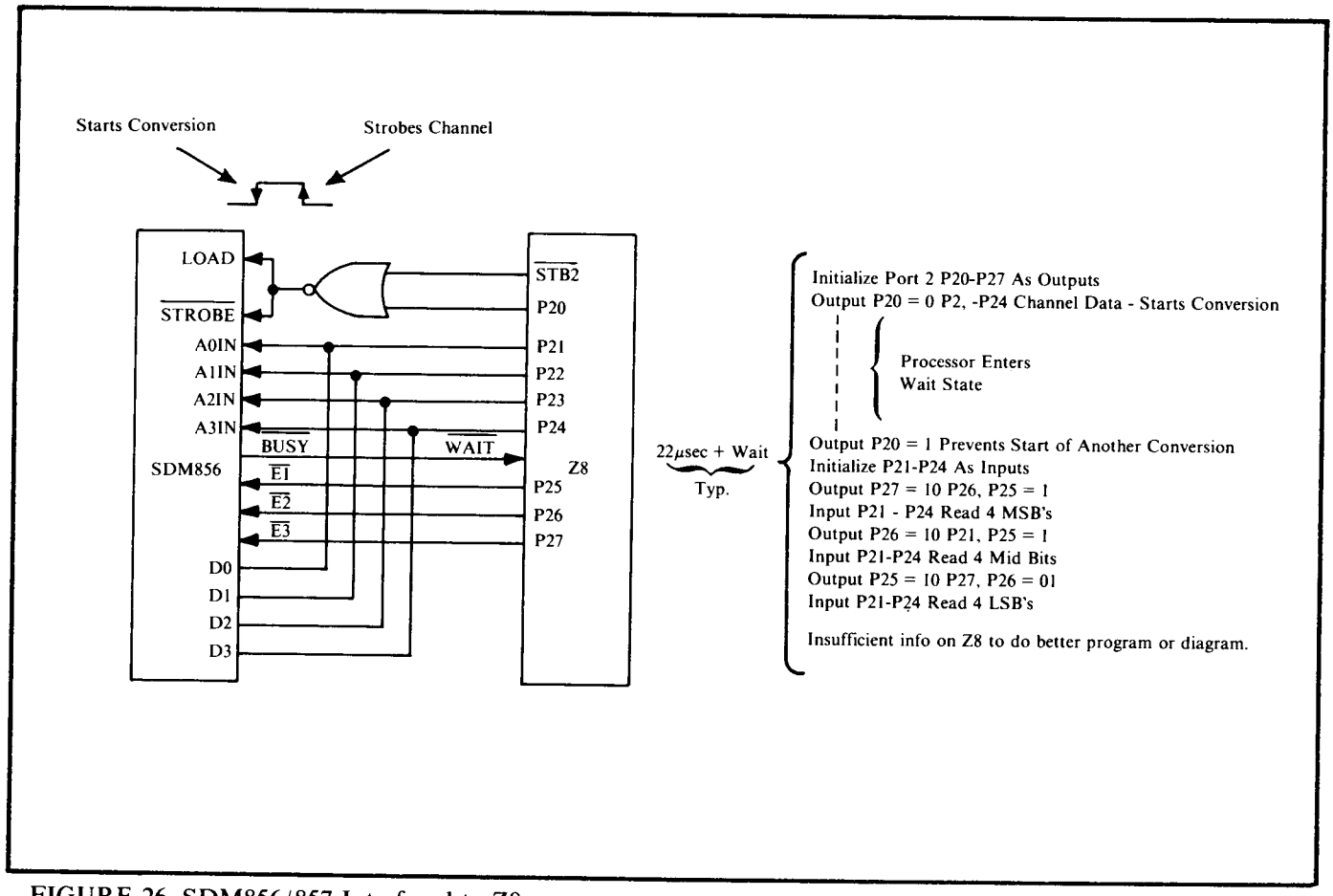


FIGURE 26. SDM856/857 Interfaced to Z8.