HN27V101A Series

Preliminary

131072-Word x 8-Bit CMOS One Time Electrically Programmable ROM

HITACHI

Rev. 0
Mar. 16, 1992

The Hitachi HN27V101A is a 131072-word x 8-bit one time electrically programmable ROM. Initially, all bits of the HN27V101A are in the "1" state (output high). Data is introduced by selectively programming "0" into the desired bit locations. This device is packaged in 32-pin plastic package, therfore, this device is cannot be rewritten and erased.

Features

- Low voltage, single power supply:
  +2.7 V to 5.5V
- High speed: Access time 200/250 ns (max)
- Low power dissipation:
  Standby mode; 5 µW (typ),
  Active mode; 50 mW/MHz (typ)
- Fast high-reliability page programming and fast high-reliability programming: (compatible with HN27C101ATT/ARR)
  Program voltage; +12.5 V DC
  Program time; 14 sec (typ)
  (Theoretical in page programming)
- Pin arrangement: 32-pin JEDEC standard
  (TTP-32D)
- Device identifier mode: Manufacturer code and device code

Ordering Information

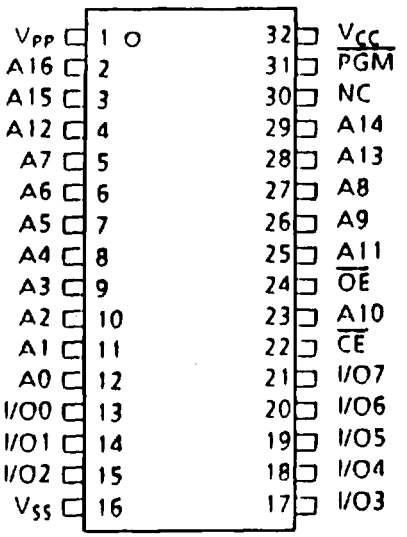
Type No.	Access time	Package
HN27V101ATT-20	200 ns	400-mil 32-pin TSOP type II (TTP-32D)
HN27V101ATT-25	250 ns	
HN27V101ARR-20	200 ns	400-mil 32-pin TSOP type II Reverse (TTP-32DR)
HN27V101ARR-25	250 ns	

Note: This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

Hitachi semiconductor

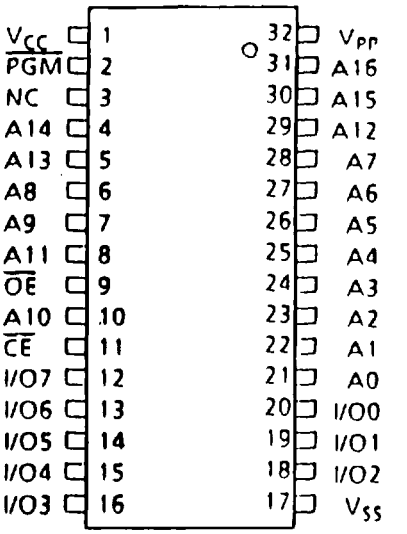
Pin Arrangement

HN27V101ATT Series



(Top View)

HN27V101ARR Series

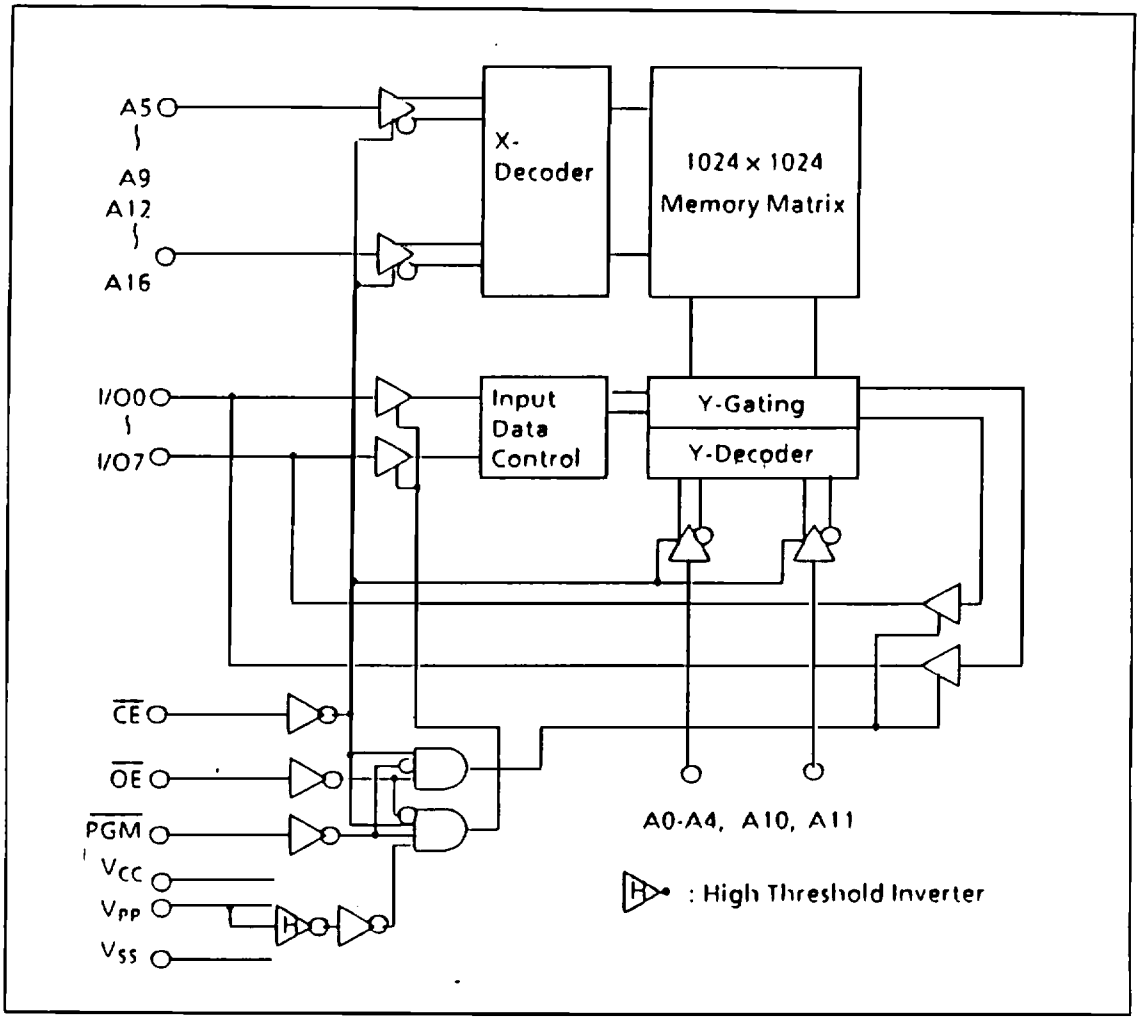


(Top View)

Pin Description

Pin name	Function
A0 – A16	Address
I/O0 – I/O7	Input/output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{PGM}$	Programming enable
V_{CC}	Power supply
V_{PP}	Programming power supply
V_{SS}	Ground
NC	No connection

Block Diagram



Mode Selection

Mode	TT RR	$\overline{CE}$ (22) (11)	$\overline{OE}$ (24) (9)	$\overline{PGM}$ (31) (2)	A9 (26) (7)	V_{PP} (1) (32)	V_{CC} (32) (1)	I/O (13 – 15, 17 – 21) (12 – 16, 18 – 20)
Read		V_{IL}	V_{IL}	V_{IH}	X	V_{CC}	V_{CC}	Dout
Output disable		V_{IL}	V_{IH}	V_{IH}	X	V_{CC}	V_{CC}	High-Z
Standby		V_{IH}	X	X	X	V_{CC}	V_{CC}	High-Z
Program		V_{IH}	V_{IH}	V_{IL}	X	V_{PP}	V_{CC}	Din
Program verify		V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	Dout
Page data latch		V_{IH}	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	Din
Page program		V_{IH}	V_{IH}	V_{IL}	X	V_{PP}	V_{CC}	High-Z
Program inhibit		V_{IL}	V_{IL}	V_{IL}	X	V_{PP}	V_{CC}	High-Z
		V_{IL}	V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	High-Z
		V_{IH}	V_{IL}	V_{IL}	X	V_{PP}	V_{CC}	High-Z
		V_{IH}	V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	High-Z
Identifier		V_{IL}	V_{IL}	V_{IH}	V_H*2	V_{CC}	V_{CC}	Code

Notes: 1. X: Don't care.
2. V_H: 12.0 V ± 0.5 V

Absolute Maximum Ratings

Item	Symbol	Value	Unit
All input and output voltages *1	Vin, Vout	–0.6*2 to +7.0	V
A9 input voltage *1	V_{ID}	–0.6*2 to +13.5	V
V_{PP} voltage *1	V_{PP}	–0.6 to +13.5	V
V_{CC} voltage *1	V_{CC}	–0.6 to +7.0	V
Operating temperature range	Topr	0 to +70	°C
Storage temperature range *3	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–10 to +80	°C

Notes: 1. Relative to V_{SS}.
2. Vin, Vout, V_{ID} min = –1.0 V for pulse width ≤ 50 ns

Capacitance (Ta = 25°C, f = 1 MHz)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	10	pF	Vin = 0 V
Output capacitance	Cout	—	—	15	pF	Vout = 0 V

Read Operation

DC Characteristics (V_{CC} = 2.7V to 5.5V, $V_{PP} = V_{CC}$, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2	µA	Vin = 0 V/V_{CC}
Output leakage current	I_{LO}	—	—	2	µA	Vout = 0 V/V_{CC}
V_{PP} current	I_{PP1}	—	1	20	µA	V_{PP} = 5.5 V
Standby V_{CC} current	I_{SB1}	—	—	1	mA	$\overline{CE}$ = V_{IH}
	I_{SB2}	—	1	20	µA	$\overline{CE}$ = V_{CC} ± 0.3 V
Operating V_{CC} current	I_{CC1}	—	—	30	mA	Iout = 0 mA, $\overline{CE}$ = V_{IL}
	I_{CC2}	—	—	30	mA	Iout = 0 mA, f = 5 MHz
		—	—	45	mA	Iout = 0 mA, f = 5.4 MHz
Input voltage*3	V_{IL}	−0.3*1	—	0.8	V	
	V_{IH}	2.2	—	V_{CC}+1*2	V	
Output voltage	V_{OL}	—	—	0.45	V	I_{OL} = 1.0 mA
		—		0.2	V	I_{OL} = 20 uA
	V_{OH}	2.4	—	—	V	I_{OH} = -400 uA
		V_{CC}−0.2	—	—	V	I_{OH} = −20 uA

Notes: 1. V_{IL} min = −1.0 V for pulse width ≤ 50 ns
2. V_{IH} max = V_{CC} +1.5 V for pulse width ≤ 20 ns
If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.
3 Only defined for DC test .V_{IL} max = 0.45 V and V_{IH} min = 0.45 V AC operation

AC Characteristics (V_{CC} = 2.7Vto 5.5V, V_{PP} = V_{CC}, Ta = 0 to +70°C)

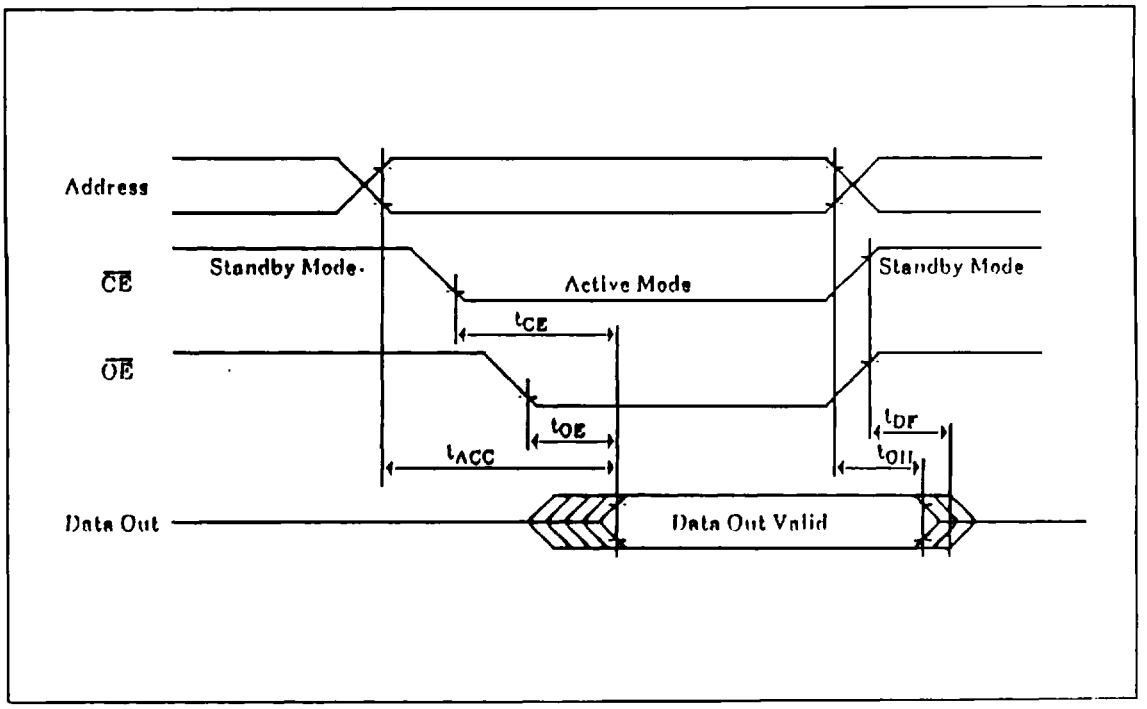
Test Conditions

Test Conditions
- Input pulse levels: 0.45 to 2.4 V
- Input rise and fall times: ≤ 10 ns
- Output load: 50 pF
- Reference levels for measuring timing: 0.8 V, 2.0 V

		HN27V101 ATT/RR-20		HN27V101 ATT/RR-25			
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**
Address to output delay	t_{ACC}	—	200	—	250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to output delay	t_{CE}	—	200	—	250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to output delay	t_{OE}	—	100	—	120	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ high to output float*[1]	t_{DF}	0	100	0	120	ns	$\overline{CE}$ = V_{IL}
Address to output hold	t_{OH}	0	—	0	—	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

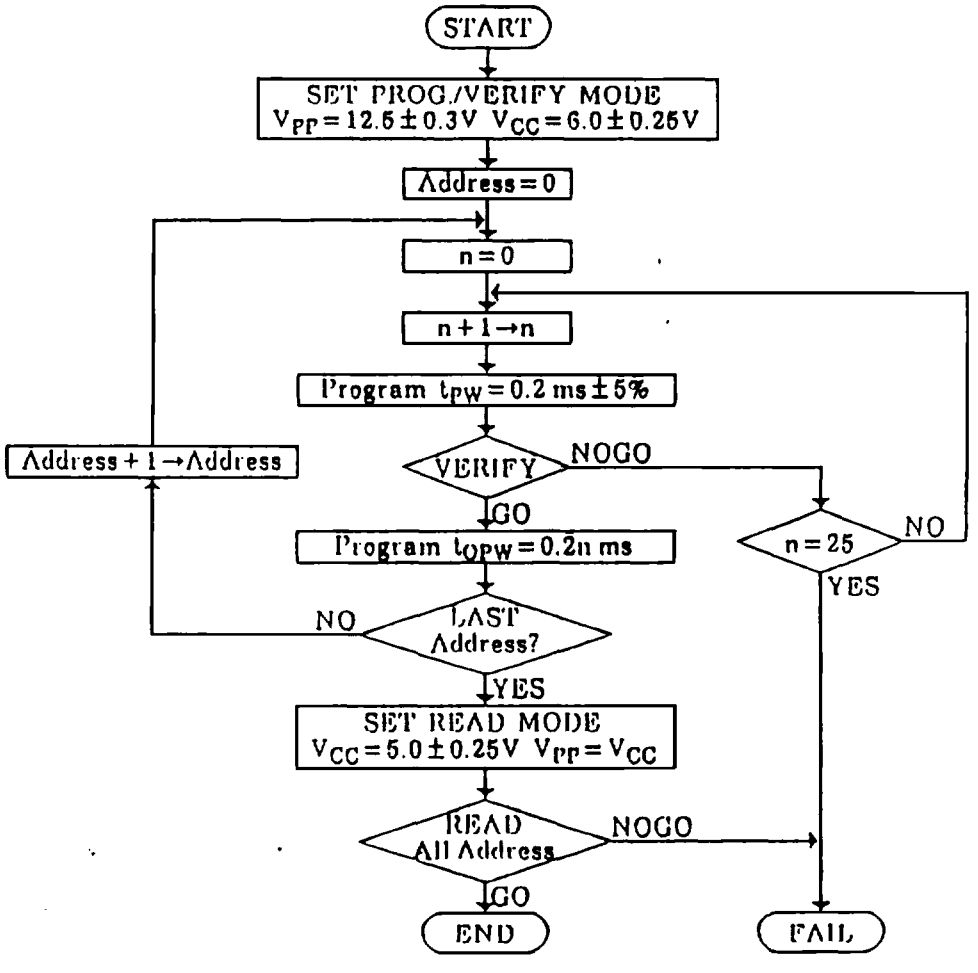
Note: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Read Timing Waveform



Fast High-Reliability Programming

This device can be applied the fast high-reliability programming algorithm shown in the following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



Fast High-Reliability Programming Flowchart

DC Characteristics (V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, Ta = 25°C ± 5°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2	µA	Vin = 0 V/V_{CC}
V_{PP} supply current	I_{PP}	—	—	40	mA	$\overline{CE}$=$\overline{PGM}$ = V_{IL}
Operating V_{CC} current	I_{CC}	—	—	30	mA	
Input voltage	V_{IL}	−0.1*5	—	0.8	V	
	V_{IH}	2.2	—	V_{CC}+0.5*6	V	
Output voltage during verify	V_{OL}	—	—	0.45	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	—	—	V	I_{OH} = −400 µA

Notes: 1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13.5 V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.5 V.
4. Do not alter V_{PP} either V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE}$ = low.
5. V_{IL} min = −0.6 V for pulse width < 20 ns.
6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics (V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, Ta=25°C ± 5°C)

Test Conditions

- Input pulse levels: 0.45 to 2.4 V
- Input rise and fall times: < 20 ns
- Reference levels for measuring timing:
  Inputs; 0.8 V, 2.0 V,
  Outputs; 0.8 V, 2.0 V

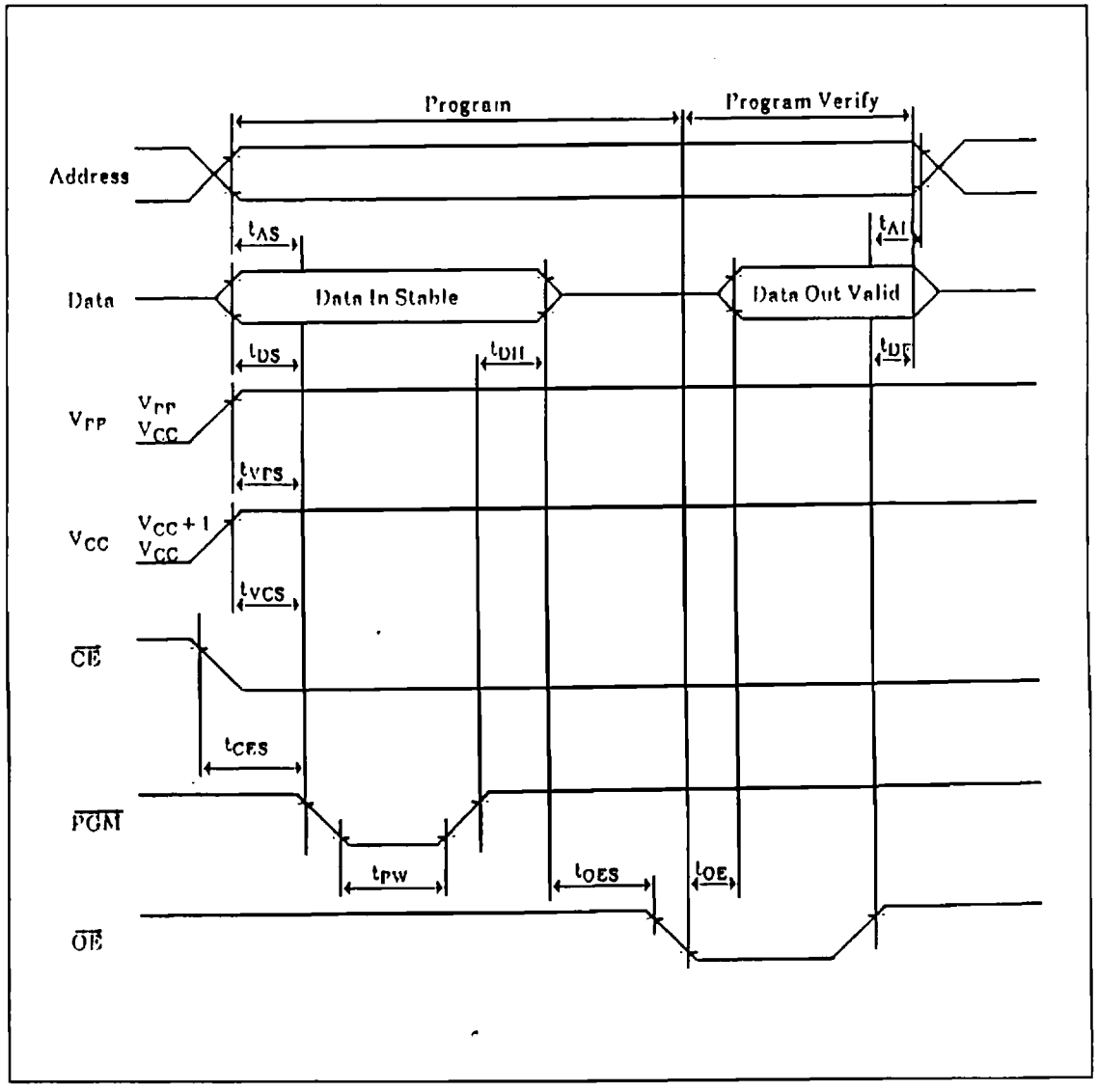
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	2	—	—	µs	
$\overline{OE}$ setup time	t_{OES}	2	—	—	µs	
Data setup time	t_{DS}	2	—	—	µs	
Address hold time	t_{AH}	0	—	—	µs	
Data hold time	t_{DH}	2	—	—	µs	
$\overline{OE}$ to output float delay	t_{DF}*1	0	—	130	ns	
V_{PP} setup time	t_{VPS}	2	—	—	µs	
V_{CC} setup time	t_{VCS}	2	—	—	µs	
$\overline{PGM}$ initial programming pulse width	t_{PW}	0.19	0.2	0.21	ms	

AC Characteristics (V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, Ta=25°C ± 5°C)(cont)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
$\overline{PGM}$ overprogramming pulse width	t_{OPW}*2	0.19	—	5.25	ms	
$\overline{CE}$ setup time	t_{CES}	2	—	—	µs	
Data valid from $\overline{OE}$	t_{OE}	0	—	150	ns	

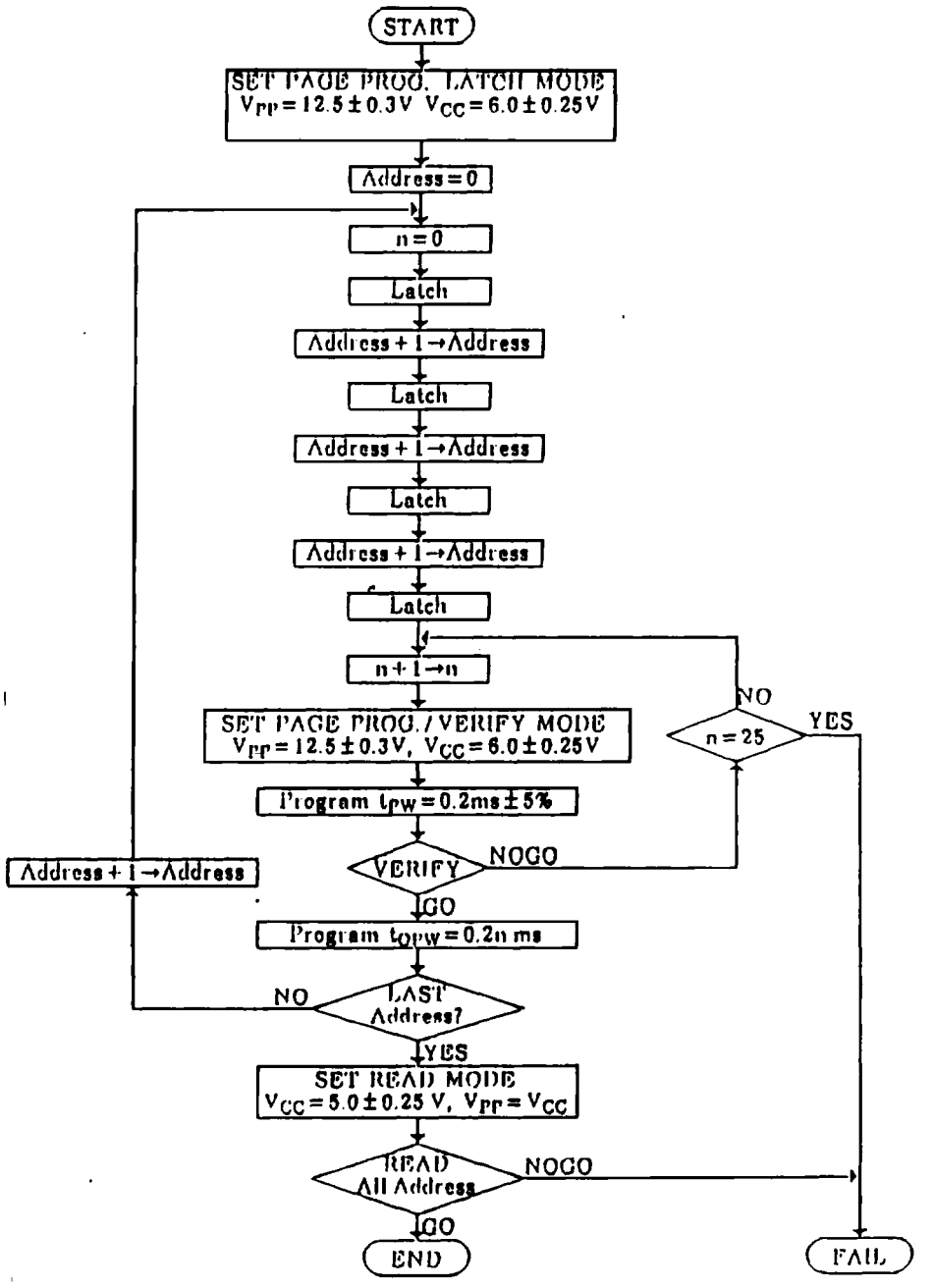
Notes: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
2. Refer to the programming flowchart for t_{OPW}.

Fast High-Reliability Programming Timing Waveform



Fast High-Reliability Page Programming

This device can be applied the fast high-reliability page programming algorithm shown in the following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



Fast High-Reliability Page Programming Flowchart

DC Characteristics (V_{CC} = 6 V ± 0.25 V, V_{PP} =12.5 V ± 0.3 V, Ta=25°C ± 5°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2	µA	Vin = 0 V/V_{CC}
Output voltage during verify	V_{OL}	—	—	0.45	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	—	—	V	I_{OH} = –400 µA
Operating V_{CC} current	I_{CC}	—	—	30	mA	
Input voltage*3	V_{IL}	–0.1*5	—	0.8	V	
	V_{IH}	2.2	—	V_{CC} +0.5*6	V	
V_{PP} supply current	I_{PP}	—	—	50	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IH}, $\overline{PGM}$ = V_{IL}

Notes: 1. VCC must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13.5 V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.5 V.
4. Do not alter V_{PP} either V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE}$ = low.
6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics (V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, Ta = 25°C ± 5°C)

Test Conditions

- Input pulse levels: 0.45 to 2.4 V
- Input rise and fall times: ≤ 20 ns
- Reference levels for measuring timings: 0.8 V, 2.0 V

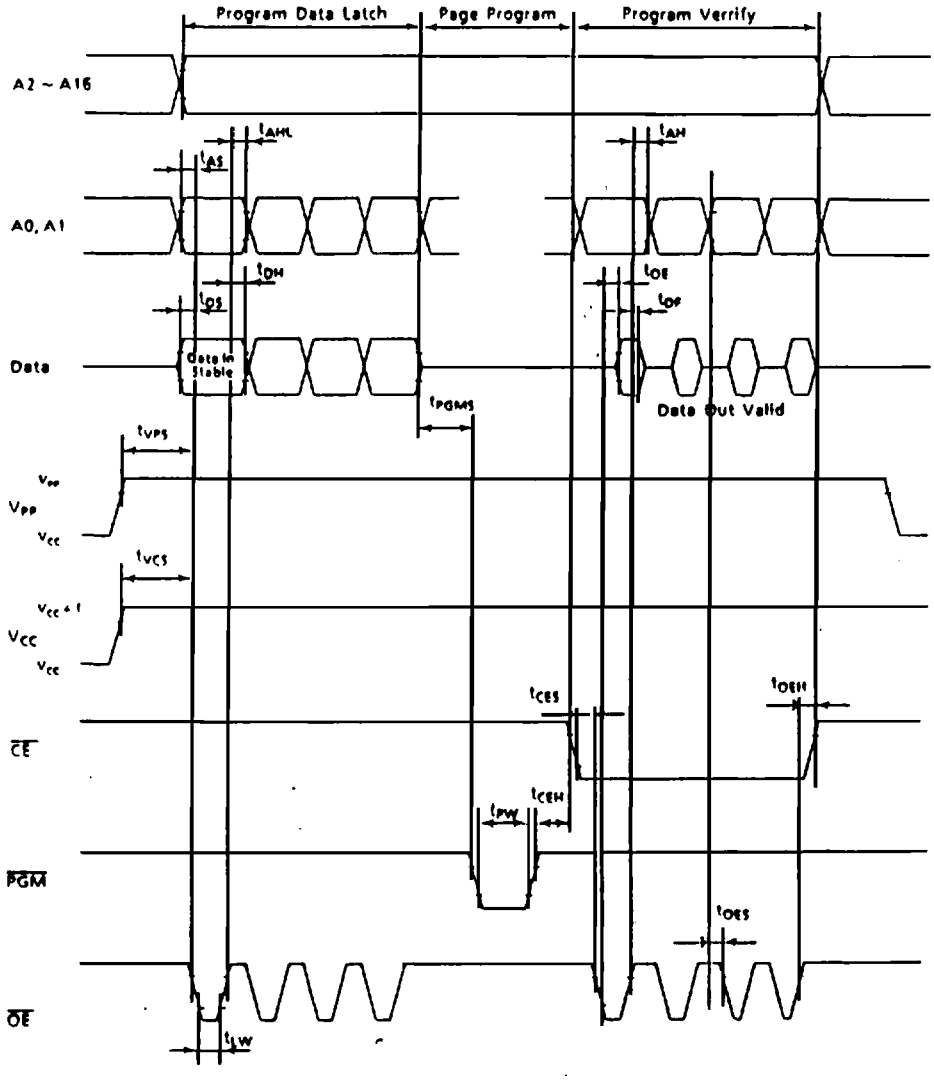
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	2	—	—	µs	
$\overline{OE}$ setup time	t_{OES}	2	—	—	µs	
Data setup time	t_{DS}	2	—	—	µs	
Address hold time	t_{AH}	0	—	—	µs	
	t_{AHL}	2	—	—	µs	
Data hold time	t_{DH}	2	—	—	µs	
$\overline{OE}$ to output float delay	t_{DF}*1	0	—	130	ns	
V_{PP} setup time	t_{VPS}	2	—	—	µs	
V_{CC} setup time	t_{VCS}	2	—	—	µs	
$\overline{PGM}$ initial programming pulse width	t_{PW}	0.19	0.2	0.21	ms	

AC Characteristics (V_{CC} = 6.V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, Ta = 25°C ± 5°C)(cont)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
$\overline{PGM}$ overprogramming pulse width	t_{OPW}*2	0.19	—	5.25	ms	
$\overline{CE}$ setup time	t_{CES}	2	—	—	µs	
Data valid from $\overline{OE}$	t_{OE}	0	—	150	ns	
$\overline{OE}$ pulse width during data latch	t_{LW}	1	—	—	µs	
$\overline{PGM}$ setup time	t_{PGMS}	2	—	—	µs	
$\overline{CE}$ hold time	t_{CEH}	2	—	—	µs	
$\overline{OE}$ hold time	t_{OEH}	2	—	—	µs	

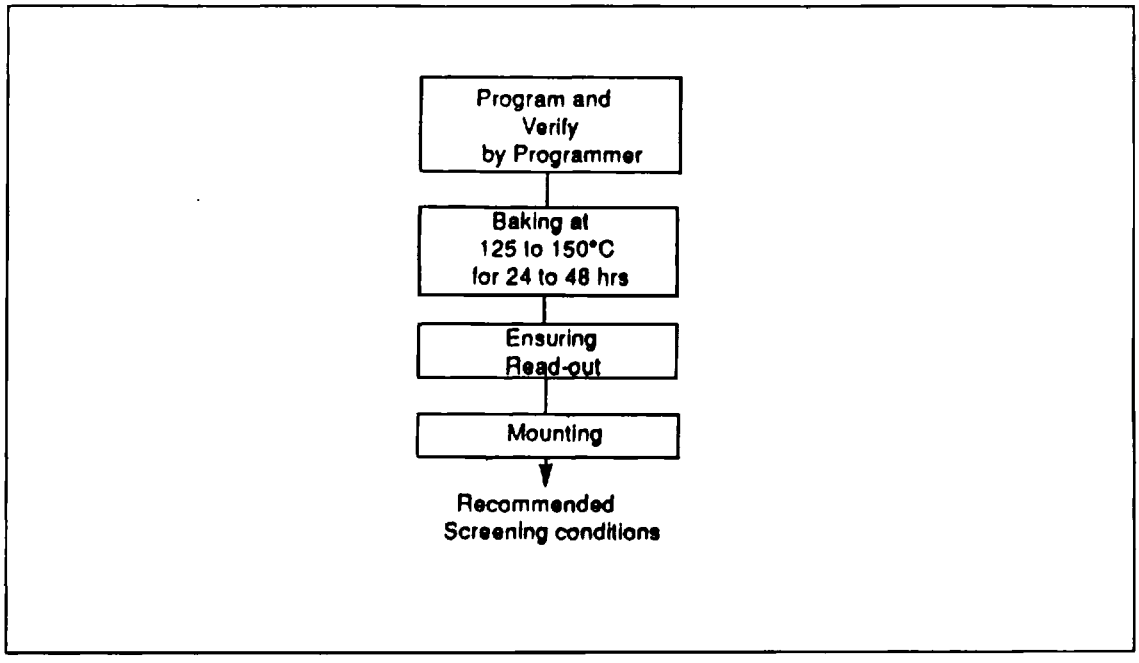
Notes: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
2. Refer to the programming flowchart for t_{OPW}.

Fast High-Reliability Page Programming Timing Waveform



Recommended Screening Conditions

Before mounting, please make the screening (baking without bias) shown in the right.



Mode Description

Device Identifier Mode

The device identifier mode allows the reading out of binary codes that identify manufacturer and type of device, from outputs of OTPROM. By this mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.

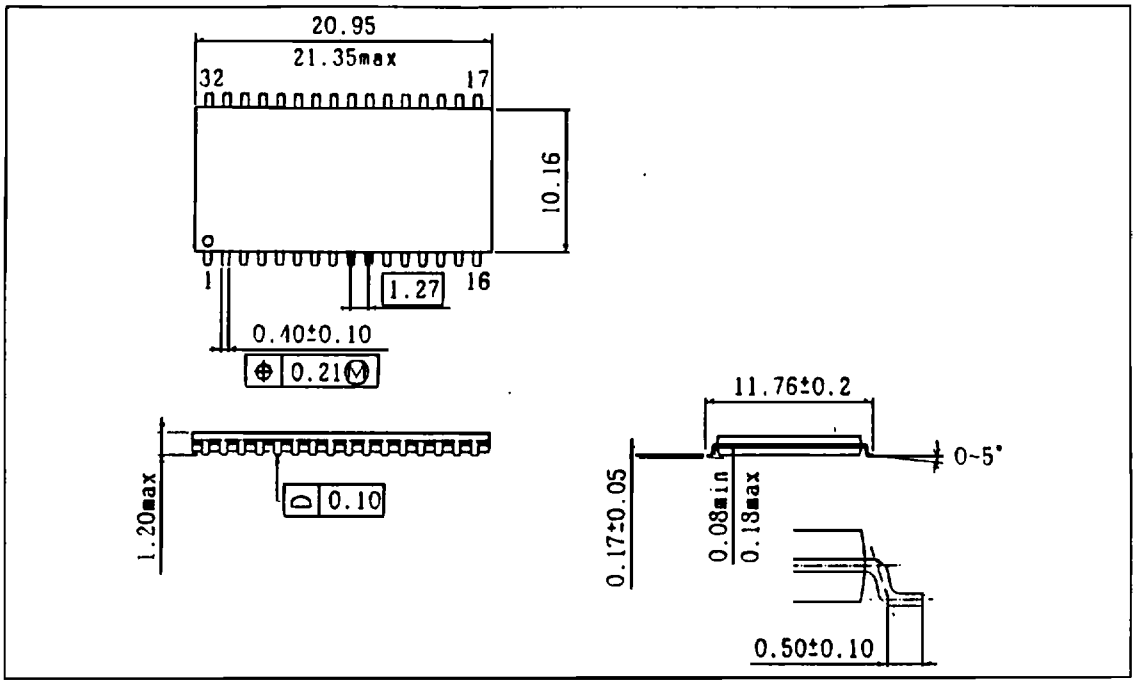
HN27V101A Identifier Code

Identifier	TT / RR	A0 (12) / (21)	A9 (26) / (7)	I/O7 (21) / (12)	I/O6 (20) / (13)	I/O5 (19) / (14)	I/O4 (18) / (15)	I/O3 (17) / (16)	I/O2 (15) / (18)	I/O1 (14) / (19)	I/O0 (13) / (20)	Hex Data
Manufacturer code		V_{IL}	V_H	0	0	0	0	0	1	1	1	07
Device code		V_{IH}	V_H	0	0	1	1	1	0	0	0	38

Notes: 1. V_H = 12.0 V ± 0.5 V
2. A1–A8, A10–A16, $\overline{CE}$, $\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}

Package Dimensions

HN27V101ATT Series (TTP-32D) **Unit: mm**



HN27V101ARR Series (TTP-32D) **Unit: mm**

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