7.3 CY7C602 Electrical and Mechanical Characteristics

7.3.1 CY7C602 Maximum Ratings

Storage Temperature ..... −65° C to +150° C
Ambient Temperature with Power Applied ..... −55° C to +125° C
Supply Voltage to Ground Potential [1] ..... −0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V
DC Input Voltage ..... −3.0V to +7.0V
Output Low Sink Current ..... 4.0 mA

7.3.2 CY7C602 Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0° C to 85° C	5V ± 10%

7.3.3 CY7C602 DC Characteristics Over the Operating Range

Parameters	Description	Test Conditions	Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.5	V
V_{IH}	Input HIGH Voltage		2.1		V
V_{IL}	Input LOW Voltage		−3.0	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}	−10	10	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = V_{SS}	−10	10	µA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \le V_{OUT} \le V_{CC}$	−10	10	µA
I_{CCQ}	Quiescent Supply Current	$V_{SS} \le V_{IN} \le V_{IL}$ or $V_{IH} \le V_{IN} \le V_{CC}$		150	mA
I_{CC}	Supply Current, Commercial	V_{CC} = Max., f = 40 MHz		450	mA
		V_{CC} = Max., f = 33 MHz		400	
		V_{CC} = Max., f = 25 MHz		350	

7.3.4 CY7C602 Capacitance [3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	V_{CC} = 5.0 V, T_A = 25° C, f = 1 MHz	15	pF
C_{OUT}	Output Capacitance	V_{CC} = 5.0 V, T_A = 25° C, f = 1 MHz	20	pF
C_{IO}	I/O Bus Capacitance	V_{CC} = 5.0 V, T_A = 25° C, f = 1 MHz	15	pF
$C_{\overline{DOE}}$	$\overline{DOE}$ Input Capacitance	V_{CC} = 5.0 V, T_A = 25° C, f = 1 MHz	30	pF
C_{CLK}	CLK Input Capacitance	V_{CC} = 5.0 V, T_A = 25° C, f = 1 MHz	25	pF

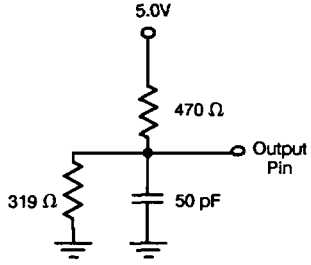
Notes:

1. All power and ground pins must be connected to the other pins of same type before any power is applied to the part.
2. Ambient temperature is the 'instant on' case temperature.
3. Tested initially and after any design or process changes that may affect these parameters.

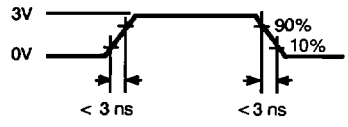
7.3.5 CY7C602 AC Characteristics

Parameter	Description	Reference Edge	CY7C602-25		CY7C602-33		CY7C602-40		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
1	Clock Cycle		40		30		25		ns
2	Clock High and Low		18		13		11		ns
3	A(31:2) Set-Up	CLK+	3		3		2		ns
4	A(31:2) Hold	CLK+	6		6		6		ns
5	D(31:0) Input Set-Up	CLK+	3		2		2		ns
6	D(31:0) Input Hold	CLK+	5		5		4		ns
7	D(31:0) Output Delay	CLK-		20		15		13	ns
8	D(31:0) Data Valid	CLK-	4		4		4		ns
9	D(31:0) Output Turn-Off	FLUSH		31		22		18	ns
10	D(31:0) Output Valid	FLUSH	0		0		0		ns
11	D(31:0) Output Turn-Off	$\overline{DOE}$+		15		11		9	ns
12	D(31:0) Output Turn-On	$\overline{DOE}$-		15		11		9	ns
13	D(31:0) Output Valid	$\overline{DOE}$-	0		0		0		ns
14	FINS1/2 Set-Up	CLK+	9		9		7		ns
15	FINS1/2 Hold	CLK+	2.5		2.5		2.5		ns
16	INST Setup	CLK+	16		12		9		ns
17	INST Hold	CLK+	2		2		2		ns
18	FXACK Set-Up	CLK+	16		12		9		ns
19	FXACK Hold	CLK+	2		2		2		ns
20	FLUSH Set-Up	CLK+	21		14		11		ns
21	FLUSH Hold	CLK+	2		2		2		ns
22	$\overline{RESET}$ Set-Up	CLK+	15		10		8		ns
23	$\overline{RESET}$ Hold	CLK+	3		3		2		ns
24	$\overline{MHOLD}$ Set-Up	CLK-	7		4		3		ns
25	$\overline{MHOLD}$ Hold	CLK-	6		5		4.5		ns
26	$\overline{MDS}$ Set-Up	CLK-	5		4		3		ns
27	$\overline{MDS}$ Hold	CLK-	6		5		4.5		ns
28	$\overline{FHOLD}$ Delay	CLK-		29		23		19	ns
29	$\overline{FHOLD}$ Valid	CLK-	6		6		5.5		ns
30	$\overline{FHOLD}$ Delay	FINS1/2		16		15		12	ns
31	$\overline{FHOLD}$ Delay	FLUSH		28		20		16	ns
32	$\overline{FHOLD}$ Delay	$\overline{MHOLD}$-		36		27		22	ns
33	FCCV Delay	CLK-		29		23		19	ns
34	FCCV Valid	CLK-	8		6		5.5		ns
35	FCCV Delay	FLUSH		28		20		16	ns
36	FCCV Delay	$\overline{MHOLD}$-		36		27		22	ns
37	FCC(1:0) Delay	CLK+	26		19		17		ns
38	FCC(1:0) Valid	CLK+	5		4		3		ns
39	$\overline{FEXC}$ Delay	CLK+		26		19		17	ns
40	$\overline{FEXC}$ Valid	CLK+	5		4		3		ns
41	FNULL Delay	CLK+		20		13		11	ns
42	FNULL Valid	CLK+	3		3		3		ns

7.3.6 CY7C602 AC Test Loads and Waveforms



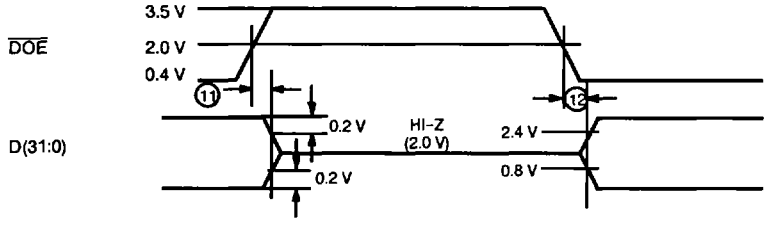
Test Load



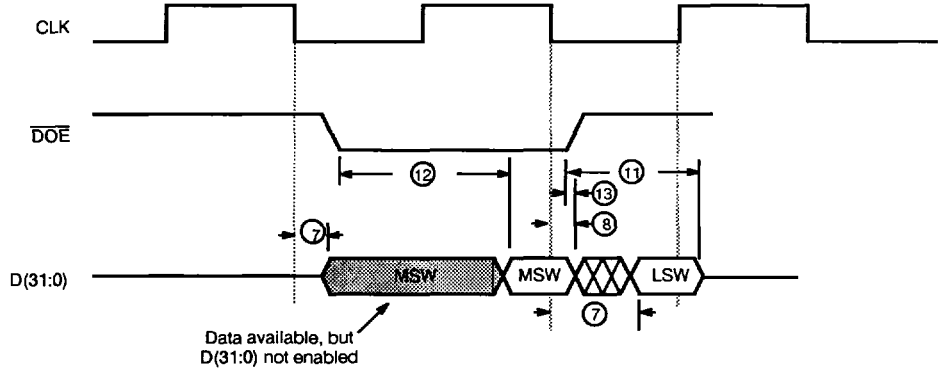
Waveform

7.3.7 CY7C602 AC Waveforms

Three-State Timing



Asynchronous Store Timing



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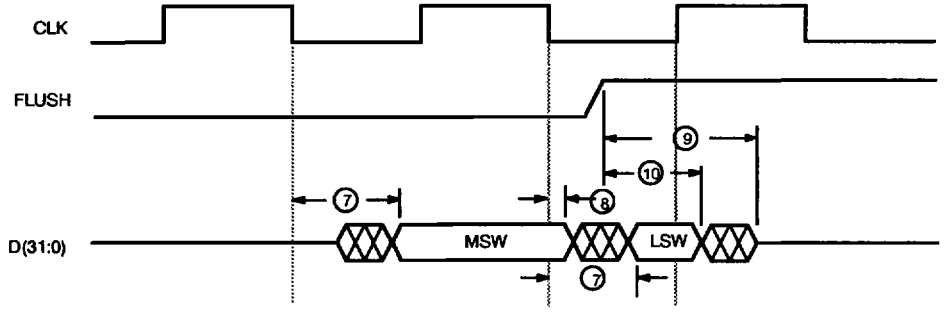
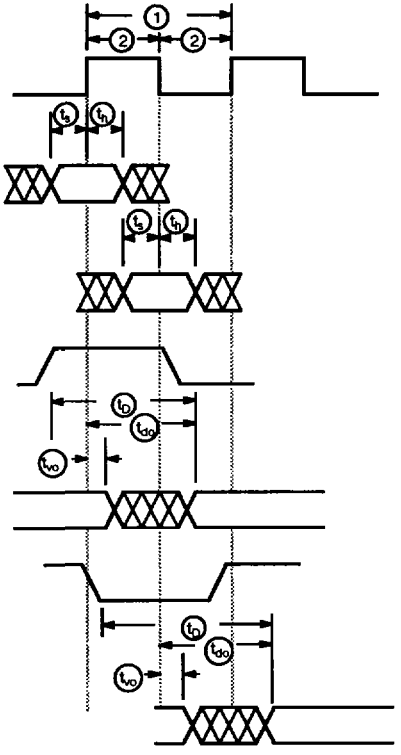
Effect of FLUSH on Store Timing



General Timing Parameters



7.3.8 CYC7602 Pin Assignments

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A		D22	A22	D24	A24	A25	D26	A26	A27	A28	A29	A30	A31	D31	GND	A
B	D21	VCC	VCC	A23	D23	VCC	D25	VCC	D27	D28	D29	D30	VCC	VCC	VCC	B
C	D20	A21	GND	GND	VCC	GND	NC	VCC	GND	GND	GND	GND	GND	VCC	FCCV	C
D	D19	VCC	GND										GND	GND	FCC1	D
E	A18	A19	A20										CCCV	FCC0	FXACK	E
F	A16	D17	D18										$\overline{\text{RESET}}$	GND	$\overline{\text{FEXC}}$	F
G	D16	A17	GND										CLK	GND	FNULL	G
H	A0	A1	D0										GND	$\overline{\text{CHOLD}}$	$\overline{\text{FHOLD}}$	H
J	D1	$\overline{\text{DOE}}$	NC										VCC	MHOLDA	$\overline{\text{BHOLD}}$	J
K	D2	VCC	GND										VCC	$\overline{\text{MDS}}$	MHOLDB	K
L	A2	D3	GND										FLUSH	VCC	VCC	L
M	A3	VCC	D5										GND	FINS1	INST	M
N	D4	VCC	GND	GND	GND	D8	GND	D10	NC	GND	D14	GND	GND	VCC	FINS2	N
P	A4	VCC	GND	A6	VCC	A8	VCC	A11	D12	VCC	VCC	VCC	D15	VCC	VCC	P
R	A5	VCC	D6	A7	D7	A9	D9	A10	D11	A12	A13	D13	A14	A15	$\overline{\text{FP}}$	R
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

CY7C602
144-PIN PGA

TOP VIEW
(cavity down)

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7.3.9 CY7C602 Package Diagrams