TOSHIBA RISC PROCESSOR **TENTATIVE**

TMPR4951F

(64-bit RISC MICROPROCESSOR)

1. GENERAL DESCRIPTION

The TMPR4951F is a 64-bit RISC (Reduced Instruction Set Computer) microprocessor that is a low-cost, low-power microprocessor developed for interactive consumer applications including LBP, set-top terminals and video games.

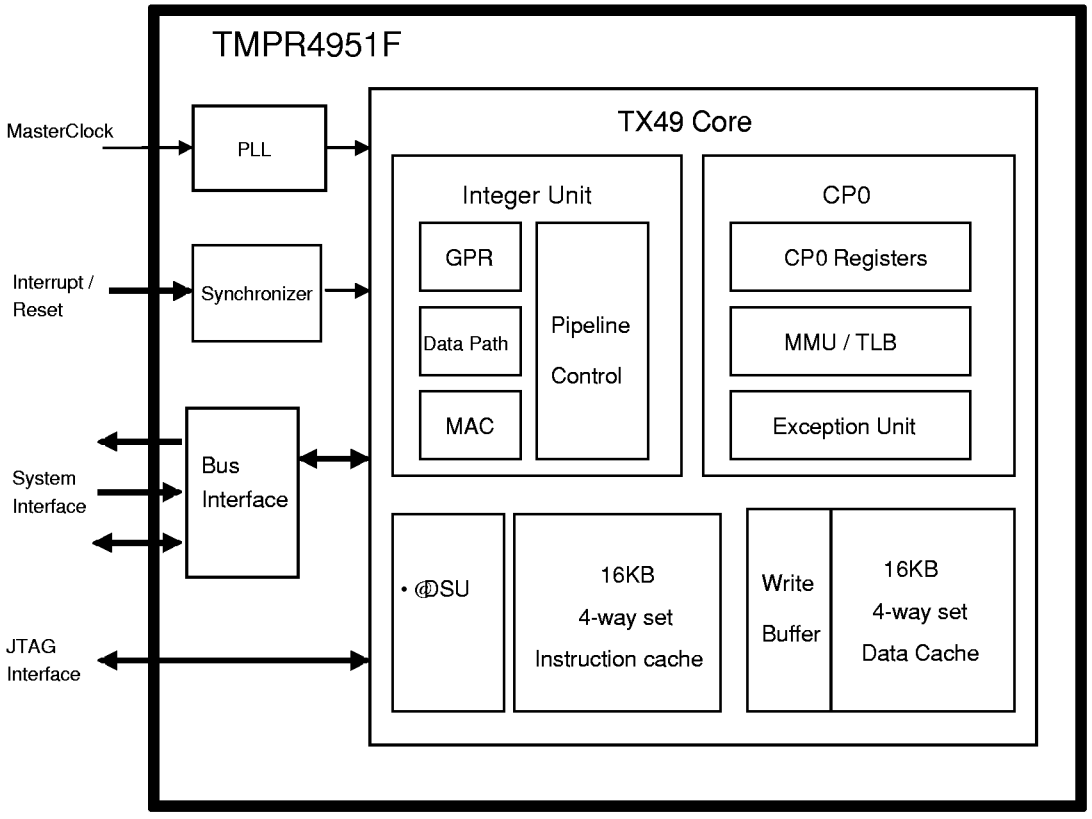
2. FEATURES

True 64-bit microprocessor, with TX49 core.
Optimized 5-stage pipeline
With 32-bit System Address Data bus
32-bit physical address space, 64-bit virtual address space.
On-chip 16-Kbyte Instruction Cache, 16-Kbyte Data Cache.
4-way set associative and Lock function support
Low power consumption
- 3.3 V power supply
- Reduced power mode

Instruction cache prefetching
Memory manegement unit containing 48-double entry JTLB
2-entry Instruction TLB and 4-entry Data TLB
Software compatibility with all MIPS processors
JTAG support
Package : QFP120pin

3. SYSTEM CONFIGURATION

3.1 TMPR4951F BLOCK DIAGRAM



4. PIN DESCRIPTION

4.1 PIN OUT (120 pin QFP)

PIN OUT	I / O	PIN NAME	PIN OUT	I / O	PIN NAME	PIN OUT	I / O	PIN NAME	PIN OUT	I / O	PIN NAME
1		VCC	31		VSS	61		VSS	91		VCC
2		VSS	32		VCC	62		VCC	92		VSS
3	I / O	SysAD22	33	I / O	SysAD16	63	I	JTDI	93	I	NMI*
4	I / O	SysAD21	34	I / O	SysAD15	64	I / O	SysAD4	94	I / O	SysAD26
5		VCC	35		VSS	65	O	JTDO	95	O	PMaster*
6		VSS	36		VCC	66	I / O	SysAD3	96		VCC
7	I / O	SysAD20	37	I / O	SysAD14	67		VSS	97		VSS
8		VCC	38	I / O	SysAD13	68		VCC	98	I / O	SysAD25
9	I	VCCP	39		VSS	69	I / O	SysAD2	99	I	EReq*
10	I	VSSP	40		VCC	70	I / O	SysAD1	100	I / O	SysCmd0
11	I	PLLCAP0	41	I / O	SysAD12	71		VSS	101		VCC
12	I	PLLCAP1	42	I / O	SysAD11	72		VCC	102		VSS
13		VCCP	43		VSS	73	I / O	SysAD0	103	I / O	SysCmd1
14		VSSP	44		VCC	74	O	PReq*	104	I	Reset*
15		VCC	45	I / O	SysAD10	75		VSS	105	I	EValid*
16	I	MasterClock	46	I	Int0*	76		VCC	106	I / O	SysCmd2
17		VSS	47	I / O	SysAD9	77	I / O	SysAD31	107		VCC
18	O	TClock	48		VSS	78	O	PValid*	108		VSS
19		VCC	49		VCC	79		VSS	109	I / O	SysCmd3
20		VSS	50	I / O	SysAD8	80		VCC	110	I	ColdReset*
21	O	SyncOut	51	I / O	SysAD7	81	I / O	SysAD30	111	I / O	SysCmd4
22	I / O	SysAD19	52	I	JTMS	82	I	EOK*	112	I	DivMode1
23		VCC	53		VSS	83	I / O	SysAD29	113		VCC
24	I	SyncIn	54		VCC	84		VSS	114		VSS
25		VSS	55	I / O	SysAD6	85		VCC	115	I / O	SysAD24
26	I / O	SysAD18	56	I / O	SysAD5	86	I / O	SysAD28	116	I	DivMode0
27	I / O	SysAD17	57	I	JTCK	87	I / O	SysAD27	117	I / O	SysAD23
28	I	Int4*	58	I	Int1*	88	I	Int2*	118	I	Int3*
29		VCC	59		VSS	89		VSS	119		VCC
30		VSS	60		VCC	90		VCC	120		VSS

4.2 PIN FUNCTION

The following is a list of interface, interrupt, and miscellaneous pins available on the TMPR4951F.

SYSTEM INTERFACE

PIN NAME	I / O	FUNCTION
SysAD(31:0)	I / O	System address / data bus A 32-bit address and data bus for communication between the processor and an external agent.
SysCmd(4:0)	I / O	System command / data identifier bus A 5-bit bus for command and data identifier transmission between the processor and an external agent.
EValid*	I	External agent valid input The external agent asserts EValid* when it is driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
PValid*	O	Processor valid output The processor asserts PValid* when it is driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
EReq*	I	External request An external agent asserts EReq* to request use of the System interface.
PReq*	O	Processor request Processor asserts PReq* to request use of the System interface.
EOK*	I	External agent ready The external agent asserts EOK* to indicate that it can accept a processor request.
PMaster*	O	Processor master Indicates the processor is master of the System interface bus.

CLOCK / CONTROL INTERFACE

PIN NAME	I / O	FUNCTION
MasterClock	I	Master clock Master clock input that establishes the processor operating frequency.
TClock	O	Transmit clock Transmit clock at the operational frequency of the system interface.
SyncOut	O	Synchronization clock out Synchronization clock output. Must be connected to SyncIn through an interconnect that models the interconnect between TClock and the external agent.
SyncIn	I	Synchronization clock in Synchronization clock input. See SyncOut.
DivMode(1:0)	I	Set the operational frequency of the System interface DivMode[1:0] MasterClock PClock TClock 0 33.3MHz 133MHz 33.3MHz 1 Reserved 2 66.6MHz 133MHz 66.6MHz 3 44.4MHz 133MHz 44.4MHz

INTERRUPT INTERFACE

PIN NAME	I / O	FUNCTION
Int(4:0)*	I	Interrupt Five general processor interrupts, bit-wise ORed with bits 4:0 of the interrupt register and visible as bits 14:10 of the Cause register.
NMI*	I	Non-maskable interrupt Non-maskable interrupt, ORed with bit 6 of the interrupt register.

JTAG INTERFACE

PIN NAME	I / O	FUNCTION
JTDI	I	JTAG data in Data is serially scanned in through this pin.
JTCK	I	JTAG clock input The processor receives a serial clock on JTCK. On the rising edge of JTCK, both JTDI and JTMS are sampled.
JTDO	O	JTAG data out Data is serially scanned out through this pin.
JTMS	I	JTAG command JTAG command signal, indicating the incoming serial data is command data.

INITIALIZATION INTERFACE

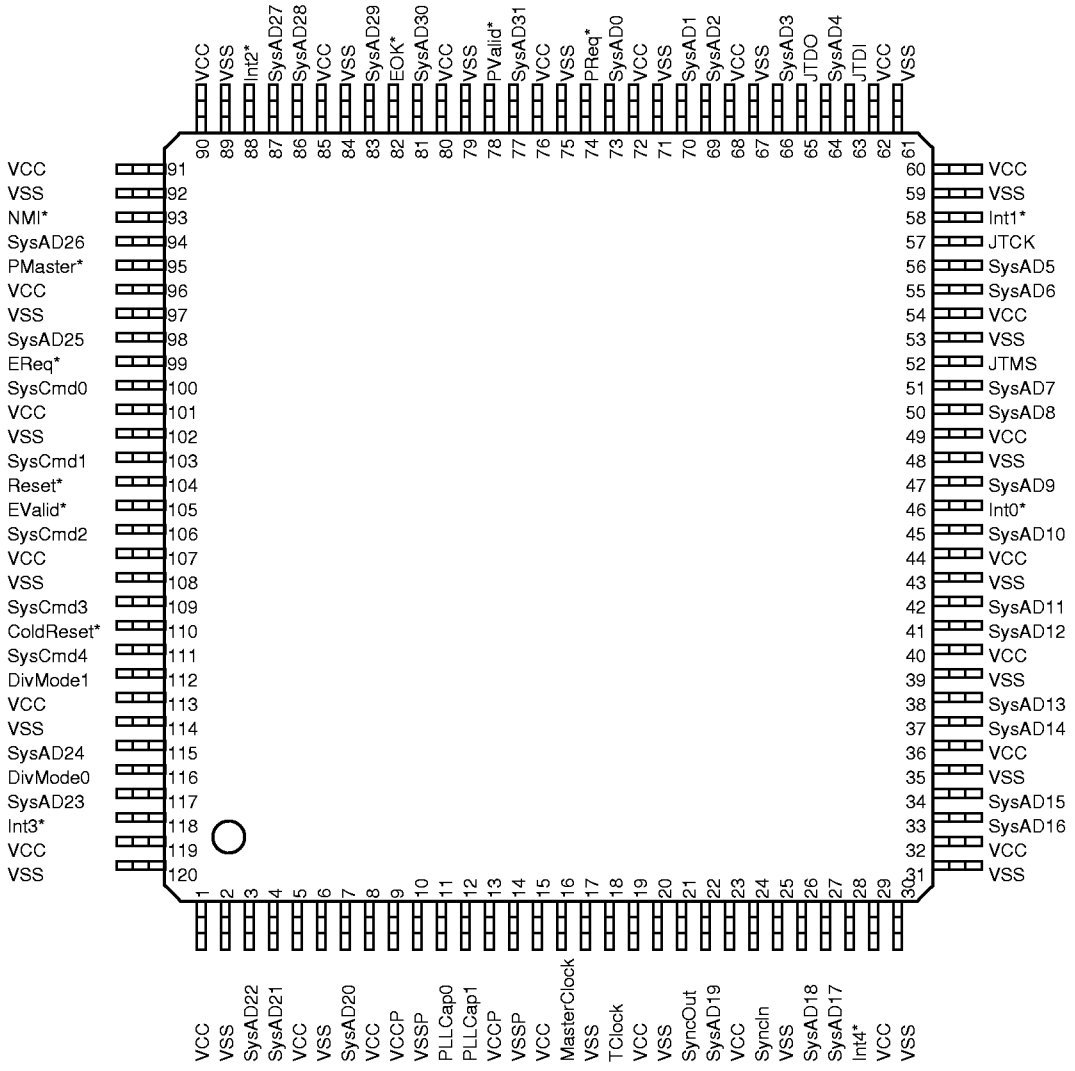
PIN NAME	I / O	FUNCTION
Reset*	I	Soft (Warm) Reset This signal must be asserted synchronously with MasterClock for a soft reset.
ColdReset*	I	Cold reset This signal indicates to the processor that the +3.3V power supply is stable and the processor should initiate a cold reset sequence, resetting the PLL.
PLLCAP0	I	PLL capacitor A capacitor is connected between PLLCAP0 and the VSSP to ensure the proper operation of the phase-locked loop.
PLLCAP1	I	PLL capacitor A capacitor is connected between PLLCAP1 and the VCCP to ensure the proper operation of the phase-locked loop.

OTHERS

PIN NAME	I / O	FUNCTION
VCCP	I	Quiet V_{CC} for PLL Quiet V_{CC} for the internal phase locked loop.
VSSP	I	Quiet V_{SS} for PLL Quiet V_{SS} for the internal phase locked loop.
VCC	I	Vcc Power supply pin
VSS	I	Vss Ground pin

4.3 PIN ASSIGNMENT

PHYSICAL SPECIFICATIONS QFP 120 pin (TMPR4951F)



5. ELECTRICAL CHARACTERISTICS

5.1 ABSOLUTE MAXIMUM RATINGS

TMPR4951F-133

V_{SS} = 0 V (GND)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply voltage	V_{CC}	-0.5 to 4.6	V
Input voltage(*1)	V_{IN}	-0.5 to V_{CC} + 0.5	V
Storage Temperature	T_{STG}	-65 to +150	°C

Note) If LSI is used above the maximum ratings, permanent destruction of LSI can result. In addition, it is desirable to use LSI for normal operation under the recommended condition. If these conditions are exceeded, reliability of LSI may be adversely affected.

(*1) VIN Min. = -1.5V for pulse width less than 10 ns.

5.2 RECOMMENDED OPERATING CONDITIONS

TMPR4951F-133

V_{SS} = 0 V (GND)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	Unit
Supply Voltage	V_{CC}		3.0	3.6	V
Operating Case Temperature	T_C		0	+85	°C

5.3 DC CHARACTERISTICS

TMPR4951F-133

T_C = 0°C to 85°C, V_{CC} = 3.3 V ± 0.3 V

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
Output High Voltage	V_{OH}	V_{CC} = Min. I_{OH} = -4 mA	2.4		V
Clock Output High Voltage (*3)	V_{OHC}	V_{CC} = Min. I_{OH} = -4 mA	2.7		V
Output Low Voltage	V_{OL}	V_{CC} = Min. I_{OL} = 4 mA		0.4	V
Input High Voltage (*2)	V_{IH}		2.0	V_{CC} + 0.3	V
Input Low Voltage (*1,2)	V_{IL}		-0.5 (*1)	0.8	V
MasterClock Input High Voltage	V_{IHC}		0.8 V_{CC}	V_{CC} + 0.3	V
MasterClock Input Low Voltage	V_{ILC}		-0.5 (*1)	0.2 V_{CC}	V
Operating Current	I_{CC}	V_{CC} = 3.6V, T_C = 0°C		T.B.D.	A
High Level Input Leakage	I_{LIH}			10	mA
Low Level Input Leakage (*4)	I_{LIL}			-30	mA
Low Level Input Leakage (*5)	I_{LIL}			-10	mA
High Level Output Leakage	I_{LOH}			20	mA
Low Level Output Leakage	I_{LOL}			-20	mA
Input Capacitance	C_{IN}			10	pF
Output Capacitance	C_{OUT}			10	pF

(*1) V_{IL} Min. = -1.5V for pulse width less than 10 ns.
(*2) Except for MasterClock input
(*3) Applies to TClock output
(*4) Applies to Int(4:1)*, JTMS, JTCK, JTDI, EReq*, Reset*, DivMode(1:0) inputs
(*5) Applies to all input signals except for (*4)

5.4 AC CHARACTERISTICS

5.4.1 CLOCK TIMING

TMPR4951F-133 T_C = 0 °C to 85 °C, V_{CC} = 3.3 V ± 0.3 V

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
MasterClock High	t_{MCH}	Transition 5 ns	4.0		ns
MasterClock Low	t_{MCL}	Transition 5 ns	4.0		ns
MasterClock Frequency (*1)	f_{MCK}		20	66.7	MHz
Internal Operation Frequency	f_{PCK}		50	133	MHz
MasterClock Period	t_{MCP}		15	50	ns
Clock Jitter	t_{MCJ}			+/- 500	ps
MasterClock Rise Time	t_{MCR}			4.0	ns
MasterClock Fall Time	t_{MCF}			4.0	ns

(*1) Operation of TMPR4951F is only guaranteed with the Phase Lock Loop enabled.
(*2) All output timings assume a 50 pF capacitive load. Output timings should be derated where appropriate.

5.4.2 SYSTEM INTERFACE

TMPR4951F-133 T_C = 0 to 85 °C, V_{CC} = 3.3 V ± 0.3 V

PARAMETER	SYMBOL	MIN.	MAX.	UNITS
Data Output *1,2,3	t_{DO}	2.0	8.0	ns
Data Setup *3	t_{DS}	3.5		ns
Data Hold *3	t_{DH}	1.5		ns
Clock Rise Time *4	t_{CORise}		4.0	ns
Clock Fall Time *4	t_{COFall}		4.0	ns
Clock High Time *4	t_{COHigh}	4.0		ns
Clock Low Time *4	t_{COLow}	4.0		ns

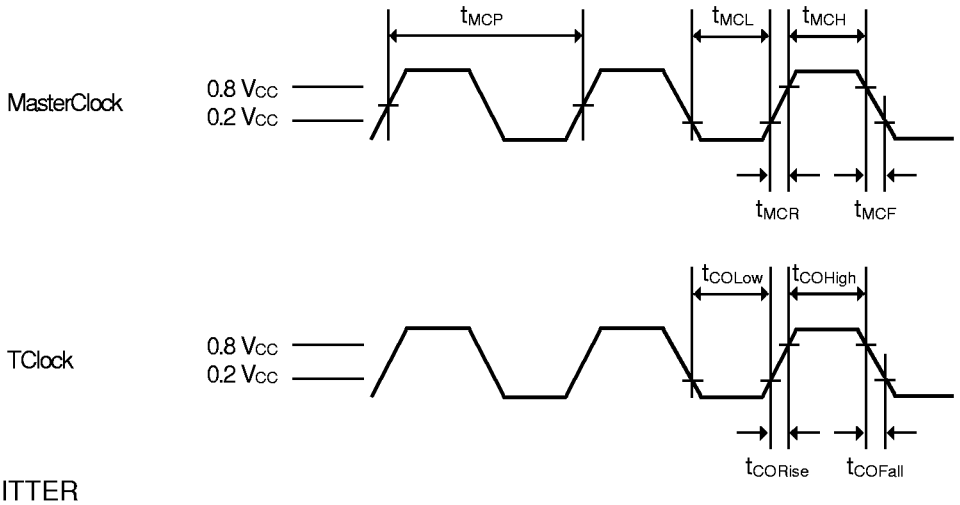
(*1) Timings are measured from 1.5V of the SClock to 1.5V of signal.
(*2) Capacitive load for all output timings is 50 pF.
(*3) Data Output, Data Setup and Data Hold apply to all logic signals driven out of or driven into the TMPR4951F on the system interface. Clocks are specified separately.
(*4) TClock.

5.4.3 CAPACITIVE LOAD DERATION T_C = 0°C to 85 °C, V_{CC} = 3.3 V ± 0.3 V

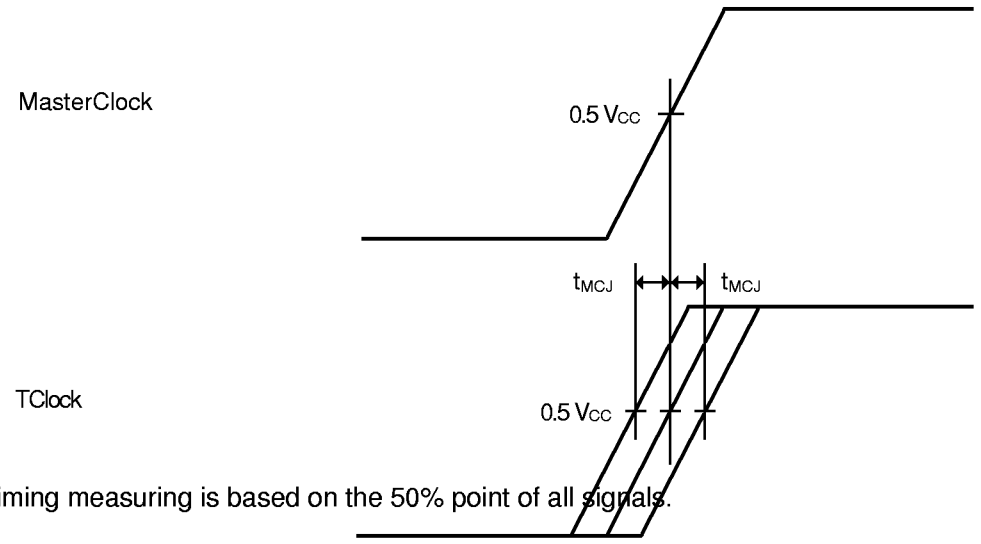
PARAMETER	SYMBOL	MIN.	MAX.	UNITS
Load Derate	C_{LD}		2.0	ns / 25 pF

5.5 TIMING DIAGRAMS

5.5.1 CLOCK TIMING

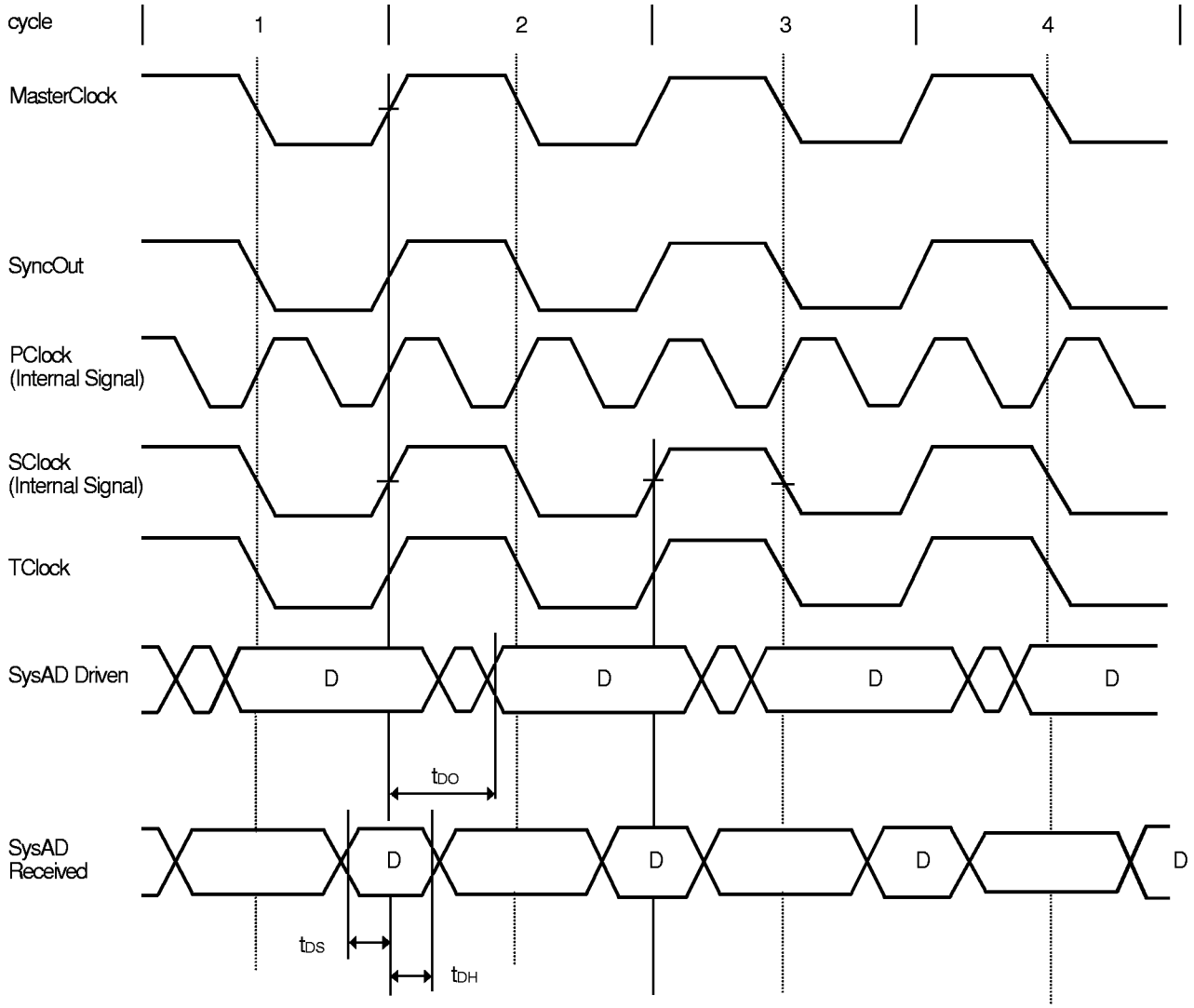


5.5.2 CLOCK JITTER

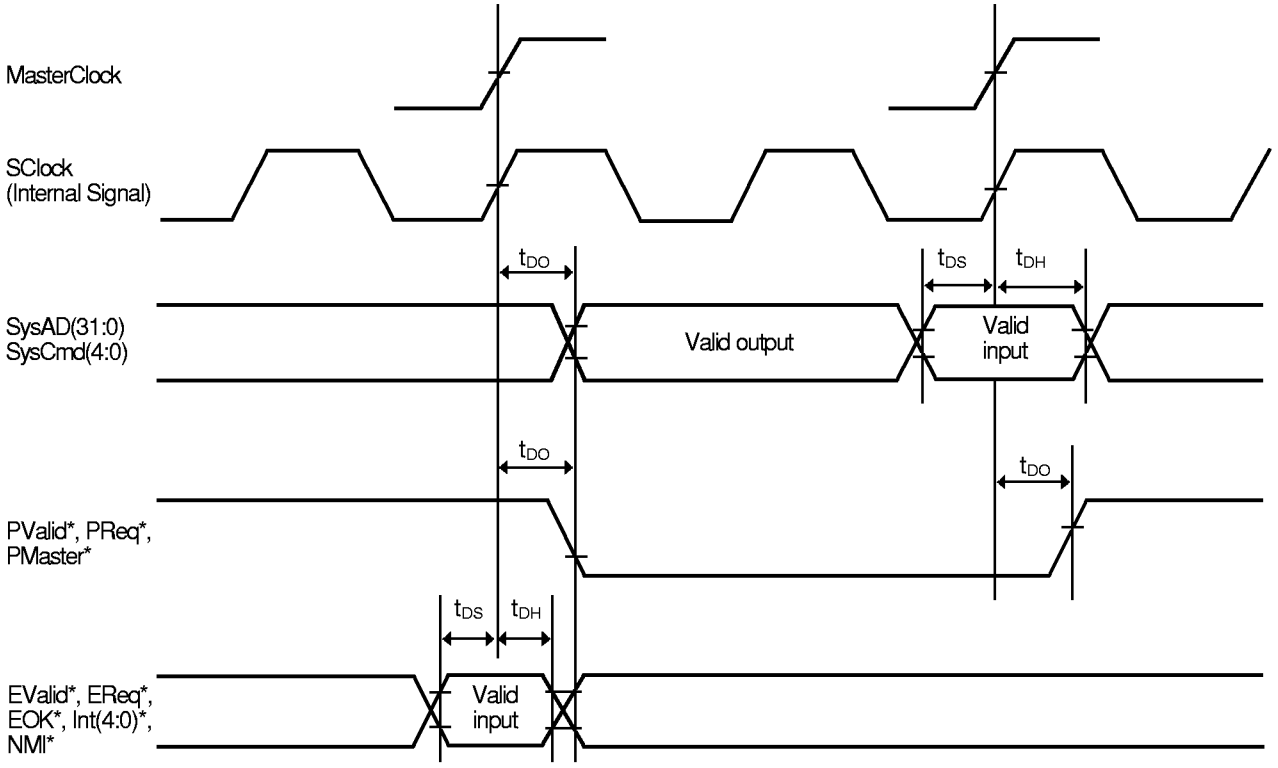


(1) Timing measuring is based on the 50% point of all signals.

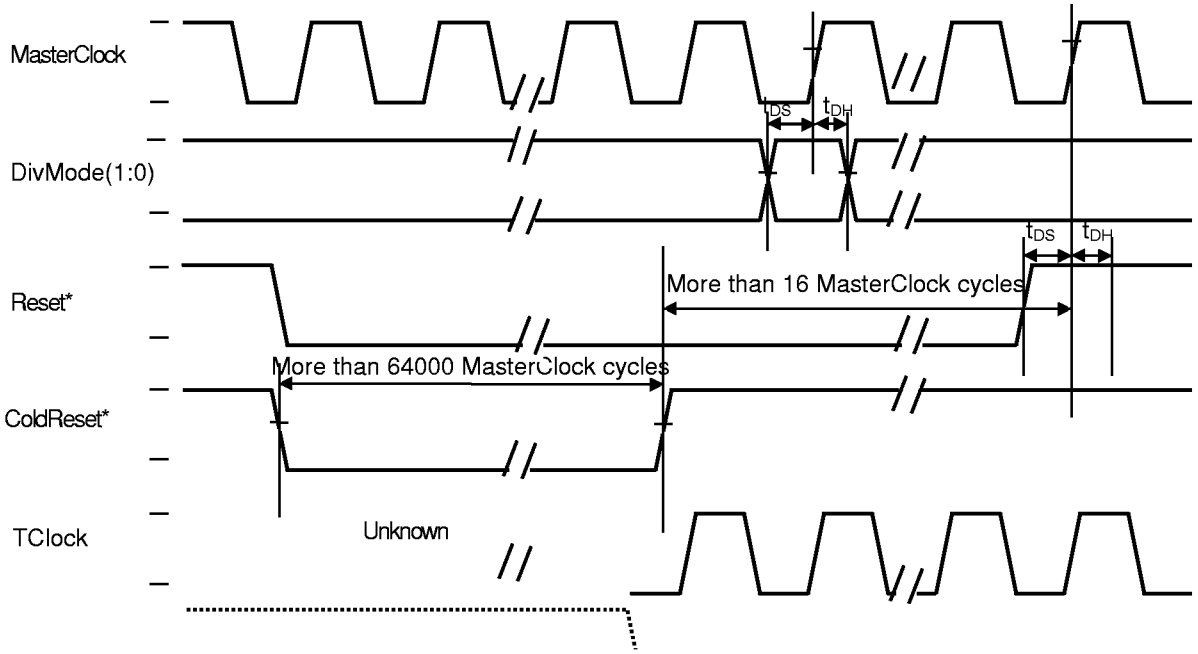
5.5.3 PClock to SClock DIVISOR of 2



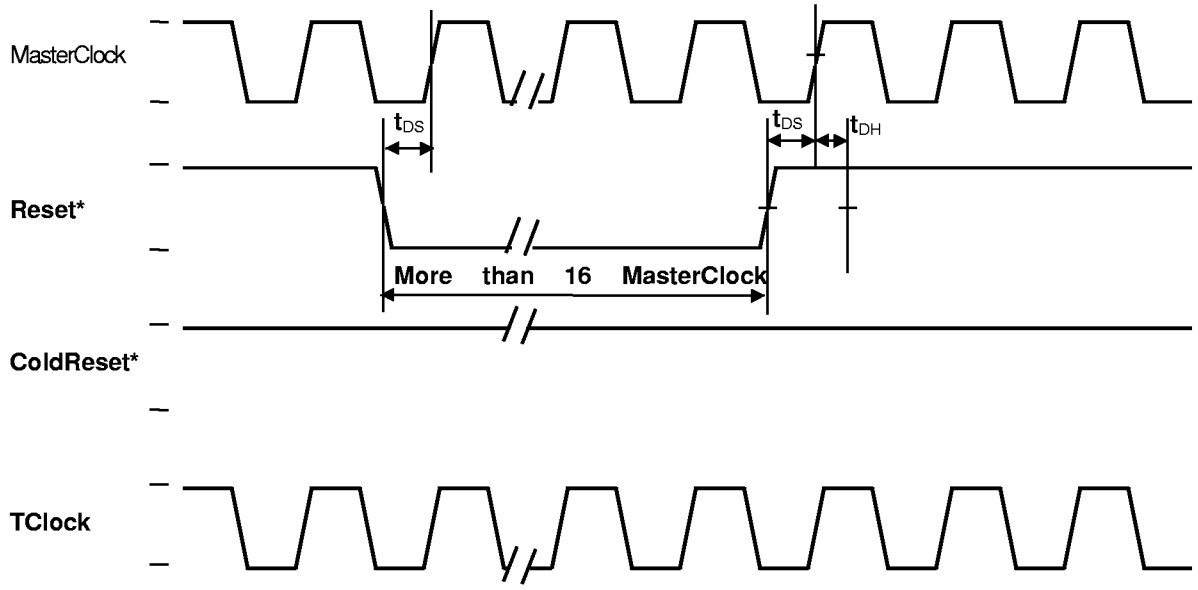
5.5.4 SYSTEM INTERFACE TIMING



5.5.5 COLD RESET TIMING



5.5.6 WARM RESET TIMING



6. PACKAGE DIMENSION

QFP120-P-2828-0.80A UNIT : mm