MAR 2 6 1992

ISD520 Tapeless Answering Machine Device

FEATURES

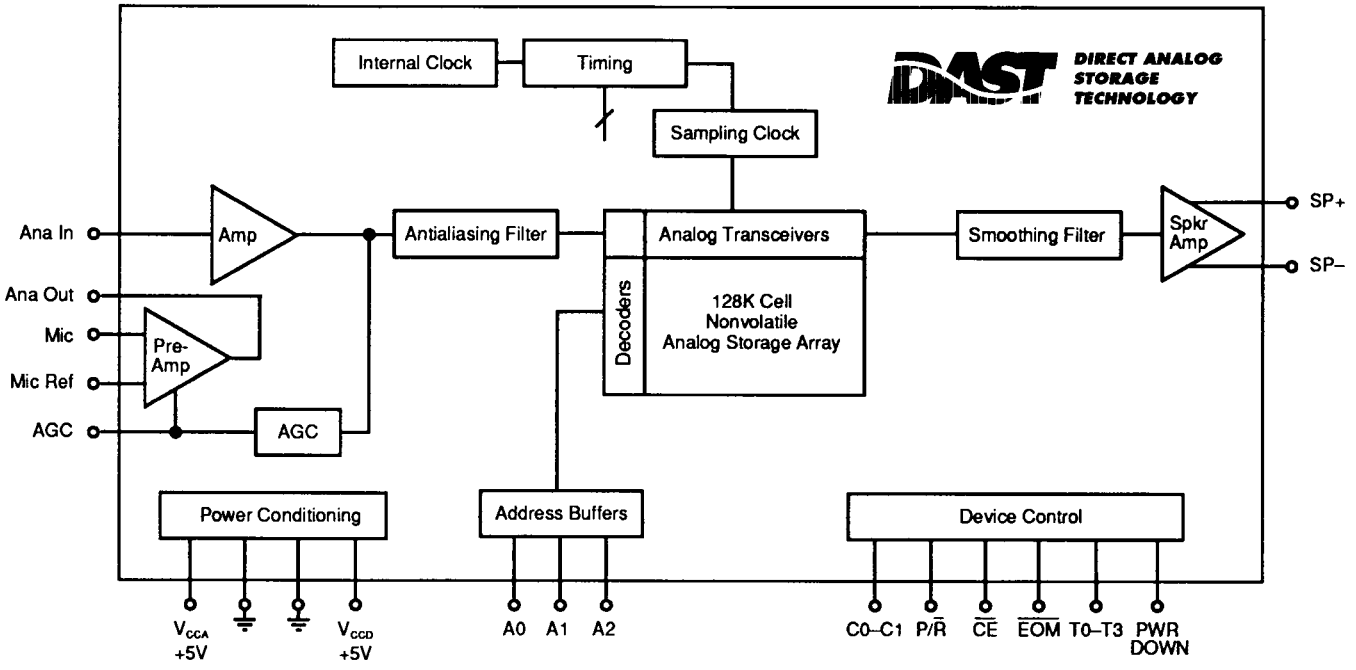
- **Natural, high-quality playback suitable for voice, music, and tones**
- **Single-chip voice record and playback OGM device**
  - Direct analog storage technology
  - Microphone preamplifier
  - Automatic gain control
  - Antialiasing and smoothing filters
  - Speaker amplifier
- **Eliminates digital memory, data converters, modulators, and battery back-up circuits**
- **Easy to use; programming and development system not required**
- **Flexible record and playback control options**
- **Nonvolatile EEPROM technology—zero power storage and 10K record cycles**
- **10-year voice retention**
- **Power down mode for lowest power consumption**
- **Single 5-volt power supply**
- **Five addressable messages**
- **Significantly reduced EMI generation and high immunity to external EMI**

GENERAL DESCRIPTION

The ISD520 is a single-chip Tapeless Answering Machine Device that provides all the circuits required to record and playback outgoing messages for a telephone answering machine. This compact, easy-to-use, nonvolatile, low-power solution has been made possible by ISD's patented DAST™ technology—the breakthrough in *Direct Analog Storage Technology* in EEPROM. DAST technology offers storage density that is eight times greater than digital memory. The DAST nonvolatile array consists of 128K cells—the equivalent of 1M bits of digital storage.

The ISD520 eliminates the need for digital conversion, digital compression, and voice synthesis techniques that often compromise voice quality and complicate usage. The ISD520 includes signal conditioning circuits and control functions which enable a complete, high-quality recording and playback system in a single device.

ISD520 BLOCK DIAGRAM



GENERAL DESCRIPTION, *continued*

The highly integrated ISD520 contains all of the basic functions required for high-quality voice recording and playback. The noise cancelling Microphone Preamplifier and Automatic Gain Control (AGC) record both the low-volume and high-volume sounds. The AGC attack and release times are adjusted by an external resistor and capacitor. Antialiasing is performed by a continuous fifth-order Chebyshev filter which rolls off at 40dB/octave. The low corner of the passband is user-settable by two external capacitors. The devices contain their own temperature-stabilized time-based oscillator. The ISD520 drives a speaker directly through differential outputs.

The device will operate from single 5-volt power supplies or from batteries. The device also includes a power down function for applications where minimum power consumption is critical. The CMOS-based design combined with the nonvolatile storage array assures lowest possible overall power consumption. The nonvolatile storage array is based on production-proven, low-power CMOS EEPROM technology.

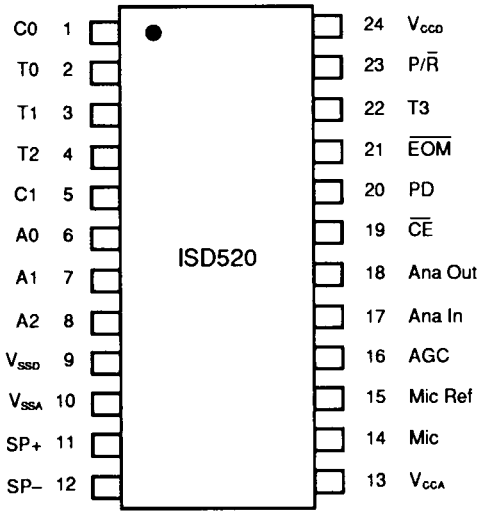
On-chip control functions make the ISD520 very easy to use in a telephone answering machine or in similar applications. Message cueing and consecutive message addressing control functions are also supported. The device may be used in applications that require little more than a few switches and a battery. The devices may also be integrated into electronic systems where digital addresses can be provided for more sophisticated message addressing and control. The ISD520 DAST arrays are organized in five segments. Addresses A0 through A2 provide access to each segment in the array for message addressing. This addressing provides the capability of accessing multiple telephone answering machine outgoing messages.

PIN NAMES

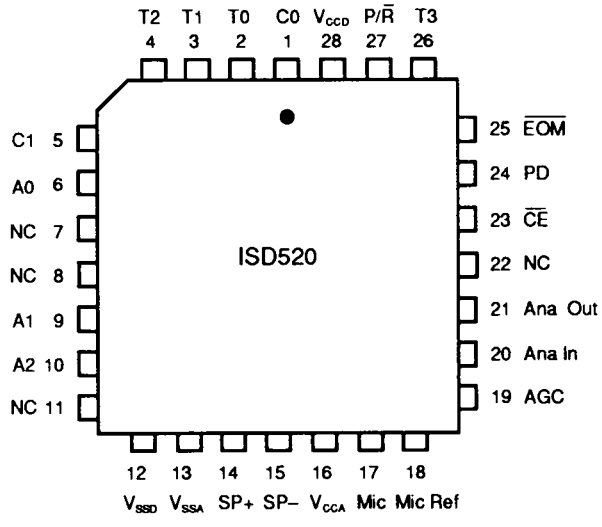
Pin	Pin # (DIP, SOIC)	Pin # (PLCC)	Name
C0–C1	1, 5	1, 5	Control Inputs
T0–T3	2, 3, 4, 22	2, 3, 4, 26	Test Pins
A0–A2	6, 7, 8	6, 9, 10	Message Address
V_{CCD}	24	28	V_{CC} Digital Power Supply
V_{CCA}	13	16	V_{CC} Analog Power Supply
V_{SSD}	9	12	V_{SS} Digital Ground
V_{SSA}	10	13	V_{SS} Analog Ground
SP+	11	14	Speaker+
SP–	12	15	Speaker–

Pin	Pin # (DIP, SOIC)	Pin # (PLCC)	Name
Mic	14	17	Microphone In
Mic Ref	15	18	Microphone Reference
PD	20	24	Power Down
P/$\overline{R}$	23	27	Playback/Record
$\overline{EOM}$	21	25	End-of-Message
$\overline{CE}$	19	23	Chip Enable
Ana Out	18	21	Analog Out
Ana In	17	20	Analog In
AGC	16	19	Automatic Gain Control

ISD520 PIN ASSIGNMENTS



DIP and SOIC



PLCC

PIN DESCRIPTION

Microphone Input (Mic)

The microphone is AC-coupled to this pin via a series capacitor. The user-selectable value of the input series capacitor (together with the 10 KΩ resistance internal to the ISD520) determines the low frequency cut-off for the ISD520 passband.

Microphone Reference (Mic Ref)

When AC-coupled to microphone ground, the noise level is significantly reduced. Ground noise is referred to the preamplifier. If this pin is not used, it must *not* be connected to any signal or voltage. It must float.

Analog Output (Ana Out)

The microphone signal is amplified and is output to the Ana Out pin. The voltage gain of the pre-amp is determined by the voltage level at the Automatic Gain Control (AGC) pin. It has a maximum gain of about 24dB for small input signal levels.

Analog In (Ana In)

An external capacitor connects Ana In to the Ana Out pin. The value of the external capacitor, together with the 2.7Ω input impedance at Ana In, can be chosen to give additional cut-off at the low frequency end of the voice passband. The Ana In pin may also be used to input alternative sources of analog signal, other than the microphone signal, through a DC-blocking capacitor.

Automatic Gain Control (AGC)

The purpose of the AGC is to dynamically adjust the preamplifier gain, and therefore extend the range of input signals which can be applied to the microphone input without distortion. The AGC considerably extends the range of recordable sounds from whispers to loud voices. Peak voltage levels at the Amplifier output are detected in the AGC circuit, and charge the external capacitor C2 on the AGC control pin. The source resistance (5K) of the internal AGC circuit and the external capacitor C2 determine the "attack" time of the gain control, "Release" time is determined by the RC time constant of the external resistor (R2) and capacitor (C2). For AGC voltages of 1.5V and below, the preamplifier is at its maximum gain of 24dB. Reduction in preamplifier gain occurs for voltages of approximately 1.8V.

Speaker Outputs (SP+ / SP–)

The SP+ and SP– pins provide direct drive for loudspeakers with impedances as low as 16 ohms. A single output may be used, but, for direct drive of loudspeakers, the two opposite polarity outputs give an improvement in output power of up to four times. When SP+ and SP– connections are used, a speaker coupling capacitor is not required. A single-ended connection will require an AC coupling capacitor between the SP pin and the speaker. The speaker outputs are held at V_{SSA} during recording and Power Down.

Power Down (PD)

The Power Down pin is taken High (when not recording or playing back) to provide a very low power mode to the ISD520. When $\overline{EOM}$ goes low for memory overflow condition, PD must be brought High to reset addresses.

Chip Enable ($\overline{CE}$)

The Chip Enable pin is taken low to enable all playback and record operations. The address inputs (A0–A2) and the playback/record input are latched into the ISD520 by this falling edge.

Playback/Record (P/$\overline{R}$)

The state of the P/$\overline{R}$ is latched into the ISD520 on the falling edge of $\overline{CE}$. A High level selects a playback cycle, while a Low level selects a record cycle. During record, the playback circuits and speaker output amplifiers are powered down, and the SP+ and SP– outputs are held at V_{SSA}. During playback, the internal record and analog inputs are disabled.

In playback mode, it is only necessary to supply the starting message address. The ISD520 will playback until an End-of-Message is encountered. In record mode, the start address determines the beginning of the message. The ISD520 records until $\overline{CE}$ is brought High or until an overflow is detected. Messages shorter than 4 seconds use only part of the segment; messages more than 4 seconds carry over into the next segment.

Address Inputs (A0-A2)

The Address Inputs provide two functions in the ISD520:

(1) Message address (C0 AND C1 = Low)

(2) ISD520 Operational Mode Options (C0 OR C1 = High)

Operational mode options are shown in Table 1 (Page 4).

Control Inputs (C0, C1)

The control pins are used to select alternative operational modes. If A1 and A2 are both high, then C0 and C1 are set to the appropriate levels, as described in the Operational Modes Table on Page 4. If either A1 or A2 is low, then both C0 and C1 should also be set to a low level.

Test (T0–T3)

The test pins are used during testing prior to product shipment. These pins are not used in system operation. The test pins must be tied Low in system operation.

PIN DESCRIPTION, *continued*

End of Message ($\overline{EOM}$)

A digital End-of-Message marker is automatically inserted in an internal nonvolatile register at the end of each recorded message. The $\overline{EOM}$ output goes Low under the following conditions:

- At end of each message
- Message overflow (device full)

The ISD520 has an internal V_{CC} detect circuit to protect against inadvertent recordings. When V_{CCD} drops below 3.5V, $\overline{EOM}$ is forced Low and the device is placed in playback mode. The $\overline{EOM}$ marker provides a convenient handshake signal for a processor. The $\overline{EOM}$ function also facilitates cascading.

V_{CCA} and V_{CCD} (+5.0 Volts)

Analog and digital circuits internal to the ISD520 use separate power buses to minimize noise on the chip. These +5 Volt buses are brought out to separate pins on the package and should be tied together as close to the supply as possible. It is important that the +5 Volt supply be decoupled as close as possible to the package.

V_{SSA} and V_{SSD} (Ground)

Similar to V_{CCA} and V_{CCD}, the analog and digital circuits internal to the ISD520 use separate ground buses to minimize noise. These pins should be tied together as close as possible to the device.

OPERATIONAL MODES

The address pins (A0–A2) can be used together with the control pins (C0, C1) to select alternative operational modes. These operational modes are selected by setting both A1 and A2 to a high level. The appropriate level must also be applied to C0 and C1, as described in the Operational Modes Table.

(1) Consecutive Addressing

Consecutive addressing allows for recording and playback of consecutive messages without the need for direct addressing or any other kind of message management. During recording, each time that $\overline{CE}$ is taken Low, a message is recorded at the next position in memory. When $\overline{CE}$ is taken High again, an End-of-Message marker is written to indicate the position of the End of the message. In this fashion, a string of messages is recorded, each one placed immediately after the previous one.

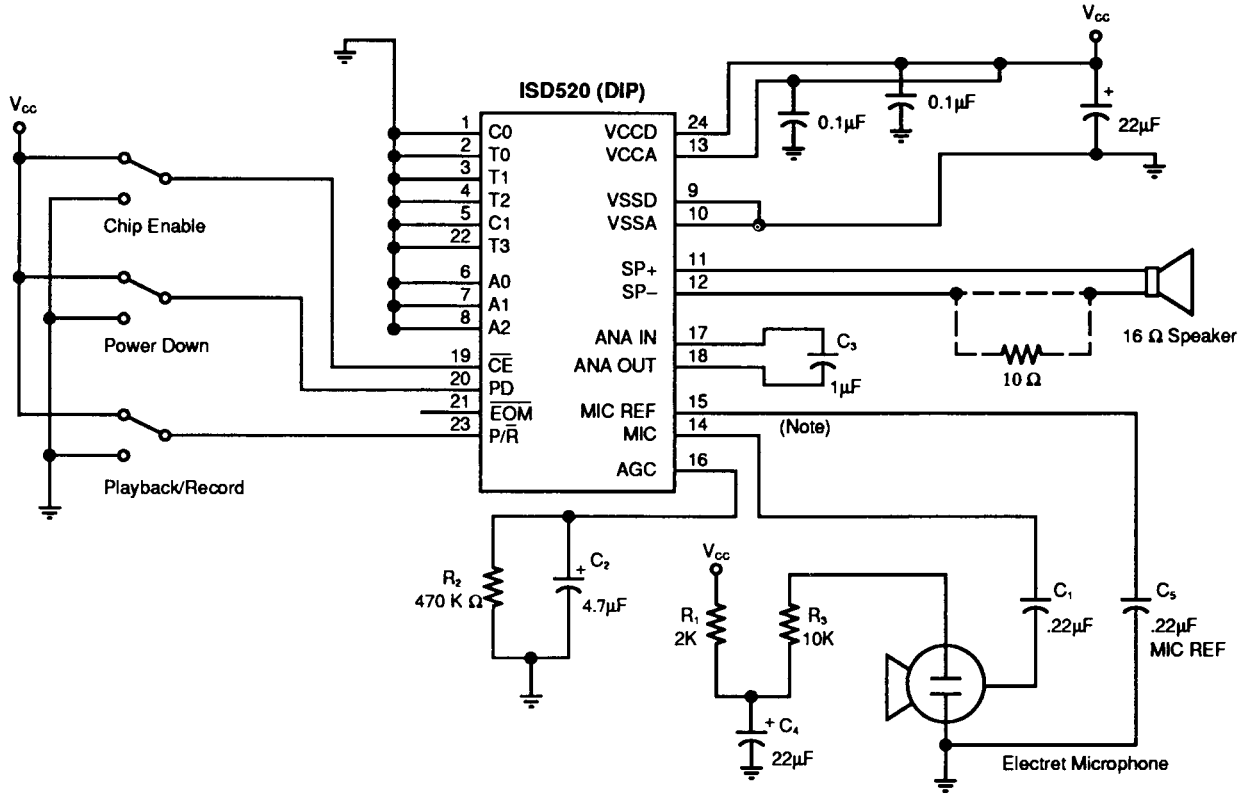
(2) Message Cueing (Available Q3, 1992)

Message cueing allows the user to skip through messages. Each time $\overline{CE}$ memory is pulsed Low with the address inputs set to this mode, the internal message pointer skips forward until it encounters an end-of-message marker and then stops. By providing a certain number of pulses to the $\overline{CE}$ pin in message cueing mode and then changing to consecutive addressing mode, the user can select and then record or playback a desired message. Message cueing should not be used in Record mode.

Table 1. Operational Modes—Options

A0	A1	A2	C0	C1	Mode
0	0	0	0	0	Addressing the 1st 4-second segment
1	0	0	0	0	Addressing the 2nd 4-second segment
0	1	0	0	0	Addressing the 3rd 4-second segment
1	1	0	0	0	Addressing the 4th 4-second segment
0	0	1	0	0	Addressing the 5th 4-second segment
1	0	1	X	X	Invalid code
0	1	1	0	1	Consecutive addressing
0	1	1	1	1	Message cueing

APPLICATION EXAMPLE— DESIGN SCHEMATIC



Note: If desired, this pin may be left unconnected (microphone preamplifier noise will be higher). In this case, pin 15 must not be tied to any other signal or voltage.

APPLICATION EXAMPLE— BASIC DEVICE CONTROL

Control Step	Function	Action
1	Power-up chip and select record/playback mode	1. PD = Low 2. P/$\overline{R}$ = As desired
2	Set message address for record/playback	Set addresses A0–A2
3	Begin record/playback	$\overline{CE}$ = Low
4	End cycle	$\overline{CE}$ = High

APPLICATION EXAMPLE— PASSIVE COMPONENT FUNCTIONS

Part	Function	Comments
R1	Microphone power supply decoupling network	Reduces power supply noise
R2	Release time constant	Sets release time for AGC
R3	Microphone biasing resistor	Provides biasing for microphone operation
C1	Microphone DC-blocking capacitor. Low frequency cutoff	Decouples microphone bias from chip. Provides single-pole low frequency cutoff
C2	Attack/Release time constant	Sets attack/release time for AGC
C3	Low frequency cutoff capacitor	Provides additional pole for low frequency cutoff
C4	Microphone power supply decoupling network	Reduces power supply noise
C5	Noise reduction	Reduces input noise

ABSOLUTE MAXIMUM RATINGS (ISD520)

Condition	Value
Operating Temperature	0° C to +70° C
Temperature under bias*	–65° C to +125° C
Storage temperature range*	–65° C to +150° C
Voltage applied to any pin*	(V_{SS} –0.3 V) to (V_{CC} + 0.3 V)
Voltage applied to any pin (input current limited to ± 20 mA)*	(V_{SS} –1.0 V) to (V_{CC} + 1.0 V)
Lead temperature (soldering –10 seconds)*	300° C
$V_{CC} - V_{SS}$	-0.3 V to +7.0 V

* Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings denoted by (*) may affect device reliability. Stress ratings denoted by (*) do not imply functional operation at these conditions.

DC PARAMETERS (ISD520)

Operating Conditions T_A = 0° C to 70° C (Note #4); V_{CC} (Note #5) = 5.0 V ± 10%; V_{SS} (Note #6) = 0 V; Unless otherwise noted

Symbol	Parameters	Min	Typ(0)	Max	Units	Conditions
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.4			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –1.6 mA
V_{OH1}	Output High Voltage	V_{CC} –0.4			V	I_{OH} = –10 µA
I_{CC}(7)	V_{CC} Current (Operating)			25	mA	R_{EXT} = ∞
I_{SB}(7)	V_{CC} Current (Standby)		1	10	µA	
I_{IL}	Input Leakage Current			±1	µA	
R_{EXT}	Output Load Impedance	16			Ω	Speaker Load
R_{MIC}	Pre-Amp In Input Resistance Pins 14 and 15		10		KΩ	
R_{AUX}	Aux Input Resistance		10		KΩ	
R_{ANA} In	Ana In Input Resistance		2.7		KΩ	
A_{PRE1}	Pre-Amp Gain 1		24		dB	AGC = 0.0 V
A_{PRE2}	Pre-Amp Gain 2			5	dB	AGC = 2.5 V
A_{ARP}	Ana In to SP+/–		22		dB	
R_{AGC}	AGC Output Resistance		5		KΩ	
I_{PREH}	Pre-Amp Out Source		100		µA	@V_{OUT} = 1.0 V
I_{PREL}	Pre-amp In Sink		100		µA	@V_{OUT} = 2.0 V

AC PARAMETERS (ISD520)

Operating Conditions T_A = 0° C to 70° C (Note #4); V_{CC} (Note #5) = 5.0 V ± 10%; V_{SS} (Note #6) = 0 V; Unless otherwise noted

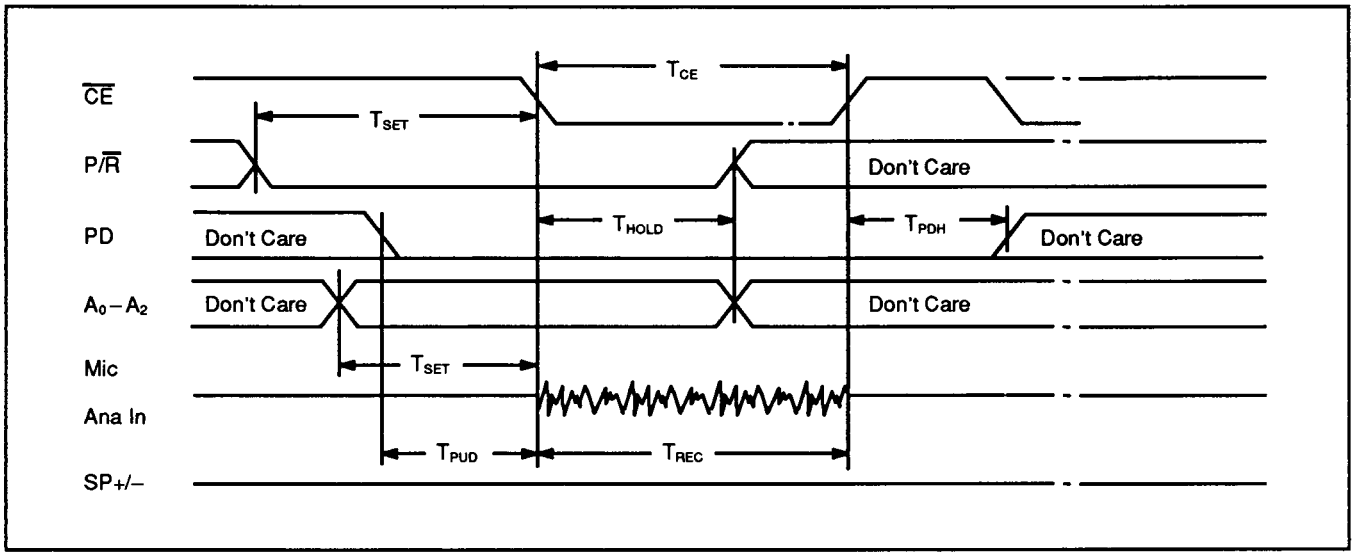
Symbol	Characteristics	Min	Typ(9)	Max	Units	Conditions
FS	Internal Clock Sampling Frequency		6.4		KHz	
BW	Passband (3)		2700		Hz	
THD	Total Harmonic Distortion		2		%	@ 1KHz
P_{OUT}	Speaker Output Power			50	mW	R_{EXT} = 16Ω
V_{OUT}	Voltage across speaker pins			2.5	Vp-p	R_{EXT} = 600Ω
V_{IN1}	Mic input voltage			20	mv	Peak – Peak (2)
V_{IN2}	Ana In input voltage			50	mv	Peak – Peak
T_{SET}	Control/Address set-up	1			msec	
T_{HOLD}	Control/Address hold	1			msec	
T_{CE}	$\overline{CE}$ Record time	100			nsec	
T_{PUD}	Power up delay	31.25			msec	
T_{PDH}	Power down hold	0			nsec	
T_{REC}	Record time		20		sec	
T_{PLAY}	Playback time		20		sec	
T_{EOM}	$\overline{EOM}$ pulse width		15.6		msec	

Notes:

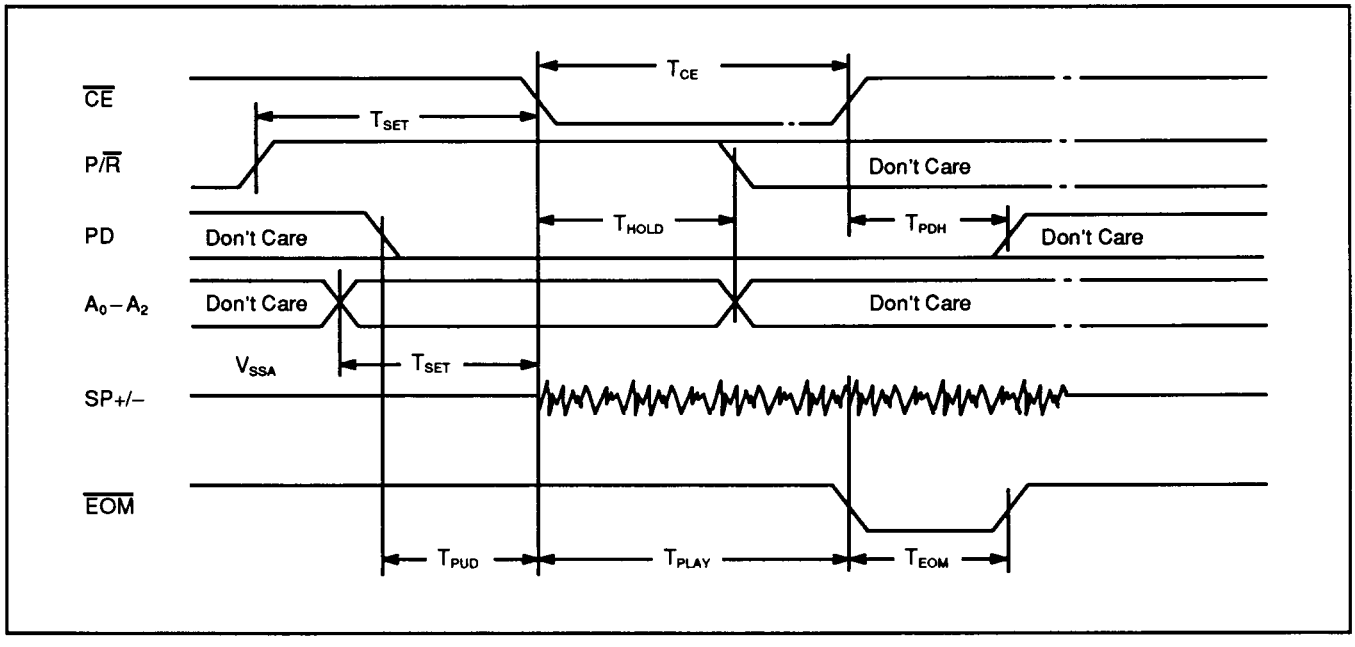
1. Typical values @ T_A = 25° C and nominal voltages
2. With 12 KΩ series resistor at Ana In
3. Low frequency cutoff depends on value of external capacitors (see Pin Descriptions).
4. Case temperature
5. $V_{CC} = V_{CCD} = V_{CCA}$
6. $V_{SS} = V_{SSA} = V_{SSD}$
7. V_{CCA} and V_{CCD} connected together

TIMING DIAGRAMS

RECORD

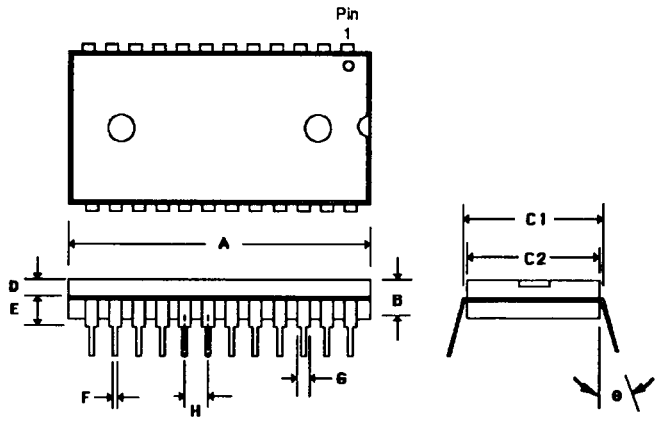


PLAYBACK



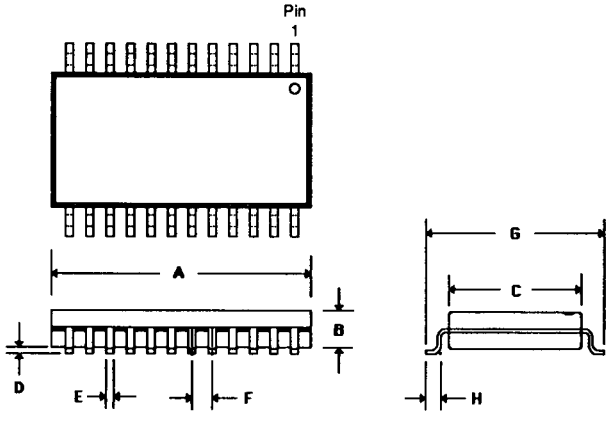
PACKAGE DIAGRAMS

24-lead Plastic Dual In-line Package (DIP) Type P



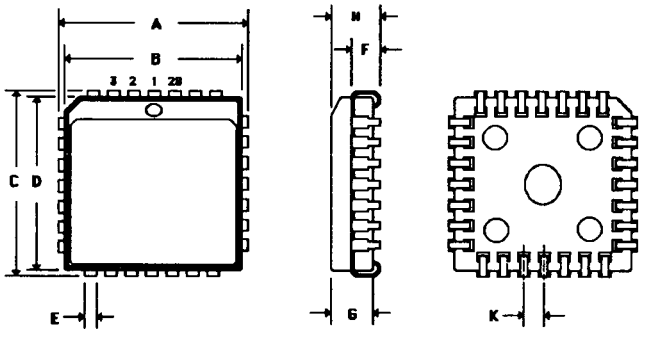
	INCHES			MILLIMETERS		
	MIN	NOM	MAX.	MIN	NOM	MAX.
A	1.245	1.250	1.255	31.62	31.75	31.88
B		.150			3.89	
C1	.600		.625	15.24		15.88
C2	.530	.540	.550	13.46	13.72	13.97
D	1.25	1.30	1.35	2.92	3.05	3.18
E	.125	.130	.135	3.18		3.43
F	.015	.018	.022	0.38	0.46	0.56
G	.055	.060	.065	1.40	1.52	1.65
H		.100			2.54	
θ	0°	7°	15°	0°	7°	15°

24-lead Plastic Small Outline Package (SOIC) Type G



	INCHES			MILLIMETERS		
	MIN	NOM	MAX.	MIN	NOM	MAX.
A	.606	.614	.618	15.39	15.60	15.70
B	.086	.088	.090	2.18	2.24	2.29
C	.340	.346	.350	8.64	8.79	8.89
D	.004	.007	.010	.102	.178	.254
E	.014	.016	.020	.360	.410	.480
F		.050			1.27	
G	.463	.470	.477	11.76	12.00	12.12
H	.020	.031	.042	.510	.790	1.07

28-lead Plastic Leadless Chip Carrier (PLCC) Type J



	INCHES			MILLIMETERS		
	MIN	NOM	MAX.	MIN	NOM	MAX.
A	.485	.490	.495	12.32	12.45	12.57
B	.450	.452	.454	11.43	11.48	11.53
C	.485	.490	.495	12.32	12.45	12.57
D	.450	.452	.454	11.43	11.48	11.53
E	.026		.032			
F	.100	.101	.110	2.54	2.56	2.79
G	.148	.152	.156	3.76	3.86	3.96
H	.165	.172	.180	4.19	4.37	4.57
K		.050				

Unless otherwise specified:
all tolerances are ± .007 inches

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Information contained in this ISD520 product specification supersedes all data for the ISD520 products published by ISD before February, 1992.

ORDERING INFORMATION

When placing an order for the ISD520 devices, please refer to the following model numbers:

Model Number	Record/Playback Duration (Seconds)	Description
ISD520P	20	24-pin plastic dual in-line package
ISD520J	20	28-lead plastic leadless chip carrier (PLCC)
ISD520G	20	24-lead small outline integrated circuit (SOIC)
ISD520X	20	Bare unpackaged die

EDN's
Innovation of the Year Award 1991

GRAND WINNER

ISD1000 Analog Storage ICs

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ISD™ *Information Storage Devices, Inc.*

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