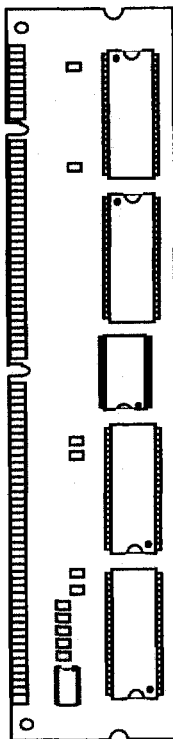




**Description**

The GMM7642000CS/SG is an 2M x 64 bits Dynamic RAM MODULE which is assembled 8 pieces of 1M x 16bit DRAMs in 42 pin SOJ package, two 16bit driver ICs in 48pin TSSOP package and one 8bit driver IC in 20 pin TSSOP package mounted on a 168 pin printed circuit board with decoupling capacitors. The GMM7642000CS/SG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size. The GMM7642000CS/SG provides common data inputs and outputs.

- GMM7642000CS/SG (Double Side)



**Features**

- 168 pins Dual In-Line Package
  - GMM7642000CS : Solder plating
  - GMM7642000CSG : Gold plating
- Fast Page Mode Capability
- Single Power Supply
- Fast Access Time & Cycle Time

(Unit: ns)

	t <sub>TRAC</sub>	t <sub>CAC</sub>	t <sub>TRC</sub>	t <sub>PC</sub>
GMM7642000CS/SG-6	60	20	110	40
GMM7642000CS/SG-7	70	25	130	45

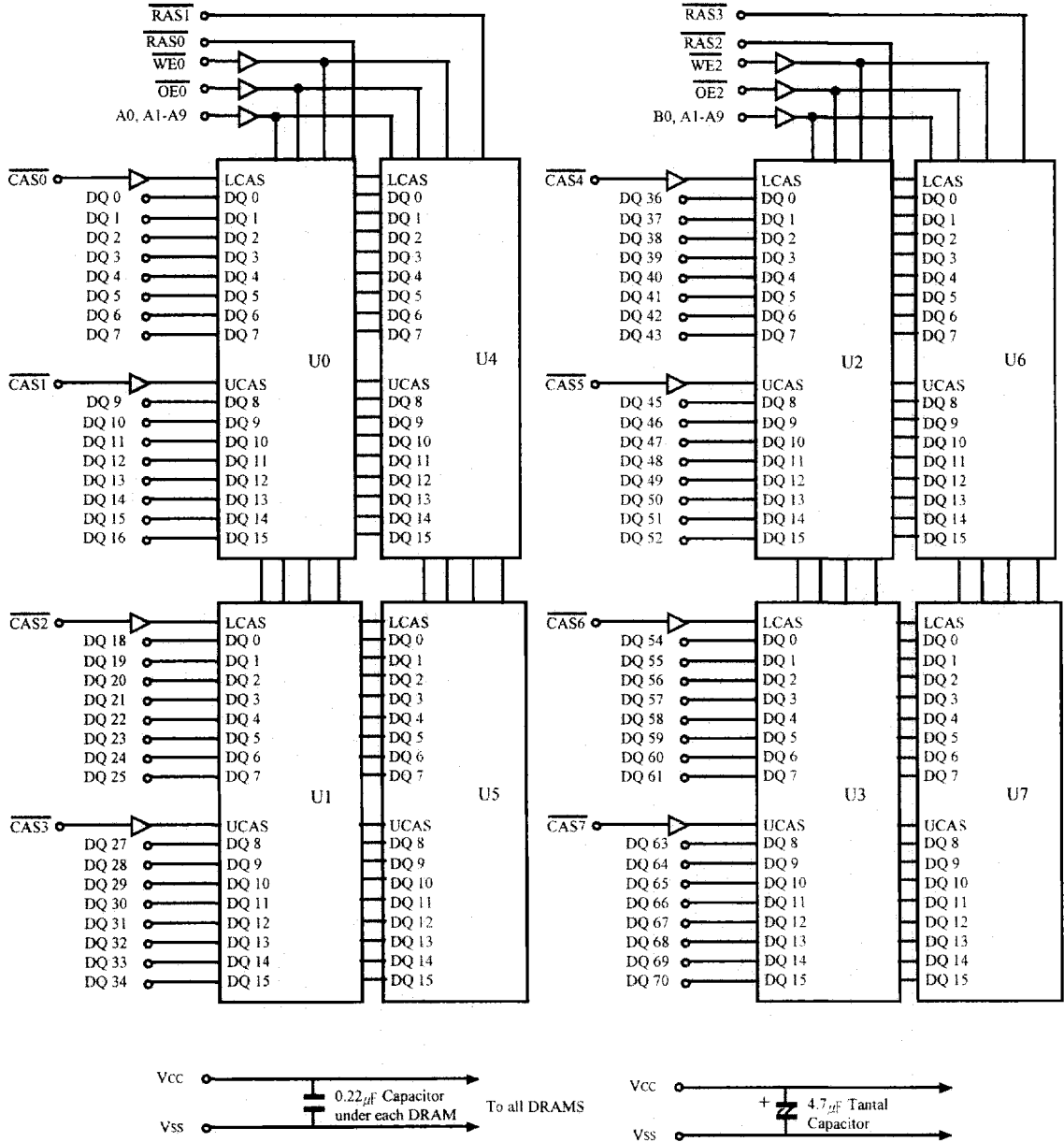
- Low Power
  - Active : 4,345/3,905 mW (MAX)
  - Standby : 539 mW (CMOS level : MAX)
- RAS Only Refresh, CAS before RAS Refresh, Hidden Refresh Capability
- All inputs and outputs TTL Compatible
- 1024 Refresh Cycles/16ms

**Pin Configuration (Top View)**

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V <sub>SS</sub>	29	/CAS <sub>2</sub>	57	DQ <sub>22</sub>	85	V <sub>SS</sub>	113	/CAS <sub>3</sub>	141	DQ <sub>58</sub>
2	DQ <sub>0</sub>	30	/RAS <sub>0</sub>	58	DQ <sub>23</sub>	86	DQ <sub>36</sub>	114	/RAS <sub>1</sub>	142	DQ <sub>59</sub>
3	DQ <sub>1</sub>	31	/OE <sub>0</sub>	59	V <sub>CC</sub>	87	DQ <sub>37</sub>	115	RFU	143	V <sub>CC</sub>
4	DQ <sub>2</sub>	32	V <sub>SS</sub>	60	DQ <sub>24</sub>	88	DQ <sub>38</sub>	116	V <sub>SS</sub>	144	DQ <sub>60</sub>
5	DQ <sub>3</sub>	33	A <sub>0</sub>	61	RFU	89	DQ <sub>39</sub>	117	A <sub>1</sub>	145	RFU
6	V <sub>CC</sub>	34	A <sub>2</sub>	62	RFU	90	V <sub>CC</sub>	118	A <sub>3</sub>	146	RFU
7	DQ <sub>4</sub>	35	A <sub>4</sub>	63	RFU	91	DQ <sub>40</sub>	119	A <sub>5</sub>	147	RFU
8	DQ <sub>5</sub>	36	A <sub>6</sub>	64	RFU	92	DQ <sub>41</sub>	120	A <sub>7</sub>	148	RFU
9	DQ <sub>6</sub>	37	A <sub>8</sub>	65	DQ <sub>25</sub>	93	DQ <sub>42</sub>	121	A <sub>9</sub>	149	DQ <sub>61</sub>
10	DQ <sub>7</sub>	38	A <sub>10*</sub>	66	RSVD	94	DQ <sub>43</sub>	122	A <sub>11*</sub>	150	RSVD
11	RSVD	39	A <sub>12*</sub>	67	DQ <sub>27</sub>	95	RSVD	123	A <sub>13*</sub>	151	DQ <sub>63</sub>
12	V <sub>SS</sub>	40	V <sub>CC</sub>	68	V <sub>SS</sub>	96	V <sub>SS</sub>	124	V <sub>CC</sub>	152	V <sub>SS</sub>
13	DQ <sub>9</sub>	41	RFU	69	DQ <sub>28</sub>	97	DQ <sub>45</sub>	125	RFU	153	DQ <sub>64</sub>
14	DQ <sub>10</sub>	42	RFU	70	DQ <sub>29</sub>	98	DQ <sub>46</sub>	126	B <sub>0</sub>	154	DQ <sub>65</sub>
15	DQ <sub>11</sub>	43	V <sub>SS</sub>	71	DQ <sub>30</sub>	99	DQ <sub>47</sub>	127	V <sub>SS</sub>	155	DQ <sub>66</sub>
16	DQ <sub>12</sub>	44	/OE <sub>2</sub>	72	DQ <sub>31</sub>	100	DQ <sub>48</sub>	128	RFU	156	DQ <sub>67</sub>
17	DQ <sub>13</sub>	45	/RAS <sub>2</sub>	73	V <sub>CC</sub>	101	DQ <sub>49</sub>	129	/RAS <sub>3</sub>	157	V <sub>CC</sub>
18	V <sub>CC</sub>	46	/CAS <sub>4</sub>	74	DQ <sub>32</sub>	102	V <sub>CC</sub>	130	/CAS <sub>5</sub>	158	DQ <sub>68</sub>
19	DQ <sub>14</sub>	47	/CAS <sub>6</sub>	75	DQ <sub>33</sub>	103	DQ <sub>50</sub>	131	/CAS <sub>7</sub>	159	DQ <sub>69</sub>
20	DQ <sub>15</sub>	48	/WE <sub>2</sub>	76	DQ <sub>34</sub>	104	DQ <sub>51</sub>	132	/PDE	160	DQ <sub>70</sub>
21	DQ <sub>16</sub>	49	V <sub>CC</sub>	77	RSVD	105	DQ <sub>52</sub>	133	V <sub>CC</sub>	161	RSVD
22	RSVD	50	RSVD	78	V <sub>SS</sub>	106	RSVD	134	RSVD	162	V <sub>SS</sub>
23	V <sub>SS</sub>	51	RSVD	79	PD <sub>1</sub>	107	V <sub>SS</sub>	135	RSVD	163	PD <sub>2</sub>
24	RSVD	52	DQ <sub>18</sub>	80	PD <sub>3</sub>	108	RSVD	136	DQ <sub>54</sub>	164	PD <sub>4</sub>
25	RSVD	53	DQ <sub>19</sub>	81	PD <sub>5</sub>	109	RSVD	137	DQ <sub>55</sub>	165	PD <sub>6</sub>
26	V <sub>CC</sub>	54	V <sub>SS</sub>	82	PD <sub>7</sub>	110	V <sub>CC</sub>	138	V <sub>SS</sub>	166	PD <sub>8</sub>
27	/WE <sub>0</sub>	55	DQ <sub>20</sub>	83	ID <sub>0</sub>	111	RFU	139	DQ <sub>56</sub>	167	ID <sub>1</sub>
28	/CAS <sub>0</sub>	56	DQ <sub>21</sub>	84	V <sub>CC</sub>	112	/CAS <sub>1</sub>	140	DQ <sub>57</sub>	168	V <sub>CC</sub>

Note : Pins Marked \* are not used in this module.

Block Diagram



Pin	Function	Pin	Function
A0-A9, B0	Address Inputs	$\overline{\text{PDE}}$	Presence Detect Enable
DQ0-DQ70	Data Input/Output	V <sub>CC</sub>	Power (+5V)
$\overline{\text{RAS0}} - \overline{\text{RAS3}}$	Row Address Strobe	V <sub>SS</sub>	Ground
$\overline{\text{CAS0}} - \overline{\text{CAS7}}$	Column Address Strobe	NC	No Connection
$\overline{\text{WE0}}, \overline{\text{WE2}}$	Read/Write Enable	$\overline{\text{OE0}}, \overline{\text{OE2}}$	Output Enable
PD 1-8	Presence Detect	RSVD	Reserved Use
ID 0-1	ID bit	RFU	Reserved for Future Use

**Presence Detect Pins (Optional)**

Pin	60ns	70ns
PD1	1	1
PD2	0	0
PD3	1	1
PD4	0	0
PD5	0	0
PD6	1	0
PD7	1	1
PD8	1	1

Refresh Mode	
	ID1
Normal	0
Self-Refresh	1

\* 0 : V<sub>SS</sub>  
 1 : NC or V<sub>CC</sub>

**Absolute Maximum Ratings\***

Symbol	Parameter	Rating	Unit
T <sub>A</sub>	Ambient Temperature under Bias	0 ~ 70	°C
T <sub>STG</sub>	Storage Temperature (Plastic)	-55 ~ 125	°C
V <sub>IN</sub> /V <sub>OUT</sub>	Voltage on any Pin Relative to V <sub>SS</sub>	-0.5 ~ 7.0	V
V <sub>CC</sub>	Power Supply Voltage	-0.5 ~ 7.0	V
I <sub>OUT</sub>	Short Circuit Output Current	50	mA
P <sub>D</sub>	Power Dissipation	5	W

\*Note: 1. Stress greater than above absolute Maximum Ratings may cause permanent damage to the device.

**Recommended DC Operating Conditions (T<sub>A</sub> = 0 ~ 70°C)**

Symbol	Parameter	Min	Typ	Max	Unit	Note
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V	1
V <sub>IH</sub>	Input High Voltage	2.4	-	6.5	V	1
V <sub>IL</sub>	Input Low Voltage	0	-	0.8	V	1

\*Note: 1. All voltages referenced to V<sub>SS</sub>.

DC Electrical Characteristics ( $V_{CC} = 5V \pm 10\%$ ,  $T_A = 0 \sim 70^\circ C$ )

Symbol	Parameter	Min	Max	Unit	Note	
$V_{OH}$	Output Level Output $\overline{M}$ Level Voltage ( $I_{OUT} = -5mA$ )	2.4	$V_{CC}$	V		
$V_{OL}$	Output Level Output $\overline{M}$ Level Voltage ( $I_{OUT} = 4.2mA$ )	0	0.4	V		
$I_{CC1}$	Operating Current Average Power Supply Operating Current ( $\overline{RAS}$ , $\overline{CAS}$ , Address Cycling: $t_{RC} = t_{RC \min}$ )	60ns	-	790	mA	1, 2
		70ns	-	710		
$I_{CC2}$	Standby Current (TTL) Power Supply Standby Current ( $\overline{RAS}$ , $\overline{CAS} = V_{IH}$ )	-	106	mA		
$I_{CC3}$	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Mode ( $\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$ , $t_{RC} = t_{RC \min}$ )	60ns	-	790	mA	2
		70ns	-	710		
$I_{CC4}$	Fast Page Mode Current Average Power Supply Current Fast Page Mode ( $\overline{RAS} = V_{IL}$ , $\overline{CAS}$ , Address Cycling: $t_{RC} = t_{RC \min}$ )	60ns	-	790	mA	1, 3
		70ns	-	710		
$I_{CC5}$	Standby Current (CMOS) Power Supply Standby Current ( $\overline{RAS}$ , $\overline{CAS} \geq V_{CC} - 0.2V$ )	-	98	mA		
$I_{CC6}$	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current ( $t_{RC} = t_{RC \min}$ )	60ns	-	790	mA	
		70ns	-	710		
$I_{CC7}$	Standby Current $\overline{RAS} = V_{IH}$ $\overline{CAS} = V_{IL}$ $D_{OUT} = \text{Enable}$	-	130	mA	1	
$I_{IL1}$	Input Leakage Current Any Input ( $0V \leq V_{IN} \leq 7V$ ) All Other Pins Not Under Test = 0V	-80	80	$\mu A$		
$I_{OL2}$	Output Leakage Current ( $D_{OUT}$ is Disabled, $0V \leq V_{OUT} \leq 7V$ )	-10	10	$\mu A$		

Note: 1.  $I_{CC}$  depends on output load condition when the device is selected.  $I_{CC}(\max)$  is specified at the output open condition.

2. Address can be changed once or less while  $\overline{RAS} = V_{IL}$ .

3. Address can be changed once or less while  $\overline{CAS} = V_{IH}$ .

**Capacitance** ( $V_{CC} = 5V \pm 10\%$ ,  $T_A = 25^\circ C$ ,  $f = 1MHz$ )

Symbol	Parameter	Min	Max	Unit	Note
C <sub>11</sub>	Input Capacitance (A0~A9, B0)	-	20	pF	1
C <sub>12</sub>	Input Capacitance ( $\overline{WE}0, \overline{WE}2, \overline{OE}0, \overline{OE}2$ )	-	20	pF	1, 2
C <sub>13</sub>	Input Capacitance ( $\overline{RAS}0 \sim \overline{RAS}3$ )	-	35	pF	1, 2
C <sub>14</sub>	Input Capacitance ( $\overline{CAS}0 \sim \overline{CAS}7$ )	-	20	pF	1, 2
C <sub>10</sub>	I/O Capacitance (DQ0~DQ70)	-	20	pF	1, 2

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.  
 2.  $\overline{CAS} = V_{IH}$  to disable DOUT.

**AC Electrical Characteristics** ( $V_{CC} = 5V \pm 10\%$ ,  $T_A = 0 \sim 70^\circ C$ , Notes 1, 15)

The GMM7642000CS/SG writes data only in early write cycle ( $twcs \geq twcs(min)$ ).  
 Delayed write cycle is not available because of I/O common.

**Read, Write and Refresh Cycle (Common Parameters)**

Symbol	Parameter	GMM7642000 CS/SG-6		GMM7642000 CS/SG-7		Unit	Note
		Min	Max	Min	Max		
t <sub>RC</sub>	Random Read or Write Cycle Time	110	-	130	-	ns	
t <sub>RP</sub>	$\overline{RAS}$ Precharge Time	40	-	50	-	ns	
t <sub>CP</sub>	$\overline{CAS}$ Precharge Time	10	-	10	-	ns	
t <sub>RAS</sub>	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	ns	
t <sub>CAS</sub>	$\overline{CAS}$ Pulse Width	15	10,000	18	10,000	ns	
t <sub>ASR</sub>	Row Address Setup Time	5	-	5	-	ns	
t <sub>RAH</sub>	Row Address Hold Time	10	-	10	-	ns	
t <sub>ASC</sub>	Column Address Setup Time	0	-	0	-	ns	
t <sub>CAH</sub>	Column Address Hold Time	10	-	15	-	ns	
t <sub>RCD</sub>	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	45	ns	9
t <sub>RAD</sub>	$\overline{RAS}$ to Column Address Delay Time	15	25	15	30	ns	10
t <sub>RSH</sub>	$\overline{RAS}$ Hold Time	20	-	23	-	ns	
t <sub>CSH</sub>	$\overline{CAS}$ Hold Time	60	-	70	-	ns	
t <sub>CRP</sub>	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	ns	
t <sub>ODD</sub>	$\overline{OE}$ to D <sub>IN</sub> Delay Time	20	-	23	-	ns	
t <sub>DZO</sub>	$\overline{OE}$ Delay Time from D <sub>IN</sub>	0	-	0	-	ns	
t <sub>DZC</sub>	$\overline{CAS}$ Set-up Time from D <sub>IN</sub>	0	-	0	-	ns	
t <sub>T</sub>	Transition Time (Rise and Fall)	3	50	3	50	ns	8
t <sub>REF</sub>	Refresh Period ( 1024 Cycles )	-	16	-	16	ms	

Read Cycle

Symbol	Parameter	GMM7642000 CS/SG-6		GMM7642000 CS/SG-7		Unit	Note
		Min	Max	Min	Max		
t <sub>RAC</sub>	Access Time from $\overline{\text{RAS}}$	-	60	-	70	ns	2, 3
t <sub>CAC</sub>	Access Time from $\overline{\text{CAS}}$	-	20	-	25	ns	3, 4
t <sub>AA</sub>	Access Time from Column Address	-	35	-	40	ns	3, 5
t <sub>OAC</sub>	Access Time from $\overline{\text{OE}}$	-	20	-	23	ns	3
t <sub>RCS</sub>	Read Command Setup Time	0	-	0	-	ns	
t <sub>RCH</sub>	Read Command Hold Time to $\overline{\text{CAS}}$	0	-	0	-	ns	6
t <sub>RRH</sub>	Read Command Hold Time to $\overline{\text{RAS}}$	0	-	0	-	ns	6
t <sub>RAL</sub>	Column Address to $\overline{\text{RAS}}$ Lead Time	35	-	40	-	ns	
t <sub>OFF</sub>	Output Buffer Turn-off Time	-	20	-	20	ns	7

Write Cycle

Symbol	Parameter	GMM7642000 CS/SG-6		GMM7642000 CS/SG-7		Unit	Note
		Min	Max	Min	Max		
t <sub>WCS</sub>	Write Command Setup Time	0	-	0	-	ns	11
t <sub>WCH</sub>	Write Command Hold Time	10	-	13	-	ns	
t <sub>WP</sub>	Write Command Pulse Width	10	-	10	-	ns	
t <sub>RWL</sub>	Write Command to $\overline{\text{RAS}}$ Lead Time	20	-	23	-	ns	
t <sub>CWL</sub>	Write Command to $\overline{\text{CAS}}$ Lead Time	15	-	18	-	ns	
t <sub>DS</sub>	Data-in Setup Time	0	-	0	-	ns	12
t <sub>DH</sub>	Data-in Hold Time	15	-	18	-	ns	12

**Refresh Cycle**

Symbol	Parameter	GMM7642000 CS/SG-6		GMM7642000 CS/SG-7		Unit	Note
		Min	Max	Min	Max		
tCSR	$\overline{\text{CAS}}$ Set-up Time ( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)	10	-	10	-	ns	
tCHR	$\overline{\text{CAS}}$ Hold Time ( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)	10	-	10	-	ns	
tRPC	$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Hold Time	0	-	0	-	ns	

**Fast Page Mode Cycle**

Symbol	Parameter	GMM7642000 CS/SG-6		GMM7642000 CS/SG-7		Unit	Note
		Min	Max	Min	Max		
tPC	Fast Page Mode Cycle Time	40	-	45	-	ns	
tRASP	Fast Page Mode $\overline{\text{RAS}}$ Pulse Width	-	100,000	-	100,000	ns	13
tACP	Access Time from $\overline{\text{CAS}}$ Precharge	-	40	-	45	ns	14
tRHCP	$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	40	-	45		ns	
tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	85	-	96	-	ns	

**Notes:**

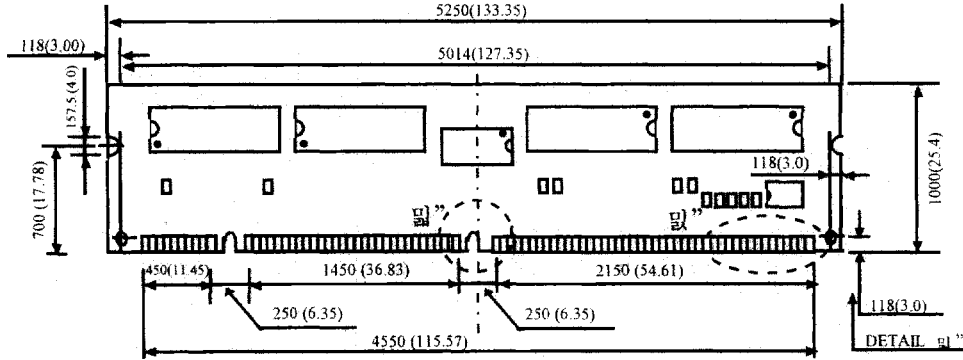
1. AC measurements assume  $t_T = 5\text{ns}$ .
2. Assumes that  $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$  and  $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$ . If  $t_{\text{RCD}}$  or  $t_{\text{RAD}}$  is greater than the maximum recommended value shown in this table,  $t_{\text{RAC}}$  exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that  $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$  and  $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$ .
5. Assumes that  $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$  and  $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max})$ .
6. Either  $t_{\text{RCH}}$  or  $t_{\text{RRH}}$  must be satisfied for a read cycles.
7.  $t_{\text{OFF}}(\text{max})$  defines the time at which the outputs achieve the open circuit condition and is not referenced to output voltage levels.
8.  $V_{\text{IH}}(\text{min})$  and  $V_{\text{IL}}(\text{max})$  are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{\text{IH}}$  and  $V_{\text{IL}}$ .
9. Operation with the  $t_{\text{RCD}}(\text{max})$  limit insures that  $t_{\text{RAC}}(\text{max})$  can be met,  $t_{\text{RCD}}(\text{max})$  is specified as a reference point only, if  $t_{\text{RCD}}$  is greater than the specified  $t_{\text{RCD}}(\text{max})$  limit, then access time is controlled exclusively by  $t_{\text{CAC}}$ .
10. Operation with the  $t_{\text{RAD}}(\text{max})$  limit insures that  $t_{\text{RAC}}(\text{max})$  can be met,  $t_{\text{RAD}}(\text{max})$  is specified as a reference point only, if  $t_{\text{RAD}}$  is greater than the specified  $t_{\text{RAD}}(\text{max})$  limit, then access time is controlled exclusively by  $t_{\text{AA}}$ .
11.  $t_{\text{WCS}}$  is not restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If  $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$ , the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle.
12. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early write cycles.
13.  $t_{\text{RASP}}$  is defines  $\overline{\text{RAS}}$  pulse width in Fast Page Mode cycles.
14. Access time is determined by the longer of  $t_{\text{AA}}$  or  $t_{\text{CAC}}$  or  $t_{\text{ACP}}$ .
15. An initial pause of  $100_{\mu\text{S}}$  is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing  $\overline{\text{RAS}}$  clock such as  $\overline{\text{RAS}}$  only refresh). If the internal refresh counter is used, a minimum of eight  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh cycles are required.

**Timing Waveforms : Please refer to attached Timing Waveform-11**

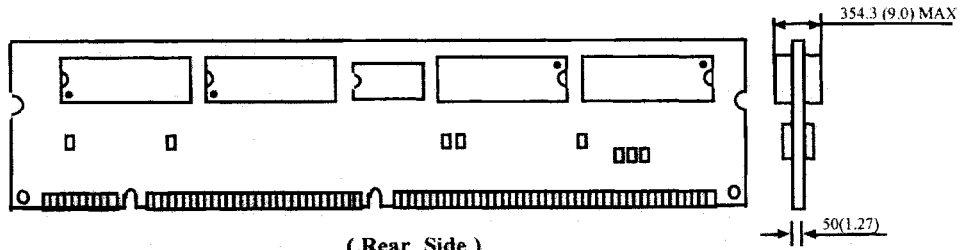
Package Dimension

Unit: mil (mm)

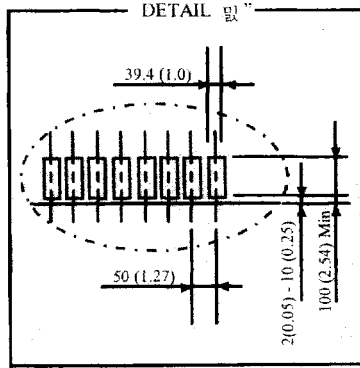
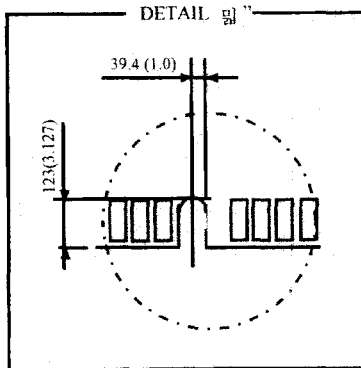
\* (1mil = 1/1000 inches)



( Front Side )



( Rear Side )



NOTE : 1. Tolerances on all dimensions  $\pm 5 (0.127)$  unless otherwise specified.  
 2. Thickness includes Plating and / or Metallization.