F10125 • F10525

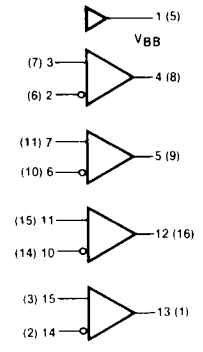
QUAD ECL TO TTL TRANSLATOR

F10K VOLTAGE COMPENSATED ECL

DESCRIPTION — The F10125 and F10525 are Quad Translators for converting F10K logic levels to TTL logic levels. Differential inputs allow each circuit to be used as an inverting, non-inverting or as a differential receiver. An Internal reference voltage generator provides V_{BB} on Pin 1 for single-ended operation or for use in Schmitt trigger applications. The outputs, which will go LOW when the inputs are left unconnected, have a fan-out of 10 Schottky TTL loads.

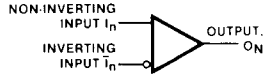
When used in the differential mode, the inputs have a common mode rejection of +1 V, making this device tolerant of ground offsets and transients between the signal source and the translator.

LOGIC DIAGRAM



V_{CC} = 9 (13) GND = 16 (4)
V_{EE} = 8 (12) ( ) = Flatpak

FUNCTION



TRUTH TABLE

INPUTS		OUTPUT
Non-Inverting I_n	Inverting $\overline{I}_n$	O_n
L	H	L
H	L	H
L	L	*
H	H	*
OPEN	OPEN	L
V_{EE}	V_{EE}	L
L	V_{BB}	L
H	V_{BB}	H
V_{BB}	L	H
V_{BB}	H	L

*Undetermined

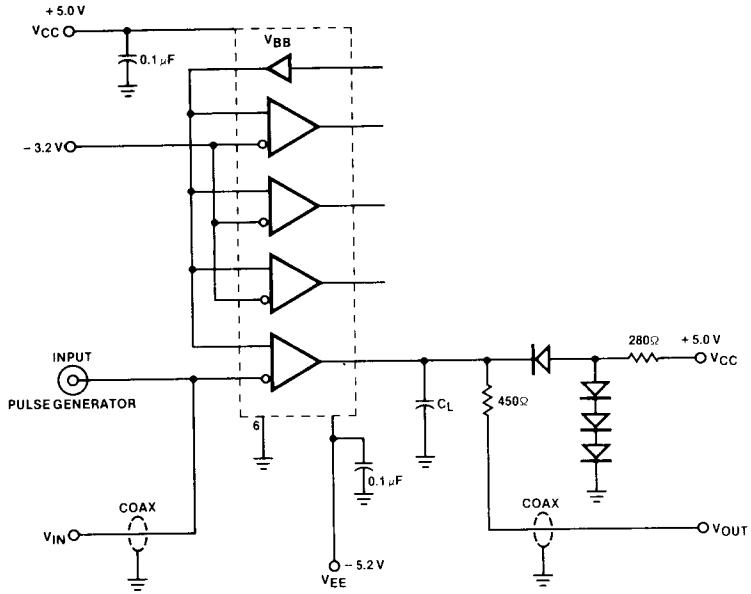
DC CHARACTERISTICS: V_{EE} = −5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS	
V_{OH}	Output Voltage HIGH	+2.5 +2.5 +2.5			V	−55/0 °C 25 °C 125/75 °C	V_{IN} = V_{IHA} or V_{ILB} per Truth Table	Loading is −2.0 mA V_{OH} +20mA V_{OL}
V_{OL}	Output Voltage LOW			+0.5 +0.5 +0.5	V	−55/0 °C 25 °C 125/75 °C		
V_{OHC}	Output Voltage HIGH	+2.5 +2.5 +2.5			V	−55/0 °C 25 °C 125/75 °C	V_{IN} = V_{IHB} or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			+0.5 +0.5 +0.5	V	−55/0 °C 25 °C 125/75 °C		

SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PLH}, t_{PHL}	Propagation Delay, LOW to HIGH, HIGH to LOW	1.0		6.0	ns	See Figure 1
t_{TLH}, t_{THL}	Output Transition Time 1.0 V to 2.0 V, 2.0 V to 1.0 V			3.3	ns	

SWITCHING CIRCUIT AND WAVEFORMS



50Ω termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50Ω coaxial cable. Wire length should be <¼ inch from TP_{IN} to input pin and TP_{OUT} to output pin.

C_L = 25 pF, including fixture

One input from each gate must be tied to V_{BB} during testing.

PROPAGATION DELAY

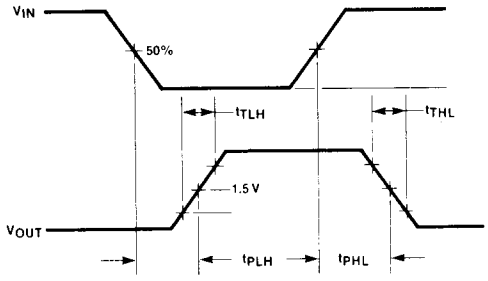


Fig. 1