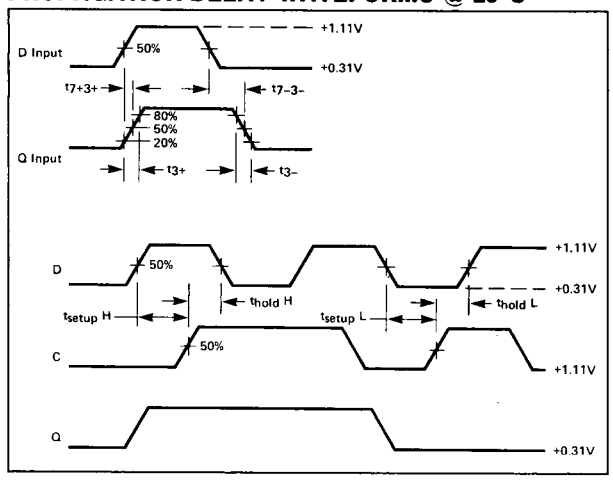
10165F

PROPAGATION DELAY WAVEFORMS @ 25°C



9-BIT PARITY CIRCUIT (WITH 2 CARRY INPUTS) 10170

10170-F

FEATURES

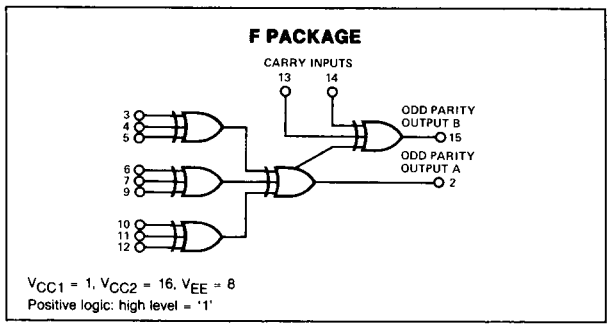
- Optimized for byte-organized systems
- Fast propagation delay
  - = 4.0 ns TYP (input to output A)
  - = 6.0ns TYP (input to output B)
  - = 2.0ns TYP (carry to output B)
- Carry inputs for easy expansion or odd/even control
- Up to 9 bit check in 4.0ns
- Up to 27 bit check in 6.0ns with no additional gates required
- Low power dissipation = 280mW/package TYP (no load)
- High fanout capability — can drive 50Ω lines
- High Z inputs — internal 50kΩ pulldowns
- High immunity from power supply variations
- Open emitter outputs for logic and bussing capability

APPLICATIONS

DETECTION OR GENERATION OF PARITY IN:

- High speed central processors
- High speed peripherals
- High speed minicomputers
- Communication systems
- Instrumentation

LOGIC DIAGRAM



TRUTH TABLE

INPUT	OUTPUT
SUM OF HIGH LEVEL INPUTS PINS 3-12	PIN 2
EVEN	LOW
ODD	HIGH
SUM OF ALL HIGH LEVEL INPUTS (INCLUDING CARRY INPUTS)	PIN 15
EVEN	LOW
ODD	HIGH

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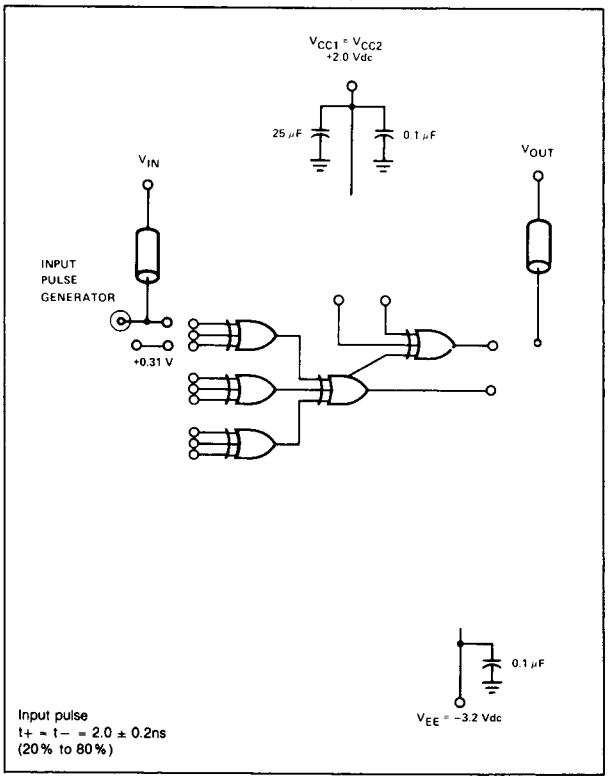
SWITCHING TIME TEST CIRCUIT



Input pulse
t+ = t− = 2.0 ± 0.2ns
(20% to 80%)

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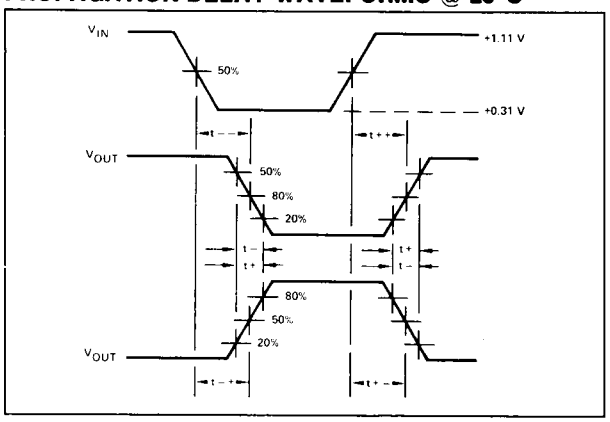

NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 fpm is maintained. Voltage levels will shift approximately 5mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to −2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire lengths should be < ¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope channel input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.