

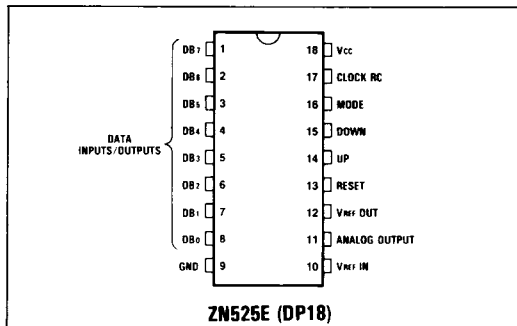
# ZN525

## 8-BIT MULTIFUNCTION DATA CONVERTER

The ZN525 is a versatile, multifunction 8-bit data conversion system. A voltage-output DAC, 8-bit up/down counter, stable 2.5V bandgap reference and clock generator are contained on a single chip.

### FEATURES

- Multimode Device Operates As:
  - DAC
  - ADC
  - Tracking ADC
  - Voltage to Frequency Converter
  - Ramp and Sawtooth Generator
  - Non-linear Waveform Generator
  - Voltage-Controlled Oscillator
  - Track-and-Hold Circuit
- 8-Bit Accuracy
- 800ns DAC Settling Time
- On-Chip Up/Down Counter
- On-Chip Clock
- On-Chip Voltage Reference
- Single +5V Supply
- Commercial or Military Temperature Range



Pin connections (top view)

### ORDERING INFORMATION

Device type	Operating temperature	Package
ZN525E	0°C to +70°C	DP18

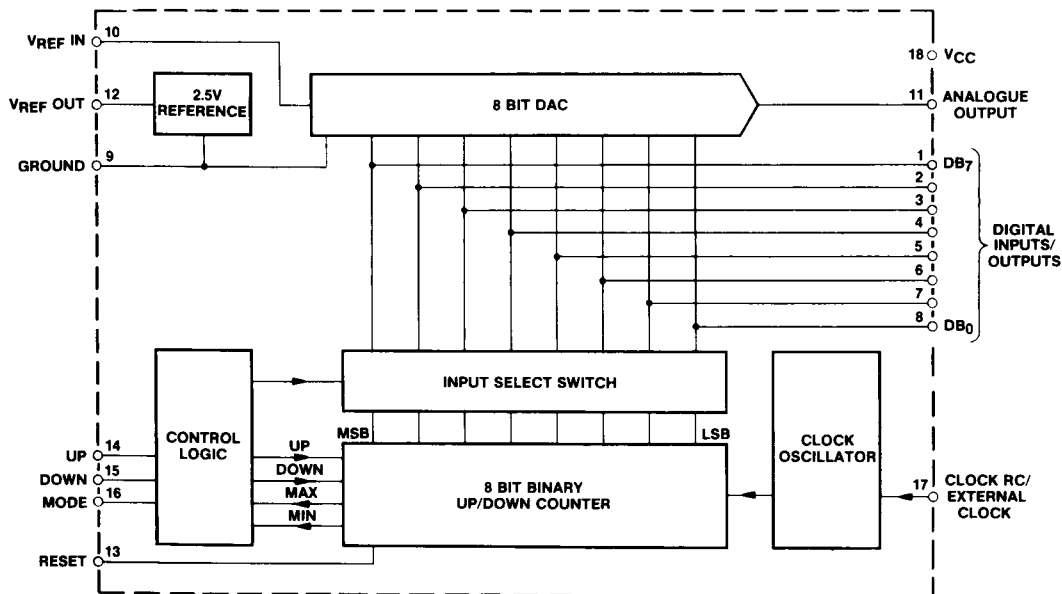


Fig.1 System diagram

**ELECTRICAL CHARACTERISTICS**

Test conditions (unless otherwise stated):

$$V_{CC} = +5V, V_{REF} = 1.5V - 3.0V, T_{amb} = +25^{\circ}C$$

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
<b>D to A Converter</b>					
Resolution	8	-	-	Bits	
Linearity error	-	±0.25	±0.5	LSB	} $T_{min}, T_{amb}, T_{max}$
Differential linearity error	±0.25		±1	LSB	
Zero error	-	5.0	10.0	mV	ZN525E All bits OFF
Settling time to 0.5 LSB	-	500	-	ns	All bits OFF to ON or vise versa
	-	800	-	ns	
Full-scale output	2.545	2.550	2.555	V	All bits ON $V_{REF} = 2.56V$
Output resistance	-	4	-	kΩ	
Full-scale temperature coefficient	-	4	-	ppm/°C	Ext. $V_{REF} = 2.56V$
Reference voltage	0	-	3	V	
<b>On-chip voltage reference</b>					
Output voltage	2.4	2.59	2.7	V	$R_{REF} = 390\Omega$
Slope resistance	-	2	4	Ω	$C_{REF} = 220nF$
Temperature coefficient of $V_{REF}$	-	50	-	ppm/°C	
Reference current	4	-	15	mA	
<b>Counter (with external clock)</b>					
High level threshold voltage $V_{T+}$	-	-	2.3	V	Note 1
Low level threshold voltage $V_{T-}$	1.7	-	-	V	
Maximum clock frequency	1	-	-	MHz	
<b>On-chip clock</b>					
Maximum frequency	500	-	-	kHz	
Clock frequency tempco	-	100	-	ppm/°C	
Clock resistor	3.3	-	100	kΩ	
Clock capacitor	100	-	-	pF	
High level threshold voltage $V_{T+}$	-	4.6	-	V	
Low level threshold voltage $V_{T-}$	-	1.5	-	V	
Supply rejection	-	0.8	-	%/V	
<b>Logic circuits</b>					
<b>Bit Inputs</b>					
High level input voltage $V_{IH}$	2.0	-	-	V	
Low level input voltage $V_{IL}$	-	-	0.8	V	
High level input current $I_{IH}$	-	-	-180	μA	$V_{IN} = 2.4V$
Low level input current $I_{IL}$	-	-	-400	μA	$V_{IN} = 0.4V$
<b>Bit Outputs</b>					
High level output voltage $V_{OH}$	-	5.0	-	} No load	
Low level output voltage $V_{OL}$	-	0.1	-		
High level output voltage $V_{OH}$	2.4	-	-	V	$I_{OH} = -40\mu A$
Low level output voltage $V_{OL}$	-	-	0.4	V	$I_{OL} = 2.5mA$
<b>Control inputs</b>					
High level input voltage $V_{IH}$	2	-	-	V	
Low level input voltage $V_{IL}$	-	-	0.8	V	
High level input current $I_{IH}$	-	-	-25	μA	$V_{IN} = 2.4V$
Low level input current $I_{IL}$	-	-	-95	μA	$V_{IN} = 0.4V$
Reset pulse width	200	-	-	ns	
<b>Power supply</b>					
Supply voltage	4.5	5	5.5	V	
Supply current	-	39	47	mA	$V_{CC} = 5.5V$

NOTES 1 Speeds of up to 1.7MHz may be obtained by reducing the mark space ratio of the clock.

**ABSOLUTE MAXIMUM RATINGS**

Supply voltage	+7V
Max. voltage, logic and V <sub>REF</sub> inputs	V <sub>CC</sub>
Operating temperature range	0°C to +70°C
Storage temperature range	-55°C to +125°C

**GENERAL CIRCUIT OPERATION**

The ZN525 incorporates an 8-bit DAC based on a voltage switching R-2R ladder network. The reference voltage for this ladder may be derived from the on-chip precision bandgap reference, or an external reference voltage may be supplied.

The ZN525 also contains an 8-bit up/down counter and control logic. The DAC may receive its digital input data from the counter, the counter outputs being simultaneously available at an 8-bit I/O port. Alternatively the counter outputs may be inhibited and the I/O port used to feed data direct to the DAC inputs.

An on-chip oscillator is provided to drive the clock input of

the up/down counter. The on-chip clock may be overridden by an external clock signal.

**UP/DOWN COUNTER AND CONTROL LOGIC**

The counter is a high-speed, synchronous up/down type, whose operation is determined by four control pins. The functions of the UP, DOWN and RESET inputs are fairly self explanatory, the MODE input determines the behaviour of the counter at zero and full-scale. When the MODE input is high the counter will reset to zero if it is clocked past full-scale in the UP direction and will reset to 255 if it is clocked past zero in the DOWN direction. When the MODE input is low the counter will stop on reaching full-scale or zero.

The normally invalid state of UP and DOWN inputs low simultaneously is also utilised in the ZN525. With the MODE input high and UP and DOWN inputs low the counter will cycle up and down continuously, reversing at full-scale and zero. With all three control inputs low the counter outputs are disabled and the DAC inputs accessible from the I/O port.

A truth table for the control inputs is given in Table 1.

Reset	Mode	Down	Up	Digital function	Analogue waveform
1	1	1	1	Counter stopped.	
1	1	1	0	Count up continuously.	
1	1	0	1	Count down continuously.	
1	1	0	0	Count up, reverse at F.S., count down, reverse at zero.	
1	0	1	1	Counter stopped.	
1	0	1	0	Count up, stop at F.S.	
1	0	0	1	Count down, stop at zero.	
X	0	0	0	DAC mode, counter output disabled. Counter can still be reset by taking reset input low.	
0	X	X	X	Counter reset. Does not affect analogue output in DAC mode.	

Table 1

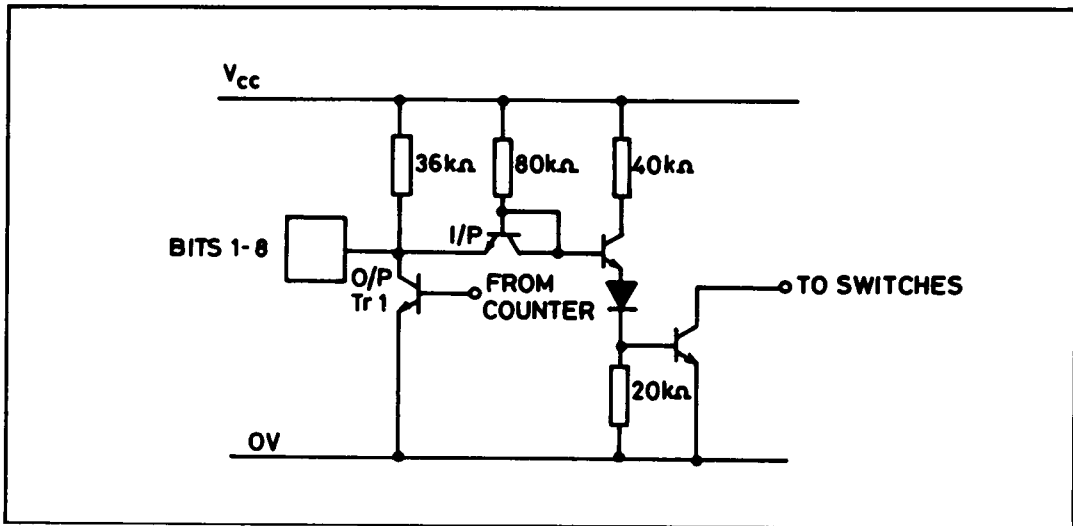


Fig.2 Bit inputs/outputs

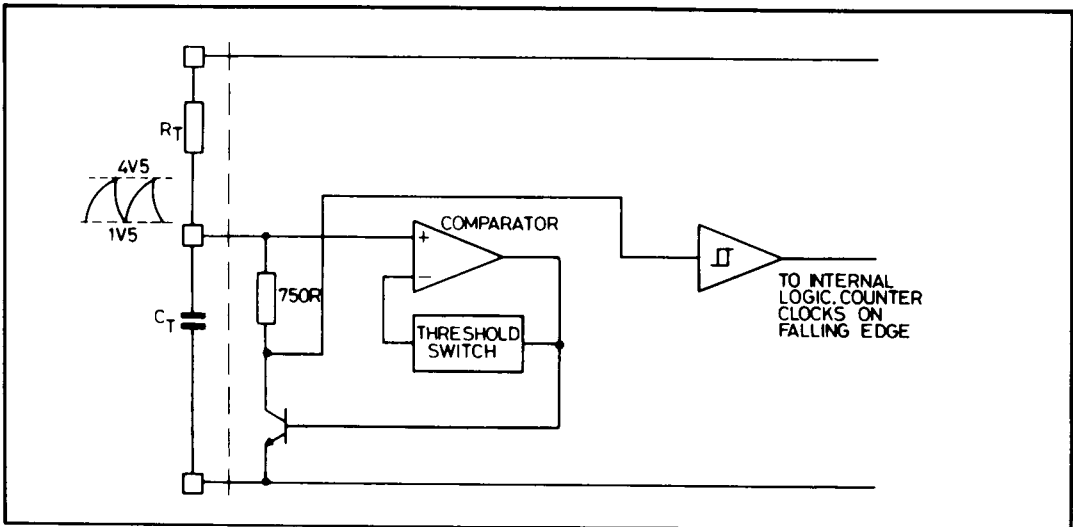


Fig.3

**DATA PORT**

One bit of the data port is shown in Fig.2. The input/output pin is the junction of the counter output buffer and the DAC input buffer.

Normally the DAC is driven from the counter and the counter data is also available at the port. However, when the counter outputs are disabled the output transistors are turned off and the DAC inputs may be accessed from the data port.

The data port can drive or be driven from B-series CMOS and all TTL families

**CLOCK CIRCUIT**

The on-chip clock circuit of the ZN525 is shown in Fig.3. The frequency of the clock is given by

$$f_{CLK} \approx \frac{1}{2R_T C_C} \text{ (Hz, } \Omega, \text{ F)}$$

Typical graphs of oscillator frequency versus resistor and capacitor values are given in Fig.4.

# ZN525

F CLK

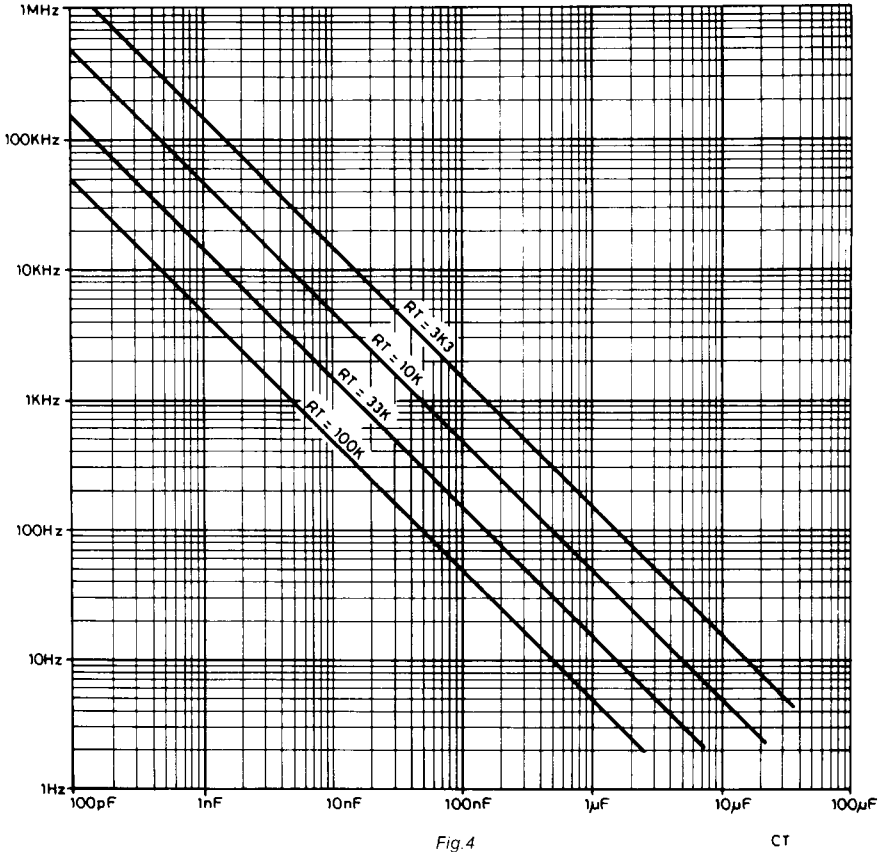


Fig. 4

The external capacitor  $C_T$  is charged via the external resistor  $R_T$  to the upper threshold of the comparator (about +4.5V with  $V_{CC} = +5V$ ). The comparator turns on the discharge transistor to discharge  $C_T$  and switches its threshold to the lower value of about 1.5V. When the voltage on  $C_T$  has fallen to this level the comparator turns off the discharge transistor and the cycle repeats.

The clock can be overdriven from either a TTL totem-pole output (Fig.5(a)), an open collector output (Fig.5(b)), or a CMOS gate (Fig.5(c)). In all three cases the  $V_{OH}$  of the driving gate must be attenuated to below 4V so that the internal discharge transistor is not turned on.

**ANALOG CIRCUITS**

**D to A Converters**

The DAC is of the voltage switching type and uses an R-2R ladder network as shown in Fig.6

Each 2R element is connected to either 0V or  $V_{REF IN}$  by transistor voltage switches specially designed for low offset voltage (<1 millivolt). A binary weighted voltage is produced at the output of the R-2R ladder.

$$V_{OUT} = \frac{n}{256} (V_{REF IN} - V_{OS}) + V_{OS}$$

where n is the digital input from the counter or data port.

$V_{OS}$  is a small offset voltage that is produced by the device supply current flowing in the package lead resistance. The value of  $V_{OS}$  is typically 5mV for the device in any package. This offset will normally be removed by the setting up procedure and since the offset temperature coefficient is small the zero drift will be small. The DAC output range can be considered to be 0V to  $V_{REF IN}$  with an output resistance R (4k $\Omega$ ).

**REFERENCE**

**On-Chip Reference**

The internal reference is an active bandgap circuit which is equivalent to a 2.5V zener diode with a very low slope impedance (Fig.7).

An external resistor ( $R_{REF}$ ) should be connected between pins 12 and 18 to bias up the on-chip reference, whilst a stabilising/decoupling capacitor ( $C_{REF}$ ) is required between pins 12 and 9.

To use the internal reference  $V_{REF OUT}$  (pin 12) is connected to  $V_{REF IN}$  (pin 10).

The recommended reference resistor of 390 $\Omega$  will supply a nominal reference current of 6.4mA which is sufficient to drive the reference inputs of up to five ZN525s. Where several ZN525s are used in a system this useful feature can save up to four resistors and capacitors as well as reducing power consumption and giving excellent gain tracking.

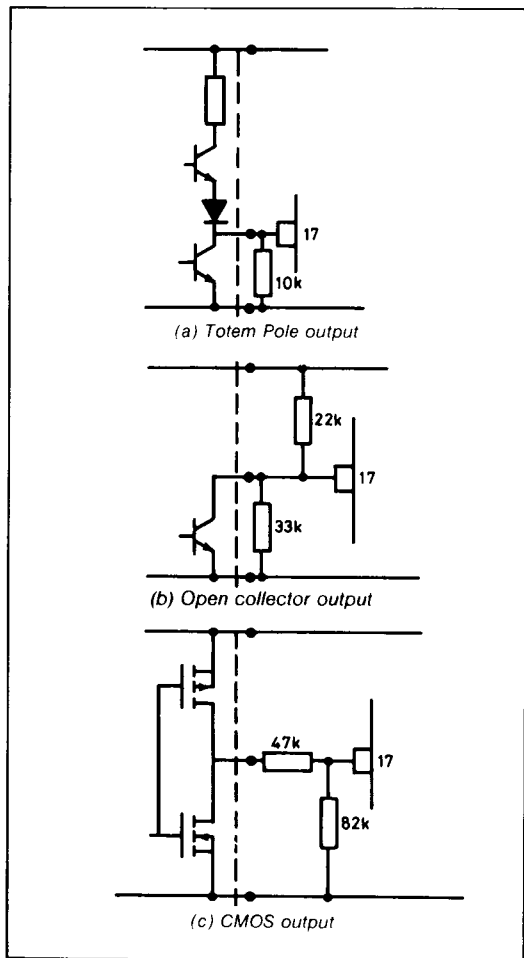


Fig.5 Overdriving the clock input

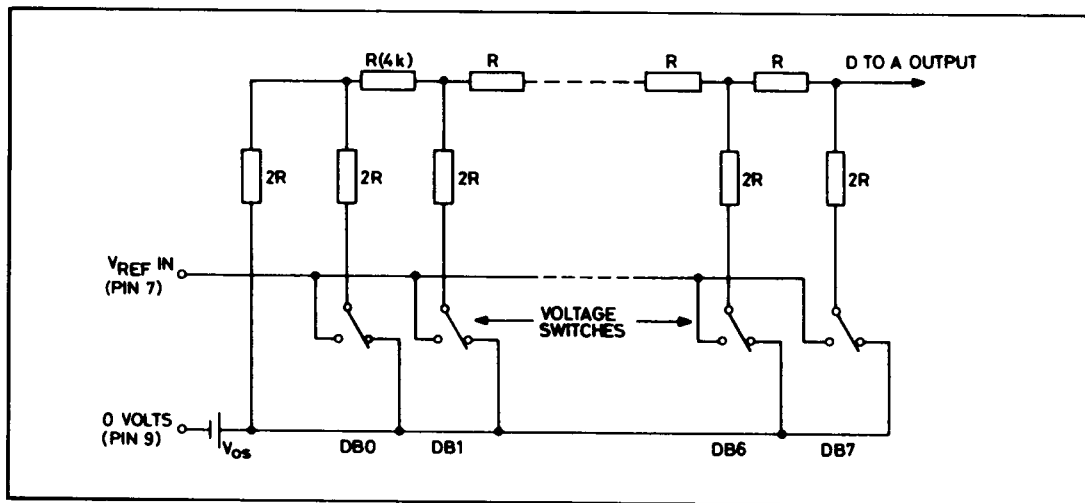


Fig.6 R-2R ladder network

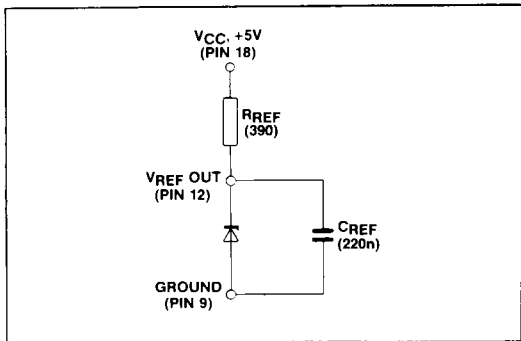


Fig.7 Internal voltage reference

**APPLICATIONS**

The applications of the ZN525 are too many and varied to detail in this data sheet. However a few basic configurations are illustrated. A feature of the device is that the UP/DOWN control lines can be changed totally asynchronously to the clock. The data presented to these UP/DOWN lines will be latched on the positive edge of clock and the counter will act upon this latched data on the following negative clock edge.

**WAVEFORM GENERATOR**

The circuit of a low frequency waveform generator is illustrated in Fig.8. This will produce stable, linear, sawtooth and triangle waveforms.

**RAMP AND COMPARE A TO D CONVERTER**

A simple ramp and compare A to D converter can be constructed using the ZN525 as shown in Fig.9.

The counter is set to count up from zero, producing a positive-going ramp at the analog output. When the ramp voltage exceeds the analog input the comparator output will go high, inhibiting the clock and stopping the counter. The converter can be reset and re-started by applying a low-going pulse to the reset input.

The basic analog input range is 0 -  $V_{REF}$ , but other ranges can be accommodated by adding an attenuator to the comparator unit. The comparator offset adjustment can be used for zero adjustment. Note that in this circuit the mode input is tied low to make the counter stop at full-scale. This prevents the counter cycling in the event of an overrange input.

**TRACKING A TO D CONVERTER**

The on-chip up-down counter allows the ZN525 to be configured very simply as a tracking A to D converter using an external comparator, as shown in Fig.10.

In this circuit two ZN424 op amps are used to make a window comparator. This has a deadband equal to one LSB of the DAC output (10mV), which is set by adjusting the offset of A1 until its threshold is 10mV above that of A2.

Whenever the analog voltage is above the threshold of A1 the counter will count up so that the DAC output increases to follow the analog voltage. Whenever the analog voltage is below the threshold of A2 the counter will count down to make the DAC follow the analog voltage. When the analog voltage is between the two thresholds the outputs of A1 and A2 will be high and the counter will be stopped.

The circuit here has an analog input range of  $\pm 10V$ . Other ranges may be accommodated by suitable choice of input resistors.

Note that in this circuit the mode input is tied low. This causes the counter to stop when full-scale or zero is reached, i.e. when the analog input exceeds plus or minus full-scale. Without this feature the counter would simply cycle continuously.

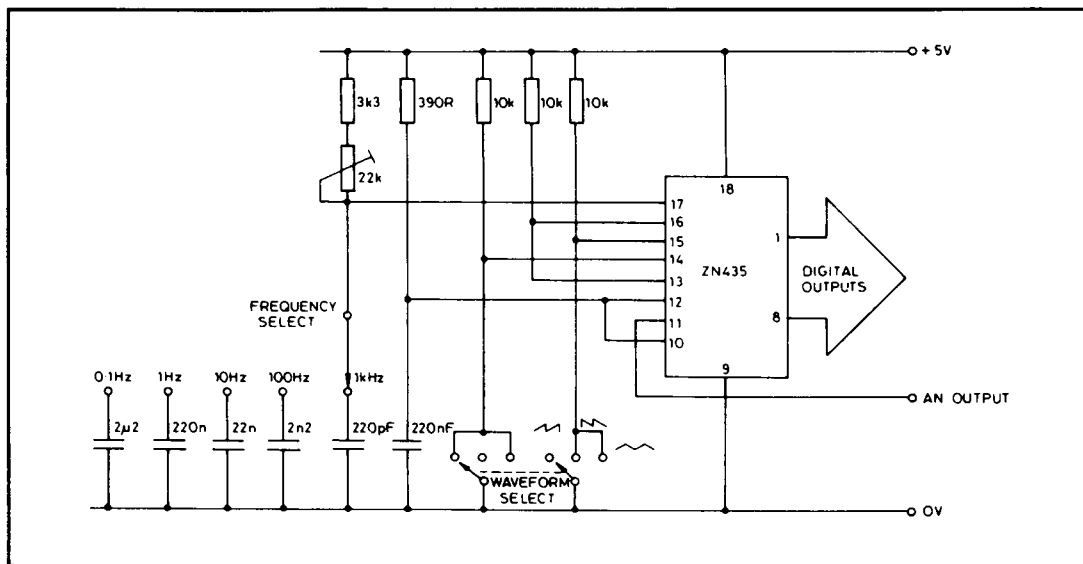


Fig.8 Waveform generator

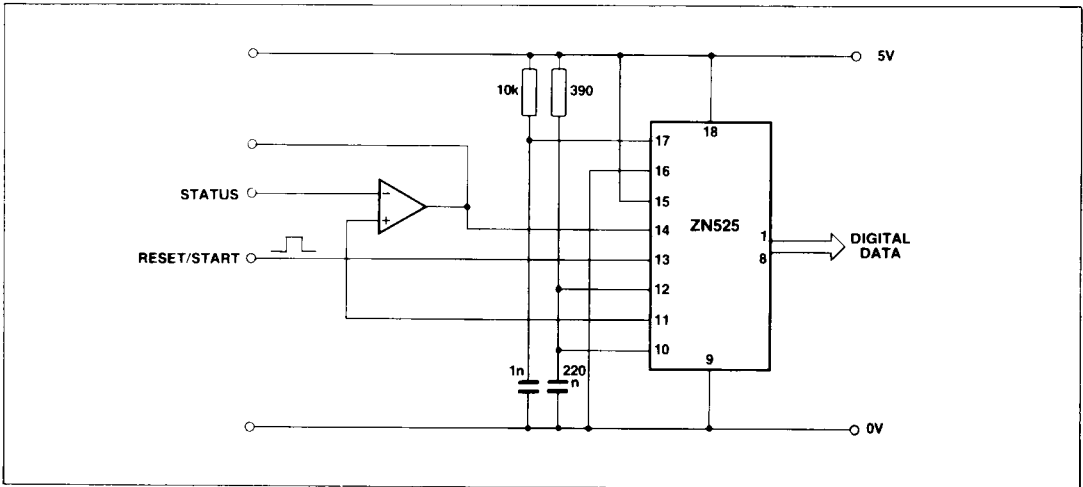


Fig 9 Ramp and compare ADC

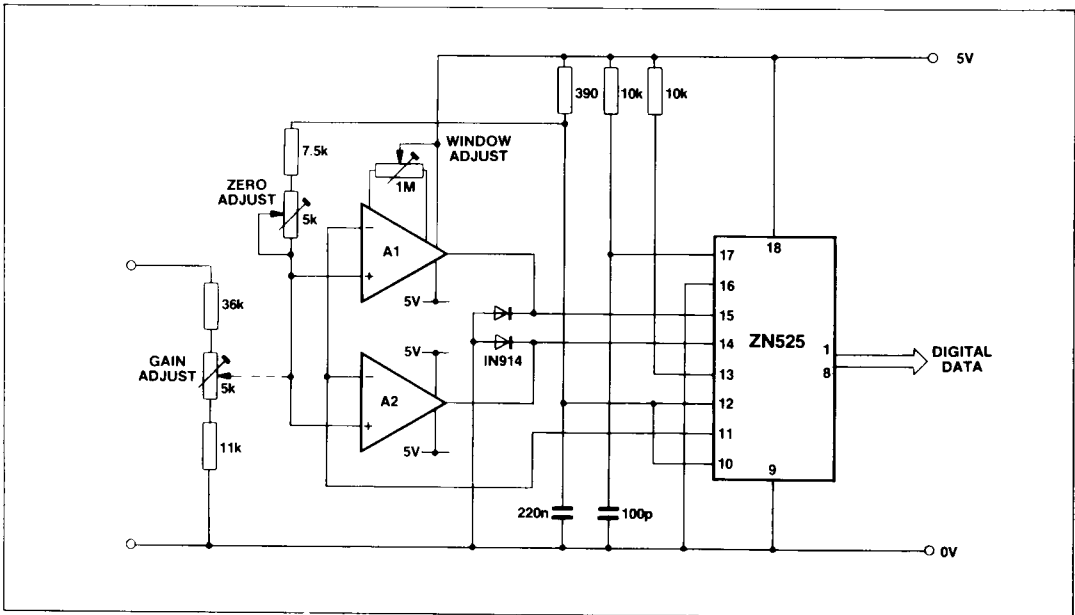


Fig 10 Tracking ADC