

TC74HC696AP/AF • TC74HC697AP/AF TC74HC698AP/AF • TC74HC699AP/AF

SYNCHRONOUS PRESETTABLE 4-BIT UP/DOWN COUNTER WITH OUTPUT REGISTER
(MULTIPLEXED 3-STATE OUTPUTS)

TC74HC696AP/AF DECADE, ASYNCHRONOUS CLEAR
TC74HC697AP/AF BINARY, ASYNCHRONOUS CLEAR
TC74HC698AP/AF DECADE, SYNCHRONOUS CLEAR
TC74HC699AP/AF BINARY, SYNCHRONOUS CLEAR

The TC74HC696A, 697A, 698A, and 699A are high speed CMOS UP/DOWN COUNTERS fabricated with silicon gate CMOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC696A/698A are BCD decade counters and the TC74HC697A/699A are 4 bit binary counters.

They count on the rising edge of the Counter Clock (CCK) input when "counter mode" is selected. If the up/down (U/D) input is held high, the internal counter counts up. Conversely, if $\overline{U/D}$ is held low, it counts down. The internal counters' outputs are latched into the output registers on the rising edge of the Register Clock (RCK) input.

The outputs (QA~QD) are selected as either internal counter or registered outputs by the output select (R/C) input. When high, the outputs are counter outputs and when low, they are registered outputs.

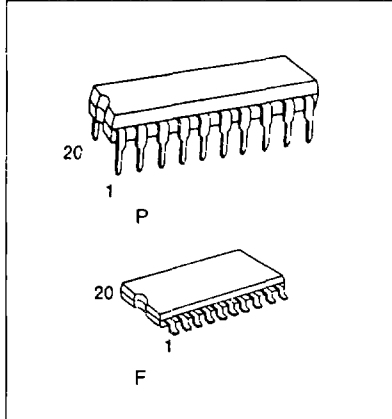
The clear function of the TC74HC698A/699A are synchronous to clock, while the TC74HC696A/697A are cleared asynchronously.

Two enable (ENP, \overline{ENT}) inputs and a carry (\overline{RCO}) output are provided to enable cascading of the counters. This facilitates easy implementation of n-bit counters without using external gates.

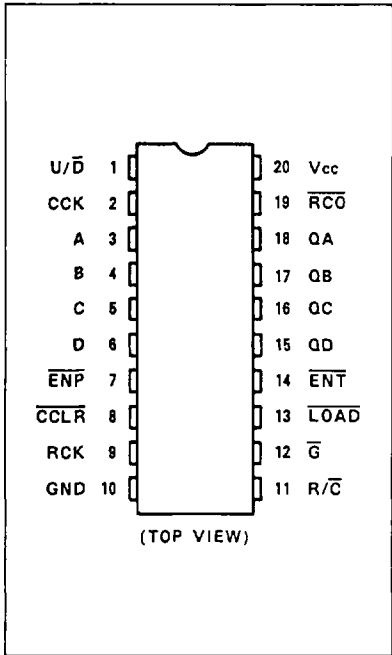
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed $f_{MAX}=38MHz(Typ.)$ at $V_{CC}=5V$
- Low Power Dissipation $I_{CC}=4\mu A(Max.)$ at $T_a=25^{\circ}C$
- High Noise Immunity $V_{NIH}=V_{NHL}=28\% V_{CC}(Min.)$
- Output Drive Capability 15 LSTTL Loads For QA~QD
10 LSTTL Loads For \overline{RCO}
- Symmetrical Output Impedance $|I_{OH}|=I_{OL}=6mA(Min.)$ For QA~QD
 $|I_{OH}|=I_{OL}=4mA(Min.)$ For \overline{RCO}
- Balanced Propagation Delays $t_{PLH} \approx t_{PHL}$
- Wide Operating Voltage Range ... $V_{CC}(opr)=2V\sim 6V$
- Pin and Function Compatible with 74LS696~699

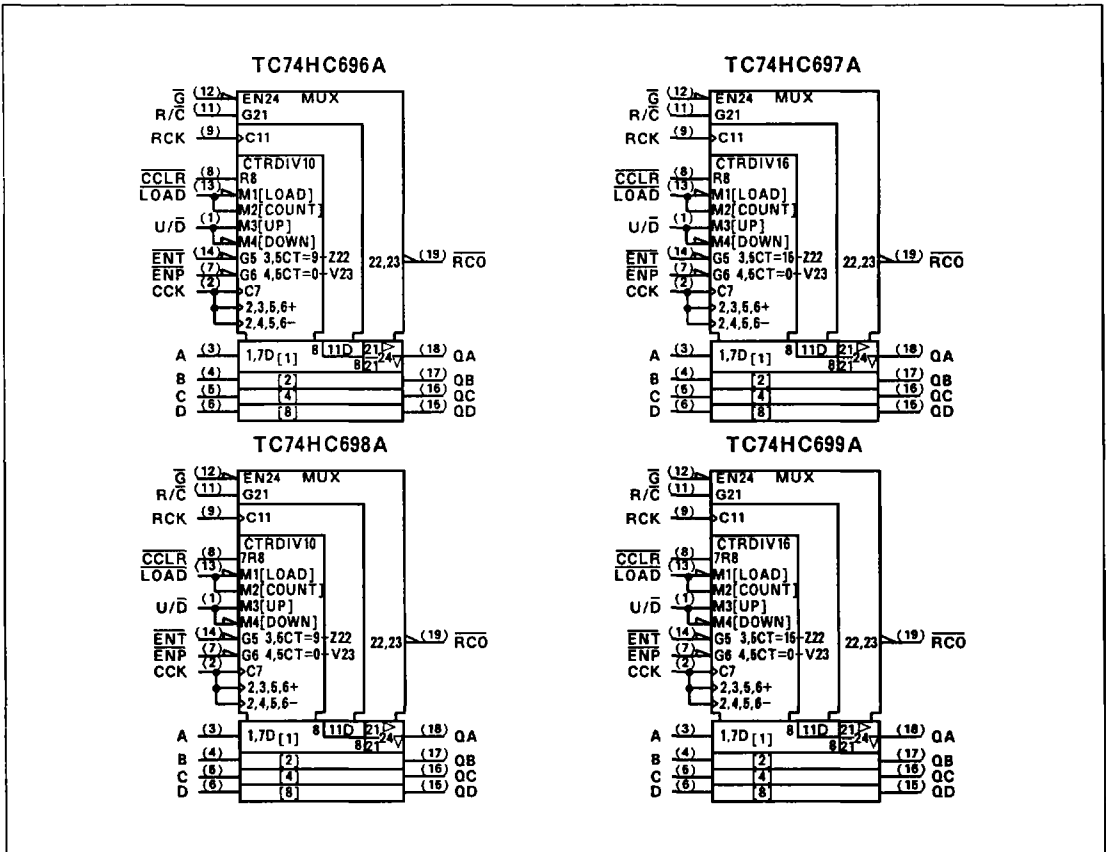


PIN ASSIGNMENT



TC74HC696AP/AF 697AP/AF 698AP/AF 699AP/AF-1

IEC LOGIC SYMBOL



TC74HC696AP/AF 697AP/AF 698AP/AF 699AP/AF-2

TRUTH TABLE

INPUTS										OUTPUTS				FUNCTION
CCLR	LOAD	ENP	ENT	CCK	CCK	U/D	RCK	R/C	G	QA	QB	QC	CD	
X	X	X	X	X	X	X	X	X	H	Z	Z	Z	Z	HIGH IMPEDANCE
L	X	X	X	X	┌	X	X	L	L	L	L	L	L	CREAR COUNTER
H	L	X	X	┌	┌	X	X	L	L	a	b	c	d	LOAD COUNTER
H	H	H	X	┌	┌	X	X	L	L	NO CHANGE				NO COUNT
H	H	X	H	┌	┌	X	X	L	L	NO CHANGE				NO COUNT
H	H	L	L	┌	┌	H	X	L	L	COUNT UP				COUNT
H	H	L	L	┌	┌	L	X	L	L	COUNT DOWN				COUNT
H	X	X	X	┌	┌	X	X	L	L	NO CHANGE				NO COUNT
X	X	X	X	X	X	X	┌	H	L	a'	b'	c'	d'	LOAD REGISTER
X	X	X	X	X	X	X	┌	H	L	NO CHANGE				NO COUNT

X : Don't care

Z : High Impedance

a ~ d : The level of steady state inputs at inputs A through D respectively.

a' ~ d' : The level of steady state outputs at internal counter outputs QA' through QD' respectively.

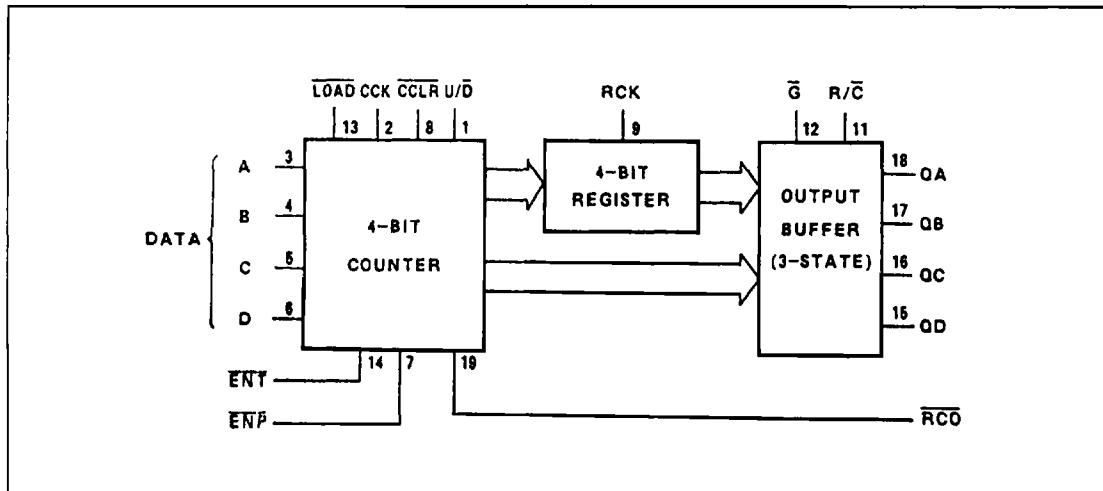
HC696A/698A ; $RCO = (\overline{UP} \cdot QA \cdot QD \cdot ENT + UP \cdot \overline{QA} \cdot \overline{QD} \cdot ENT)$

HC697A/699A ; $RCO = (\overline{UP} \cdot QA \cdot QB \cdot QC \cdot QD \cdot ENT + \overline{UP} \cdot \overline{QA} \cdot \overline{QB} \cdot \overline{QC} \cdot \overline{QD} \cdot ENT)$

• TC74HC696A/697A

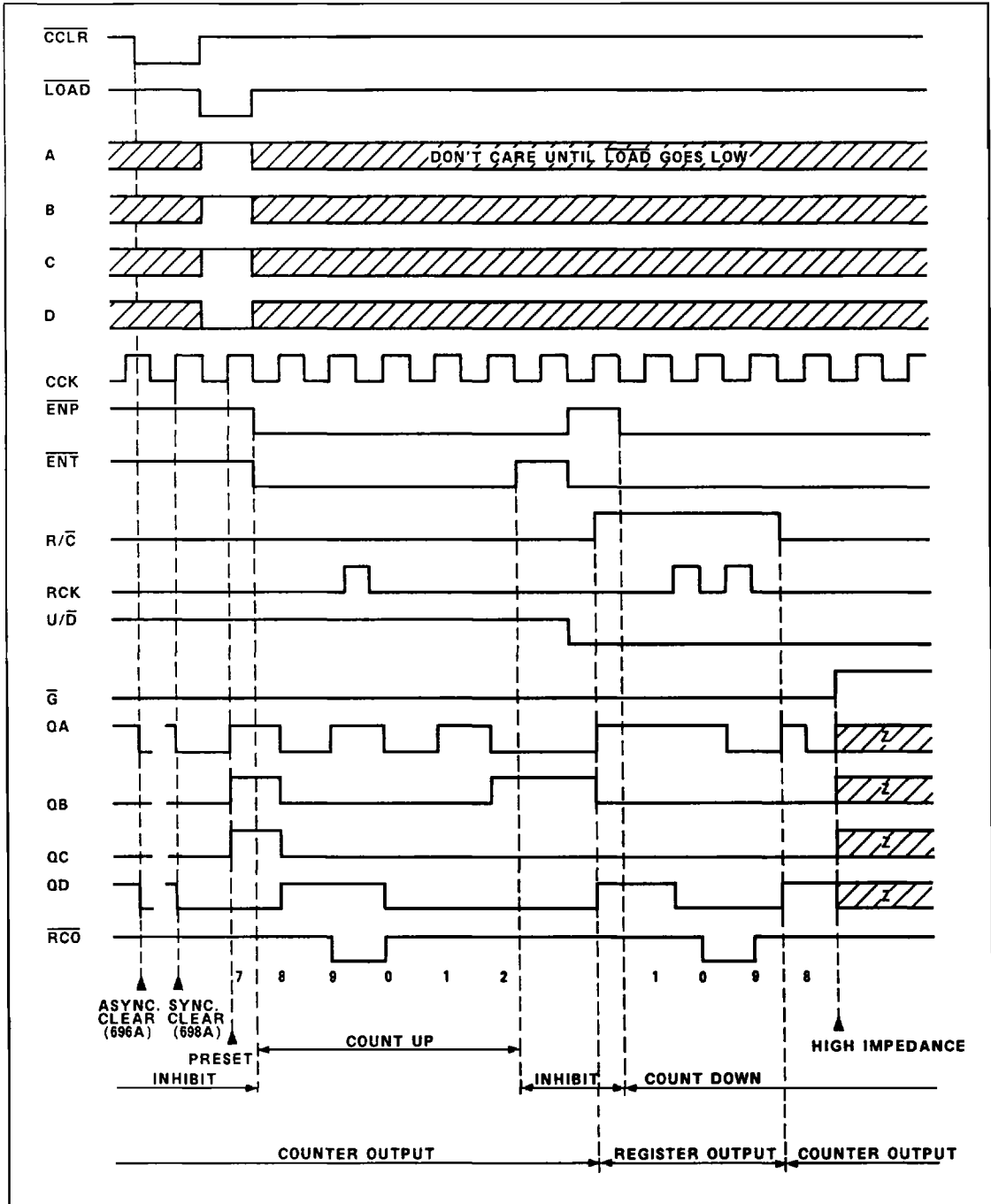
• • TC74HC698A/699A

BLOCK DIAGRAM



TC74HC696AP/AF 697AP/AF 698AP/AF 699AP/AF-3

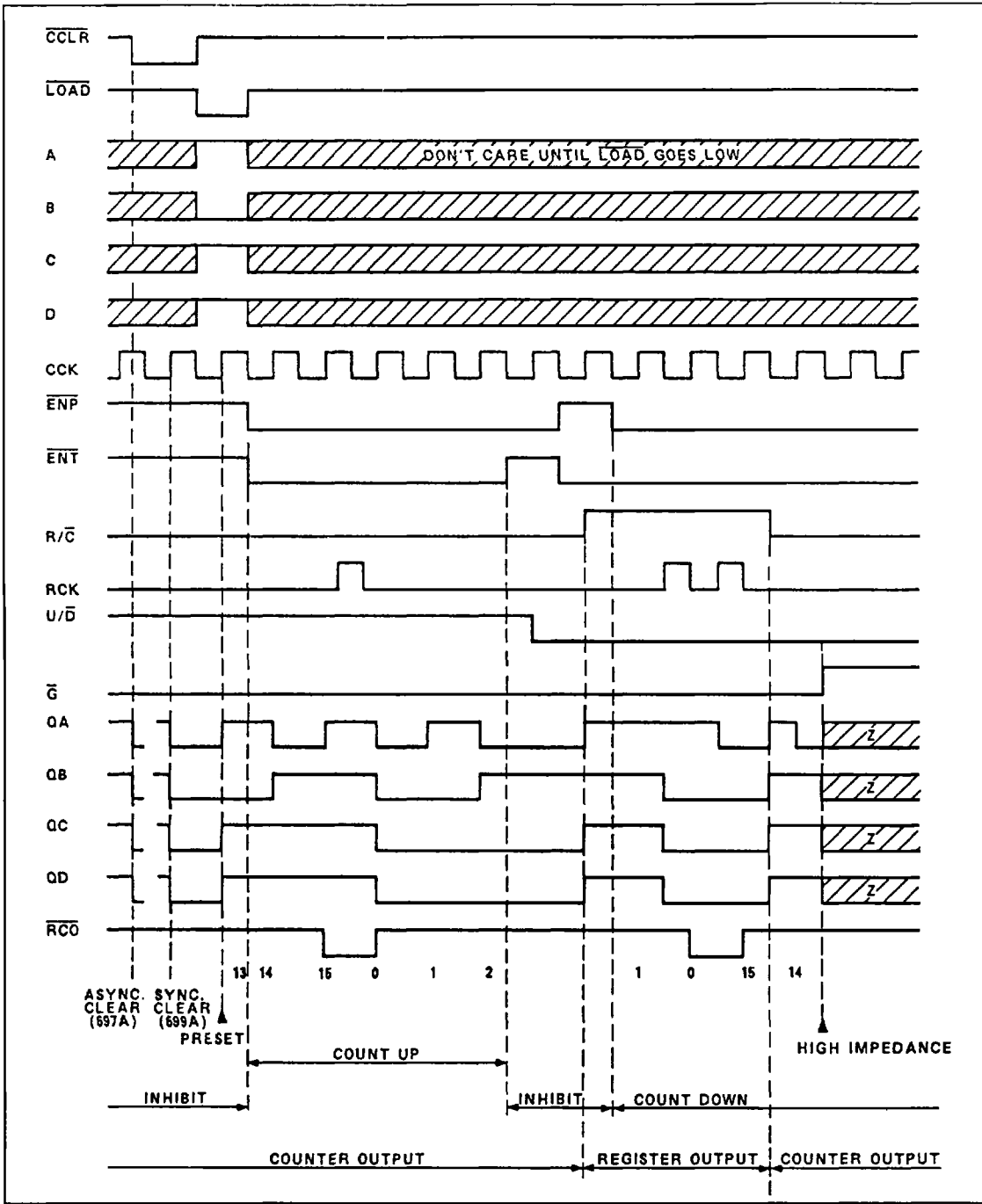
TIMING CHART (TC74HC696A/698A ; DECADE COUNTER)



TC74HC696AP/AF 697AP/AF 698AP/AF 699AP/AF-4

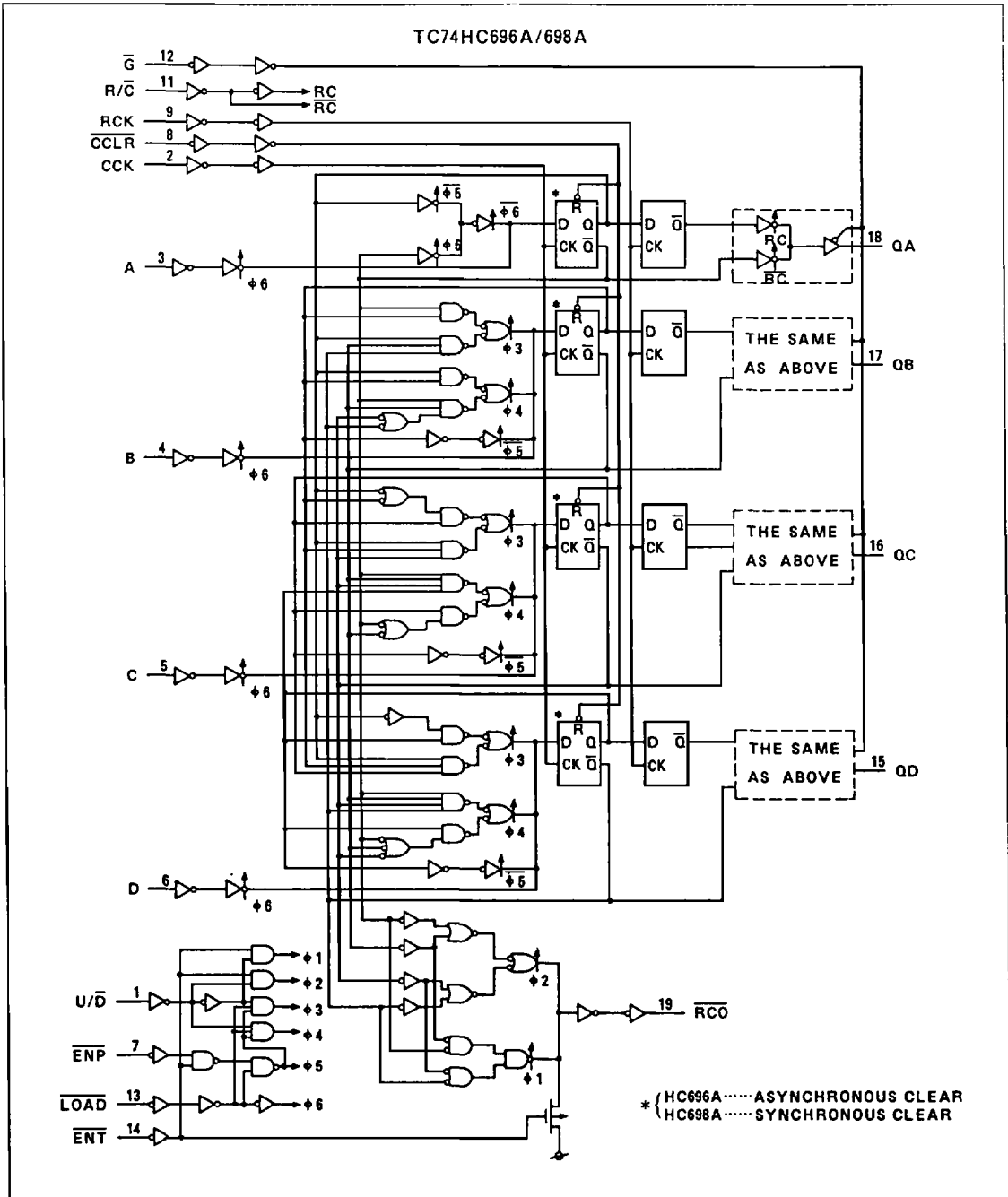


TIMING CHART (TC74HC697A/699A ; BINARY COUNTER)



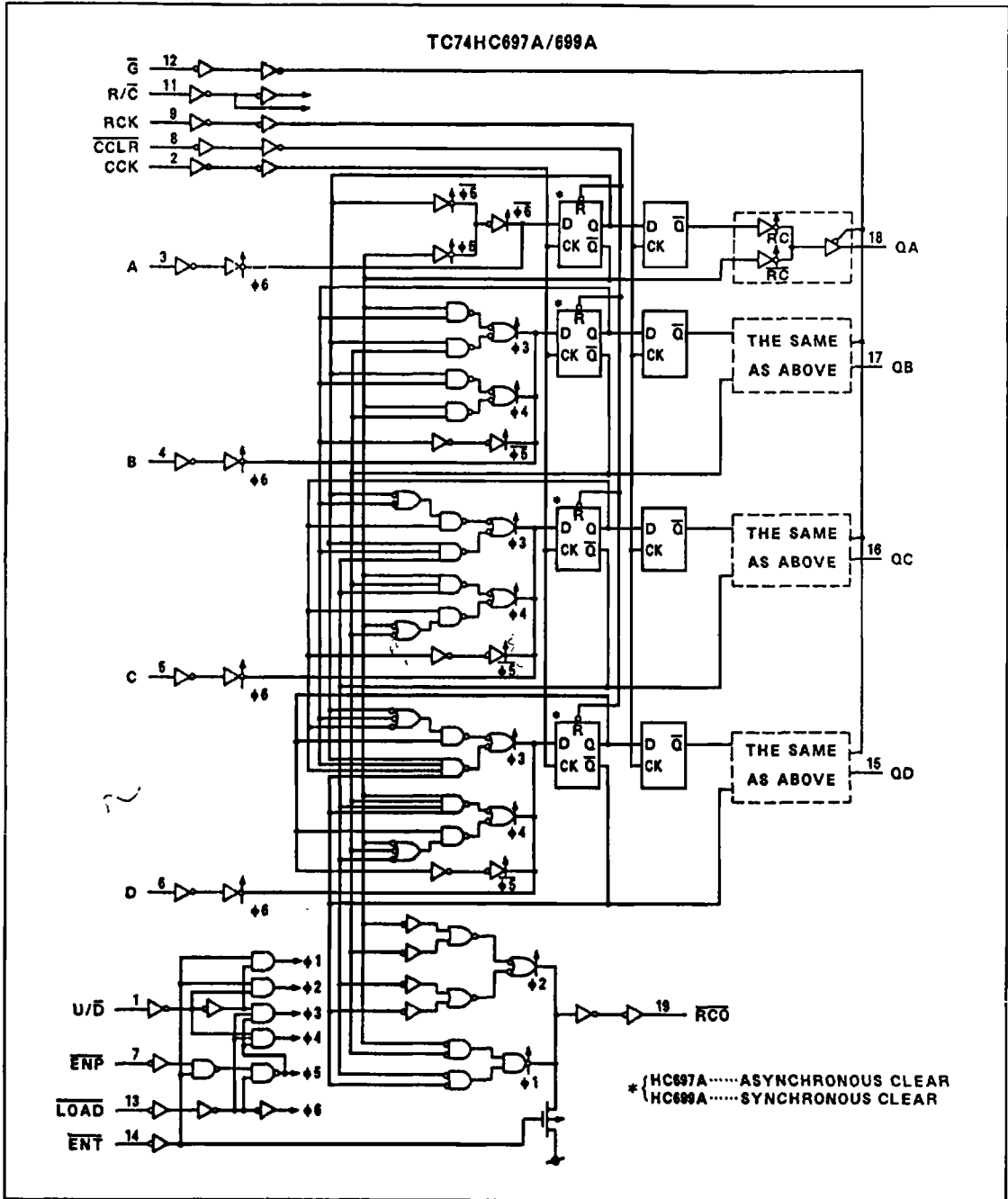
TC74HC696AP/AF 697AP/AF 698AP/AF 699AP/AF-5

SYSTEM DIAGRAM



TC74HC696AP/AF 697AP/AF 698AP/AF 699AP/AF-6

SYSTEM DIAGRAM



TC74HC696AP/AF 697AP/AF 698AP/AF 699AP/AF-7

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ $V_{CC}+0.5$	V
DC Output Voltage	V_{OLT}	-0.5 ~ $V_{CC}+0.5$	V
Input Diode Current	I_{IK}	+20	mA
Output Diode Current	I_{OY}	±20	mA
DC Output Current (RCO) ($Q_A \sim Q_D$)	I_{OLT}	±25 ±35	mA
DC V_{CC} /Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

*500mW in the range of $T_a = -40^\circ\text{C} \sim 65^\circ\text{C}$. From $T_a = 65^\circ\text{C}$ to 85°C a derating factor of -10mW/°C shall be applied until 300mW

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OLT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 1000 ($V_{CC}=2.0\text{V}$)	ns
		0 ~ 500 ($V_{CC}=4.5\text{V}$)	
		0 ~ 400 ($V_{CC}=6.0\text{V}$)	

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	$T_a=25^\circ\text{C}$			$T_a=-40 \sim 85^\circ\text{C}$		UNIT			
			V_{CC}	MIN.	TYP.	MAX.	MIN.		MAX.		
High-Level Input Voltage	V_{IH}		2.0	1.5	-	-	1.5	-	V		
			4.5	3.15	-	-	3.15	-			
			6.0	4.2	-	-	4.2	-			
Low-Level Input Voltage	V_{IL}		2.0	-	-	0.5	-	0.5	V		
			4.5	-	-	1.35	-	1.35			
			6.0	-	-	1.8	-	1.8			
High-Level Output Voltage	V_{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -20 \mu\text{A}$	2.0	1.9	2.0	-	1.9	-	V		
			4.5	4.4	4.5	-	4.4	-			
			6.0	5.9	6.0	-	5.9	-			
			RCO	$I_{OH} = -4 \text{ mA}$	4.5	4.18	4.31	-		4.13	-
				$I_{OH} = -5.2 \text{ mA}$	6.0	5.68	5.80	-		5.63	-
			$Q_A \sim Q_D$	$I_{OH} = -6 \text{ mA}$	4.5	4.18	4.31	-		4.31	-
$I_{OH} = -7.8 \text{ mA}$	6.0	5.68		5.80	-	5.63	-				
Low-Level Output Voltage	V_{OL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 20 \mu\text{A}$	2.0	-	0.0	0.1	-	0.1	V		
			4.5	-	0.0	0.1	-	0.1			
			6.0	-	0.0	0.1	-	0.1			
			RCO	$I_{OL} = 4 \text{ mA}$	4.5	-	0.17	0.26		-	0.33
				$I_{OL} = 5.2 \text{ mA}$	6.0	-	0.18	0.26		-	0.33
			$Q_A \sim Q_D$	$I_{OL} = 6 \text{ mA}$	4.5	-	0.17	0.26		-	0.33
$I_{OL} = 7.8 \text{ mA}$	6.0	-		0.18	0.26	-	0.33				
3-State Output Off-State Current	I_{OZ}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{OLT} = V_{CC} \text{ or } \text{GND}$	6.0	-	-	±0.5	-	±5.0	μA		
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC} \text{ or } \text{GND}$	6.0	-	-	±0.1	-	±1.0			
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC} \text{ or } \text{GND}$	6.0	-	-	4.0	-	40.0			

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TIMING REQUIREMENTS (Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	$T_a=25^\circ C$			$T_a=-40 \sim 85^\circ C$ LIMIT	UNIT
			V_{CC}	TYP.	LIMIT		
Minimum Pulse Width (CCK, RCK)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	75	95	ns
			4.5	-	15	19	
			6.0	-	13	16	
Minimum Pulse Width (CCLR)*	$t_{w(L)}$		2.0	-	75	95	
			4.5	-	15	19	
			6.0	-	13	16	
Minimum Set-up Time (CCLR)**	t_s		2.0	-	50	65	
			4.5	-	10	13	
			6.0	-	9	11	
Minimum Set-up Time (LOAD, ENT, ENP)	t_s		2.0	-	150	190	
			4.5	-	30	38	
			6.0	-	13	32	
Minimum Set-up Time (A, B, C, D)	t_s		2.0	-	50	65	
			4.5	-	10	13	
			6.0	-	9	11	
Minimum Set-up Time (U/D)	t_s		2.0	-	100	125	
			4.5	-	20	25	
			6.0	-	17	21	
Minimum Set-up Time (CCK-RCK)	t_s		2.0	-	100	125	
			4.5	-	20	25	
			6.0	-	17	21	
Minimum Hold Time (A, B, C, D)	t_h		2.0	-	5	5	
			4.5	-	5	5	
			6.0	-	5	5	
Minimum Hold Time (CCLR)**	t_h		2.0	-	25	30	
			4.5	-	5	6	
			6.0	-	5	5	
Minimum Hold Time	t_h		2.0	-	0	0	
			4.5	-	0	0	
			6.0	-	0	0	
Minimum Removal Time	t_{rem}		2.0	-	5	5	
			4.5	-	5	5	
			6.0	-	5	5	
Clock Frequency	f		2.0	-	5	4	MHz
			4.5	-	25	20	
			6.0	-	29	24	

AC ELECTRICAL CHARACTERISTICS ($C_L=15pF, V_{CC}=5V, T_a=25^\circ C$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time (RCO)	t_{TLH}		-	4	8	ns
	t_{THL}					
Output Transition Time (CCK-RCO)	t_{PLH}		-	24	41	
	t_{PHL}					
Propagation Delay Time (ENT-RCO)	t_{PLH}		-	13	23	
	t_{PHL}					
Propagation Delay Time (CCLR-RCO)*	t_{PLH}		-	23	38	
	t_{PHL}					
Maximum Clock Frequency	f_{MAX}		25	38	-	MHz

* : for TC74HC696A/697A only

** : for TC74HC698A/699A only

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AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=8\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	CL	Ta=25°C				Ta=-40 ~85°C		UNIT
				V _{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time (Q)	$t_{T.LH}$ $t_{T.HL}$		50	2.0	-	25	60	-	75	ns
				4.5	-	7	12	-	15	
				6.0	-	6	10	-	13	
Output Transition Time (RCO)	$t_{T.LH}$ $t_{T.HL}$		50	2.0	-	30	75	-	95	
				4.5	-	8	15	-	19	
				6.0	-	7	13	-	16	
Propagation Delay Time (CCK-Q)	$t_{p.LH}$ $t_{p.HL}$		50	2.0	-	90	195	-	245	
				4.5	-	26	39	-	49	
				6.0	-	19	33	-	42	
			150	2.0	-	103	235	-	295	
				4.5	-	31	47	-	59	
				6.0	-	23	40	-	50	
Propagation Delay Time (RCK-Q)	$t_{p.LH}$ $t_{p.HL}$		50	2.0	-	82	180	-	225	
				4.5	-	24	36	-	45	
				6.0	-	18	31	-	38	
			150	2.0	-	95	220	-	275	
				4.5	-	29	44	-	55	
				6.0	-	22	37	-	47	
Propagation Delay Time (R/C-Q)	$t_{p.LH}$ $t_{p.HL}$		50	2.0	-	60	145	-	180	
				4.5	-	19	29	-	36	
				6.0	-	14	25	-	31	
			150	2.0	-	73	185	-	230	
				4.5	-	24	37	-	46	
				6.0	-	18	31	-	39	
Propagation Delay Time (CCLR-Q)*	$t_{p.HL}$		50	2.0	-	89	195	-	245	
				4.5	-	26	39	-	49	
				6.0	-	20	33	-	42	
			150	2.0	-	102	235	-	295	
				4.5	-	31	47	-	59	
				6.0	-	24	40	-	50	
Propagation Delay Time (CCK-RCO)	$t_{p.LH}$ $t_{p.HL}$		50	2.0	-	108	235	-	295	
				4.5	-	31	47	-	59	
				6.0	-	23	40	-	50	
Propagation Delay Time (ENT-RCO)	$t_{p.LH}$ $t_{p.HL}$		50	2.0	-	63	135	-	170	
				4.5	-	18	27	-	34	
				6.0	-	14	23	-	29	
Propagation Delay Time (CCLR-RCO)*	$t_{p.LH}$ $t_{p.HL}$		50	2.0	-	98	220	-	275	
				4.5	-	29	44	-	55	
				6.0	-	23	37	-	47	

* for TC74HC696A/697A only

TC74HC696AP/AF 697AP/AF 698AP/AF 699AP/AF-10

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	Ta=25°C			Ta=-40 ~85°C		UNIT		
			CL	V _{CC}	MIN.	TYP.	MAX.		MIN.	MAX.
Output Enable time ($\bar{G}-Q$)*	t_{pZL} t_{pZH}	$R_L = 1\text{ k}\Omega$	50	2.0	-	45	115	-	145	ns
				4.5	-	15	23	-	29	
				6.0	-	12	20	-	25	
			150	2.0	-	58	155	-	195	
				4.5	-	20	31	-	39	
				6.0	-	16	26	-	33	
Output Enable time ($\bar{G}-Q$)**	t_{pZL} t_{pZH}	$R_L = 1\text{ k}\Omega$	50	2.0	-	46	110	-	140	
				4.5	-	14	22	-	28	
				6.0	-	12	19	-	24	
			150	2.0	-	62	150	-	190	
				4.5	-	19	30	-	38	
				6.0	-	16	26	-	33	
Output Disable time ($\bar{G}-Q$)	t_{pLZ} t_{pHZ}	$R_L = 1\text{ k}\Omega$	50	2.0	-	32	115	-	145	
				4.5	-	17	23	-	29	
				6.0	-	14	20	-	25	
Maximum Clock Frequency	f_{MAX}		50	2.0	5	11	-	4	-	
				4.5	25	38	-	20	-	
				6.0	29	52	-	24	-	
Input Capacitance	C_{IN}			-	5	10	-	10	pF	
Output Capacitance	C_{OUT}			-	13	-	-	-		
Power Dissipation Capacitance	$C_{PD(1)}$			-	72	-	-	-		

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(ave)} = C_{PD} \cdot V_{CC} \cdot f_N + I_{CC}$$

Note (2) * : for TC74HC696A/697A only

** : for TC74HC698A/699A only