FAIRCHILD
A Schlumberger Company

μA9708 6-Channel 8-Bit μP Compatible A/D Converter

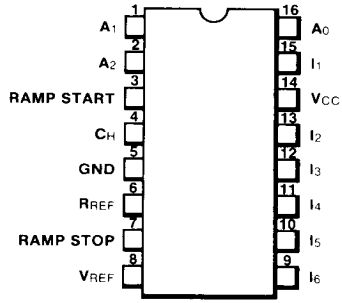
Data Aquisition Products

Description

The μA9708 is a single slope 8-bit, 6-channel ADC subsystem that provides all of the necessary analog functions for a microprocessor-based data control system. The device uses a microprocessor system like the F3870 or F6800 to provide the necessary addressing, timing and counting functions and includes a 1-of-8 decoder, 8-channel analog multiplexer, sample and hold, ramp integrator, precision ramp reference, and a comparator on a single monolithic chip.

- **MPU COMPATIBLE**
- **EXCELLENT LINEARITY OVER FULL TEMPERATURE RANGE ±0.2% MAXIMUM**
- **TYPICAL 300 μs CONVERSION TIME PER CHANNEL**
- **WIDE DYNAMIC RANGE INCLUDES GROUND**
- **AUTO-ZERO AND FULL-SCALE CORRECTION CAPABILITY**
- **RATIOMETRIC CONVERSION—NO PRECISION REFERENCE REQUIRED**
- **SINGLE-SUPPLY OPERATION**
- **TTL COMPATIBLE**
- **DOES NOT REQUIRE ACCESS TO DATA BUS OR ADDRESS BUS**

Connection Diagram
16-Pin DIP

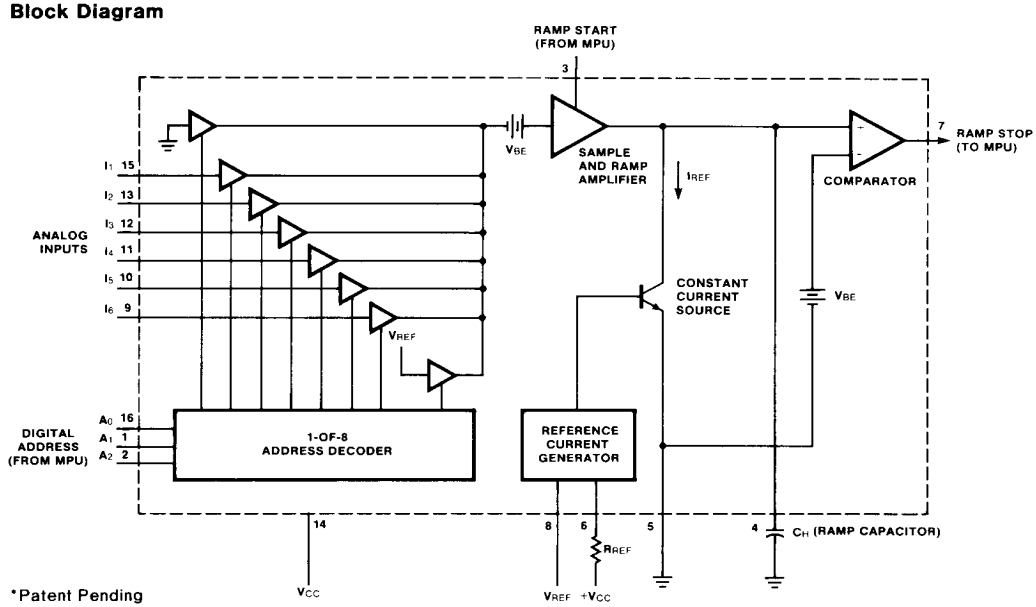


(Top View)

Order Information

Type	Package	Code	Part No.
μA9708	Ceramic DIP	7B	μA9708DM
μA9708	Ceramic DIP	7B	μA9708DC
μA9708	Molded DIP	9B	μA9708PC

Block Diagram



*Patent Pending

Absolute Maximum Ratings

Supply Voltage (V_{CC})	18 V
Comparator Output (Ramp Stop)	−0.3 V to +18 V
Analog Input Range	−0.3 V to 30 V
Digital Input Range	−0.3 V to 30 V
Output Sink Current	10 mA
Operating Temperature Range	
μA9708PC, μA9708DC	0°C to 70°C
μA9708DM	−55°C to 125°C
Storage Temperature Range	−65°C to +150°C
Continuous Total Dissipation	
Ceramic DIP Package	900 mW
Molded DIP Package	1000 mW
Pin Temperature,	
Ceramic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C

Recommended Operating Conditions

Characteristic	Min	Typ	Max	Unit
Supply Voltage (V_{CC})	4.75	5.0	15	V
Reference Voltage (V_{REF})*	2.8		5.25	V
Ramp Capacitor (C_H)	300			pF
Reference Current (I_R)	12		50	μA
Analog Input Range	0		V_{REF}	V
Ramp Stop Output Current			1.6	mA

Note

*$2\ V \leq V_{REF} \leq (V_{CC} - 2\ V)$

Channel Selection

Input Address Line			Selected Analog Input
A_2	A_1	A_0	
0	0	0	Ground
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	V_{REF}

Functional Description

This Analog to Digital Converter is a single-slope 8-bit, 6-channel a/d converter that provides all of the necessary analog functions for a microprocessor-based data/control system. The device uses the processor system to provide the necessary addressing, timing and counting functions and includes a 1-of-8 decoder, 8-channel analog multiplexer, sample and hold, precision current reference, ramp integrator and comparator on a single monolithic chip.

For applications that require auto-zero or auto-calibration, (See *Figures 2-5*) line select address 0, 0, 0 and 1, 1, 1 may be used in conjunction with the arithmetic capability of the microprocessor to provide ground and scaling factors. Address 0, 0, 0 internally connects the input of the ramp generator to ground and may be used for zero offset correction in subsequent conversions. Address 1, 1, 1 internally connects the input of the ramp generator to the voltage reference, V_{REF}, and may be used for scale factor correction in subsequent conversions. For the following, refer to the Functional Block Diagram.

Six separate external analog voltage inputs may come into terminals I_1-I_6 and the specific analog input to be converted is selected via address terminals A_0-A_2. The analog input voltage level is transferred to the external ramp capacitor connected to pin 4 when the input to the ramp start terminal (pin 3) is at a logic 0 (See *Figure 1*). The time to charge the capacitor is the acquisition time which is a function of the output impedance of an amplifier internal to the a/d converter and the value of the capacitor. After charging the external capacitor the ramp start terminal is switched to a logic 1 which introduces a high impedance between the analog input voltage and the external capacitor.

The capacitor begins to discharge at a controlled rate. The controlled rate of discharge (ramp) is established by the external reference voltage, the external reference resistor, the value of the external capacitor and the internal leakage of the a/d converter. Connected to the capacitor terminal is a comparator internal to the a/d converter with its output going to the ramp stop terminal (pin 7). The comparator output is a logic one when the capacitor is charged and switches to a logic 0 when the capacitor is in a discharged state. The ramp time is from the time when ramp start goes HIGH (logic "1") to when ramp stop goes LOW (logic "0"). The microprocessor must be programmed to determine this conversion time. The ideal (no undesirable internal source impedances, leakage paths, errors on levels where comparator switches or delay time) conversion time is calculated as follows:

$$\text{Ramp Time} = V_1 \frac{C_H}{I_R}$$

Where V_1 = Analog Input Voltage being measured

C_H = External Ramp Capacitor

$$I_R = \frac{V_{CC} - V_{REF}}{R_{REF}}$$

Where V_{CC} = Power Supply Voltage

V_{REF} = Reference Voltage

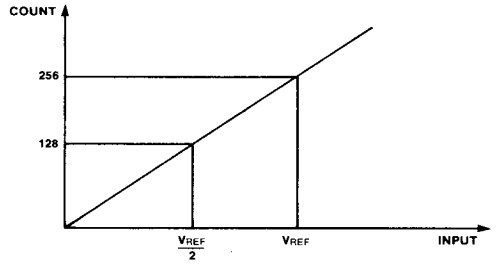
R_{REF} = Reference Resistor

In actual use the errors due to a nonideal a/d converter can be minimized by using a microprocessor to make the calculations. (See *Figures 1* through *4*)

7

Auto-Zero and Full-Scale Features

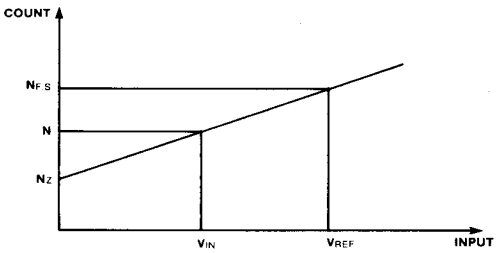
Fig. 1 Ideal Transfer Function



No Zero Offset
No Full-Scale Error

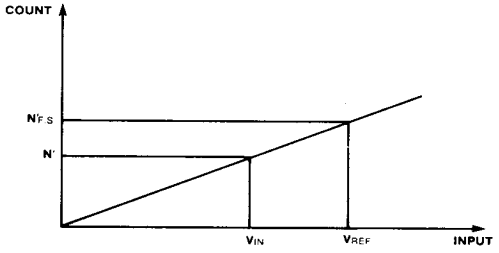
$$\text{Count (n)} = \frac{V_{IN}}{V_{REF}} \times 256$$

Fig. 2 Transfer Function with Zero and Full-Scale Error



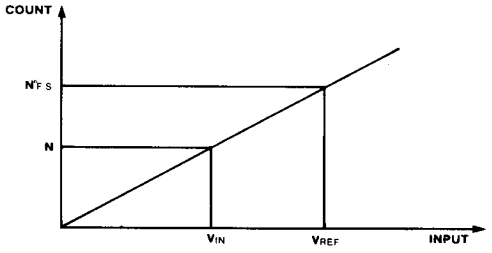
$n_{F.S.} \neq 256$
$n_Z \neq 0$
(n) Has Both Full-Scale and Zero Errors

Fig. 3 Transfer Functions with Zero-Correction Added



$n' = n - n_Z$
n′ Has Full-Scale Error

Fig. 4 Transfer Function with both Zero and Full-Scale Correction Added



$$n'' = (n - n_Z) \times \frac{256}{(n_{F.S.} - n_Z)}$$

Electrical Characteristic Over recommended operating conditions, $-55°C \leq T_A \leq +125°C$, for μA9708DM and $0°C \leq T_A \leq +70°C$ for μA9708DC or μA9708PC; unless otherwise specified.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
E_A	Conversion Accuracy	Over entire temperature range (Note 1)		±0.2	±0.3	%
E_R	Linearity	Applies to any one channel (Note 2)		±0.08	±0.2	%
V_{OSM}	Multiplexer Input Offset Voltage	Channel ON		2.0	4.0	mV
t_C	Conversion Time Per Channel	Analog Input = 0 V to V_{REF} C_H = 300 pF, I_{REF} = 50 μA		296	350	μs
t_A	Acquisition Time	C_H = 1000 pF		20	40	μs
I_A	Acquisition Current		150			μA
t_O	Ramp Start Delay Time			100		ns
t_M	Multiplexer Address Time			1.0		μs
V_{IH}	Digital Input HIGH Voltage	A_0, A_1, A_2, ramp start	2.0			V
V_{IL}	Digital Input LOW Voltage	A_0, A_1, A_2, ramp start			0.8	V
I_B	Analog Input Current	Channel ON or OFF	−3.0	−1.0		μA
I_{IL}	Input LOW Current	A_0, A_1, A_2, ramp start = 0.4 V	−15	−5		μA
I_{IH}	Input HIGH Current	A_0, A_1, A_2, ramp start = 5.5 V			1.0	μA
I_{OS}	Input Offset Current			1.0	3.0	μA
I_{OH}	Comparator Logic "1" Output Leakage Current	V_{OH} = 15 V			10	μA
V_{OL}	Comparator Logic "0" Output Voltage	I_{OL} = 1.6 mA			0.4	V
PSRR	Power Supply Rejection Ratio	(Note 3)	40			dB
	Cross Talk Between Any Two Channels	(Note 4)	60			dB
I_{CC}	Power Supply Current	V_{CC} = 5 V to 15 V, I_O = 0		7.5	15	mA
C_{IN}	Input Capacitance			3.0		pF
C_{OUT}	Comparator Output Capacitance			5.0		pF

7

Notes

1. Conversion accuracy is defined as the deviations from a straight line drawn between the points defined by channel address 000 (0 scale) and channel address 111 (full scale) for all channels.
2. Linearity is defined as the deviation from a straight line drawn between the 0 and full scale points for each channel.
3. Power supply rejection ratio is defined as the conversion error contributed by power supply voltage variations while resolving mid scale on any channel.
4. Cross Talk between channels = $20 \log \frac{\Delta V_{CH}}{\Delta V_I}$

Test Circuits

Fig. 1 Equivalent Timing Waveform for Test Circuits and Applications

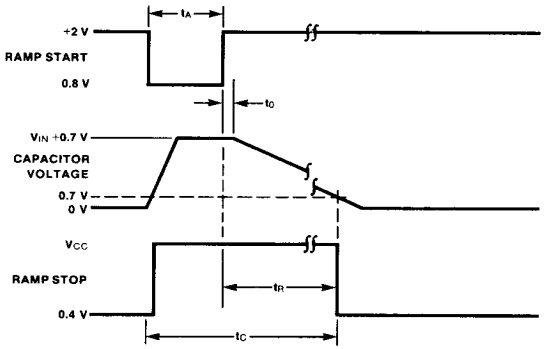
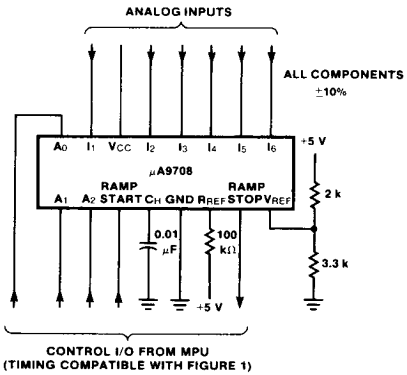


Fig. 2 Slow Speed Evaluation Circuit for Ratiometric Operation



Input Timing:

$t_A > 400\ \mu s$

$$V_{REF} = \left(\frac{3.3\ k\Omega}{2\ k\Omega + 3.3\ k\Omega}\right) 5\ V = 3.1$$

$$I_R = \frac{5\text{-}3.1}{100\ k\Omega} = 19\ \mu A$$

$$t_R|_{max} = \text{full scale ramp time}$$

$$= \frac{0.01 \times 10^{-6}}{19 \times 10^{-6}} \times 3.1 = 1.6\ ms$$

Note

For evaluation purposes, the ramp start timing generation can be implemented with a μA555 timer (astable operation) or MPU evaluation kit, and a time interval meter for ramp time measurement. The TIM meter will measure the time between the 0 to 1 transition of the ramp start and the 1 to 0 transition of the ramp stop. The ramp stop is open collector, and must have an external pull-up resistor to V_{CC}.

Fig. 3 Linearity/Acquisition Time/Conversion Time Test Circuit

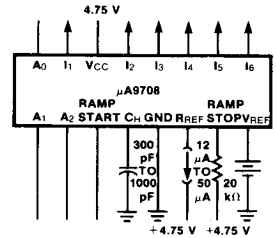
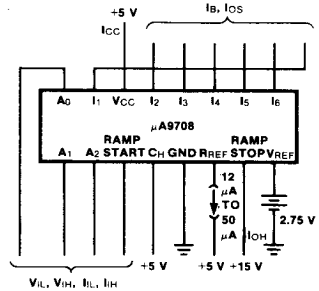


Fig. 4 Static Measurements



Typical Applications

Application Suggestions and Formulas

1. The capacitor node impedance is approximately 30 μΩ and should have no parallel resistance for proper operation.
2. t_R when $V_{IN} = 0$ V will be finite (i.e., the comparator will always toggle for $V_{IN} \geq 0$ V).
3. The ramp stop output is open collector, and an external pull-up resistor is required.
4. All digital inputs and outputs are TTL compatible.
5. For proper operation, timing commences on the 0 to 1 transition of ramp start and terminates on the 1 to 0 transition of ramp stop.
6. $t_A \geq \dfrac{C_H}{150\ \mu A - I_R} \times V_{REF}$
7. t_R (ramp time) $= \dfrac{C_H}{I_R} \times V_{IN}$, $t_R|_{max} = \dfrac{C_H}{I_R} \times V_{REF}$
8. $I_R = \dfrac{V_{CC} - V_{REF}}{R_{REF}}$
9. $2\ V \leq V_{REF} \leq (V_{CC} - 2\ V)$
10. Address lines A_0, A_1, A_2 must be stable throughout the sampling interval, t_A.
11. Pin 6 (R_{REF}) should be bypassed to ground via a 0.02 μF capacitor

Typical Applications (Cont.)

Microprocessor Considerations

Several alternatives exist from a hardware/software standpoint in microprocessor based systems using the μA9708.

1. The ramp time measurement may be implemented in software using a register increment, followed by a branch back depending on the status of the ramp stop.

2. Alternately, the ramp stop may be tied into the interrupt structure in systems containing a programmable binary timer. This scheme has the following advantages:

   a. The CPU is not committed during the ramp time interval.
   b. It requires only 4 bits of an I/O port for control signals.

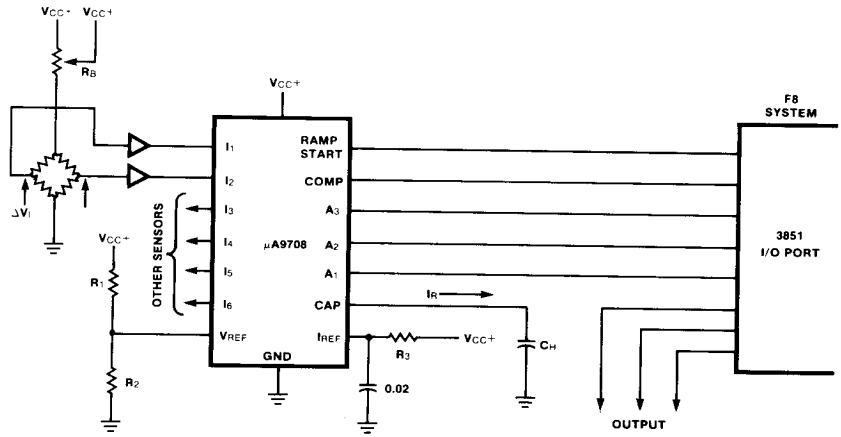
3. The auto-zero/auto-full-scale (see *Figures 2-5*) should use double precision, rounded (as opposed to truncated) arithmatics. Several points are worth noting:

   a. The subtractions are single op code instructions.
   b. The full scale correction uses a multiply by 256 and can be accomplished by a shift left 8 bits (usually one instruction) or placing $(n - n_Z)$ in the MSB register and setting the LSB register to zero, for the double precision divide.
   c. The divisor $(n_{F.S.} - n_Z)$ of the MSB register will always be zero.

These schemes have the following advantages:

   a. No access to the data bus or address bus is required, by the a/d system.
   b. 4 I/O bits completely support the a/d system.
   c. Since auto full scale/auto zero are implemented in software and long term drift (aging) effects are eliminated.
   d. Software overhead is minimal (typically 30 bytes).
   e. Where ratiometric operation is permissible, the 4 external components may be ±5% tolerance, including the power supply.

Fig. 1 Ratiometric Strain Gage Sensor/Controller

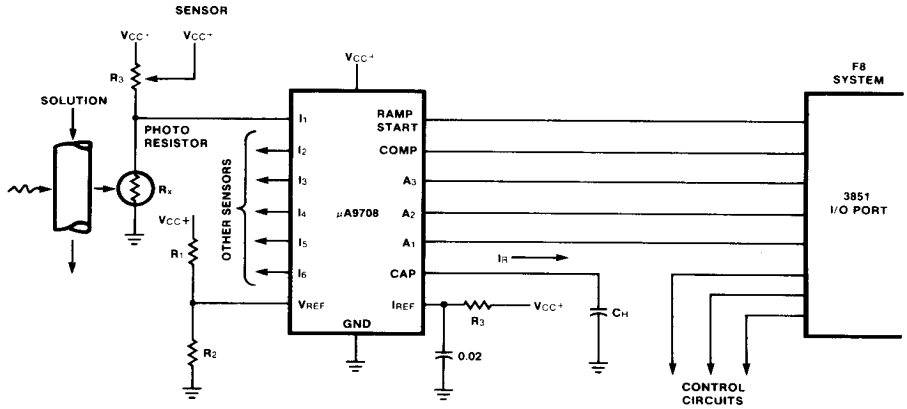


Note

ΔV_I = (Applied Force) and can be Linearized (if necessary) in F8 Software.

Typical Applications (Cont.)

Fig. 2 Opaque Solution Controller



Applications

Beverage Brewers/Dispensers
Chemical Solution Control
Automatic Liquid Mixing Control

$$\text{Ramp Current} = I_R = V_{CC}\left(\frac{R_1}{R_1 + R_2}\right)\left(\frac{1}{R_3}\right)$$

$$V_I = \left(\frac{R_X}{R_X + R_B}\right) V_{CC+}$$

$$\text{Ramp Time} = V_I\left(\frac{C_H}{I_R}\right) = \left(\frac{R_X}{R_X + R_B}\right)\left(1 + \frac{R_2}{R_1}\right)\left(C_H R_3\right)$$