Integrated Device Technology, Inc.

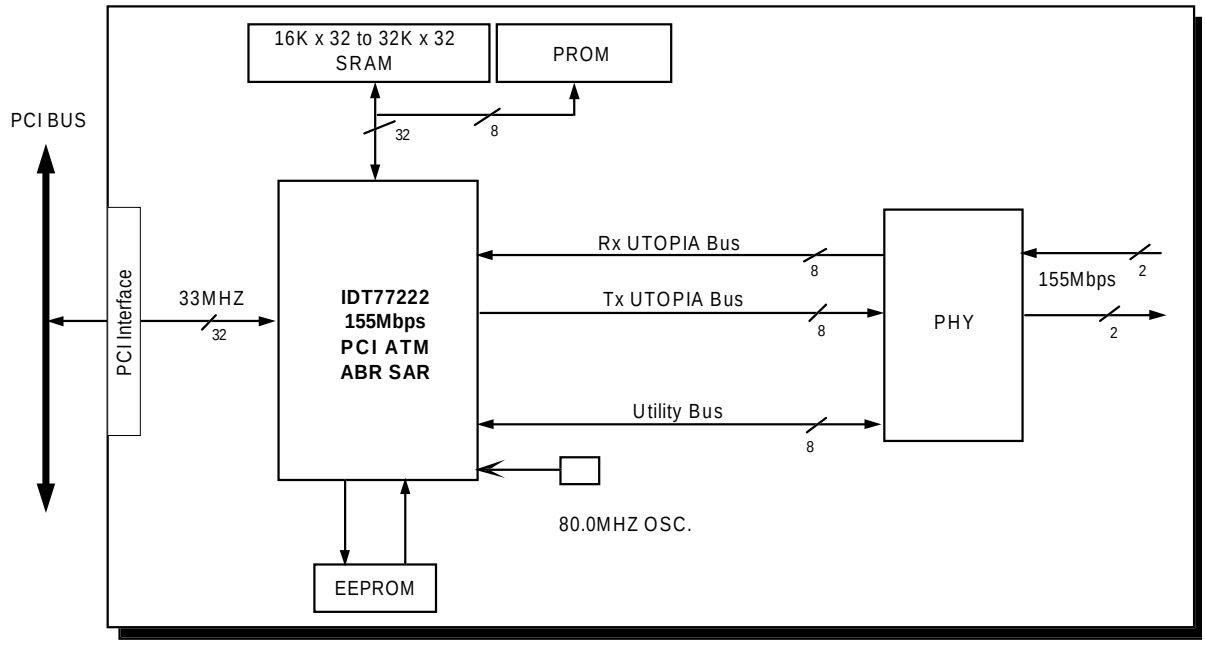
155 Mbps ATM SAR CONTROLLER WITH ABR SUPPORT FOR PCI-BASED NETWORKING APPLICATIONS

PRELIMINARY INFORMATION
IDT77222

KEY FEATURES

- Full-duplex Segmentation and Reassembly (SAR) at 155 Mbps "wire-speed" (310 Mbps aggregate speed).
- Performs ATM layer protocol functions.
- Supports AAL5, AAL3/4, AAL0 and Raw Cell formats.
- Supports Constant Bit Rate (CBR), Variable Bit Rate (VBR), and Unassigned Bit Rate (UBR), and Available Bit Rate (ABR) service classes.
- Segments and reassembles CS-PDUs into host memory.
- Four buffer pools for independent or chained reassembly
- PCI 2.1 compliant.
- Operates with ATM networks up to 155.52 Mbps.
- Up to 256 active transmit connections.
- Up to 256 active receive connections.
- UTOPIA Level 1 Interface to PHY.
- Utility & Management Interface to PHY.
- Stand-alone controller: embedded processor not required.
- Supports high-performance, lowest-cost ATM NIC solution.
- Supports any buffer alignment condition.
- Supports Big and Little Endian data transfers.
- Free Bufffer Queues mapped into PCI memory space.
- Configurable transmit FIFO depth for reduced latency.
- Null cell disable option during transmit.
- Supports greater local memory size.
- Large Rx FIFO size (configurable to 1024 Kbytes).
- Meets Power Management specification.
- Automatic AAL5 padding.
- UNI 3.1, TM 4.0 compliant.
- Pin compatible with IDT 77211 SAR

SYSTEM-LEVEL FUNCTIONAL BLOCK DIAGRAM



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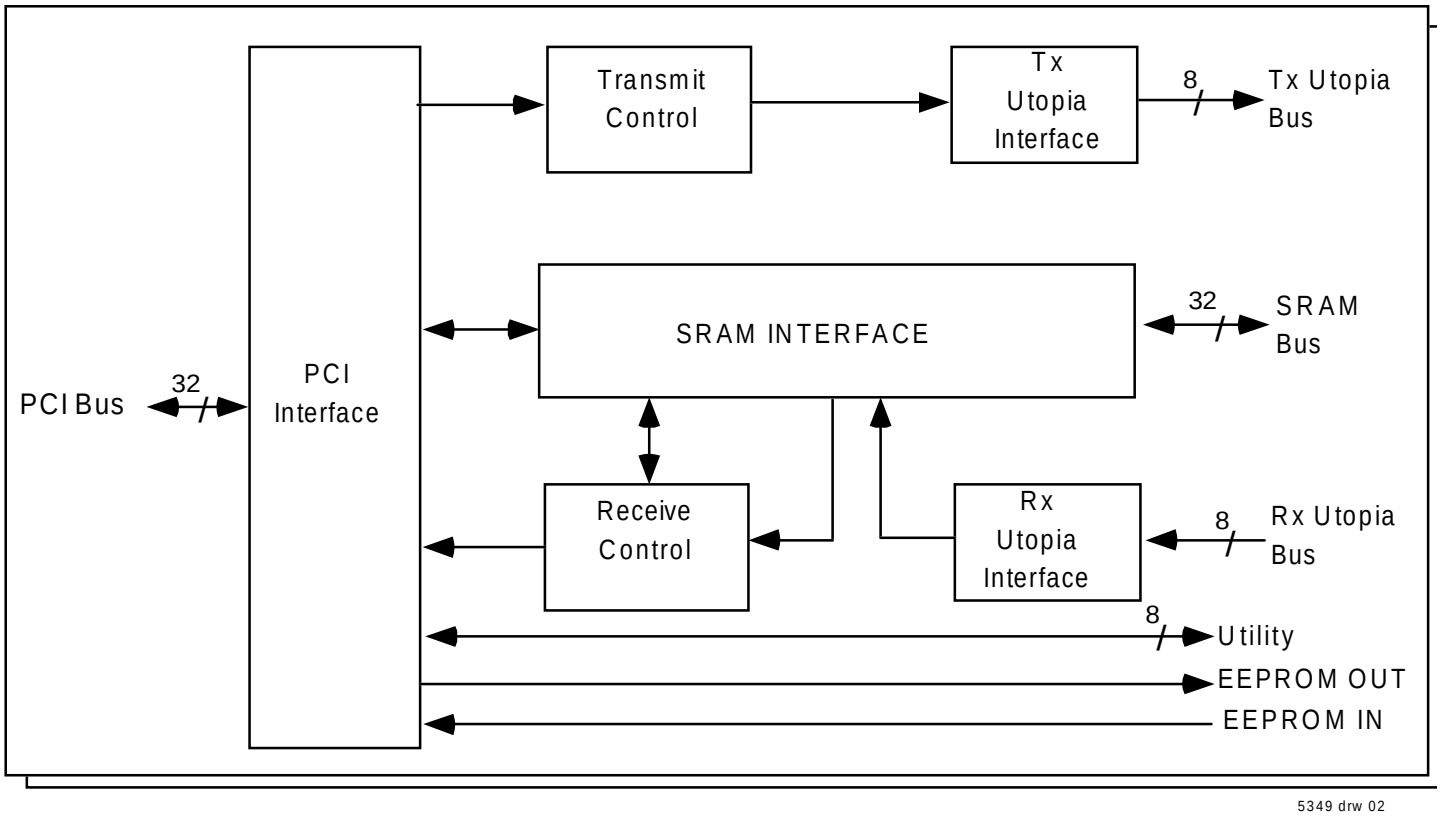
DESCRIPTION

The IDT77222 is a member of IDT's family of SAR products for Asynchronous Transfer Mode (ATM) networks. The IDT77222 performs both the ATM Adaptation Layer (AAL) Segmentation and Reassembly (SAR) function and the ATM layer protocol functions.

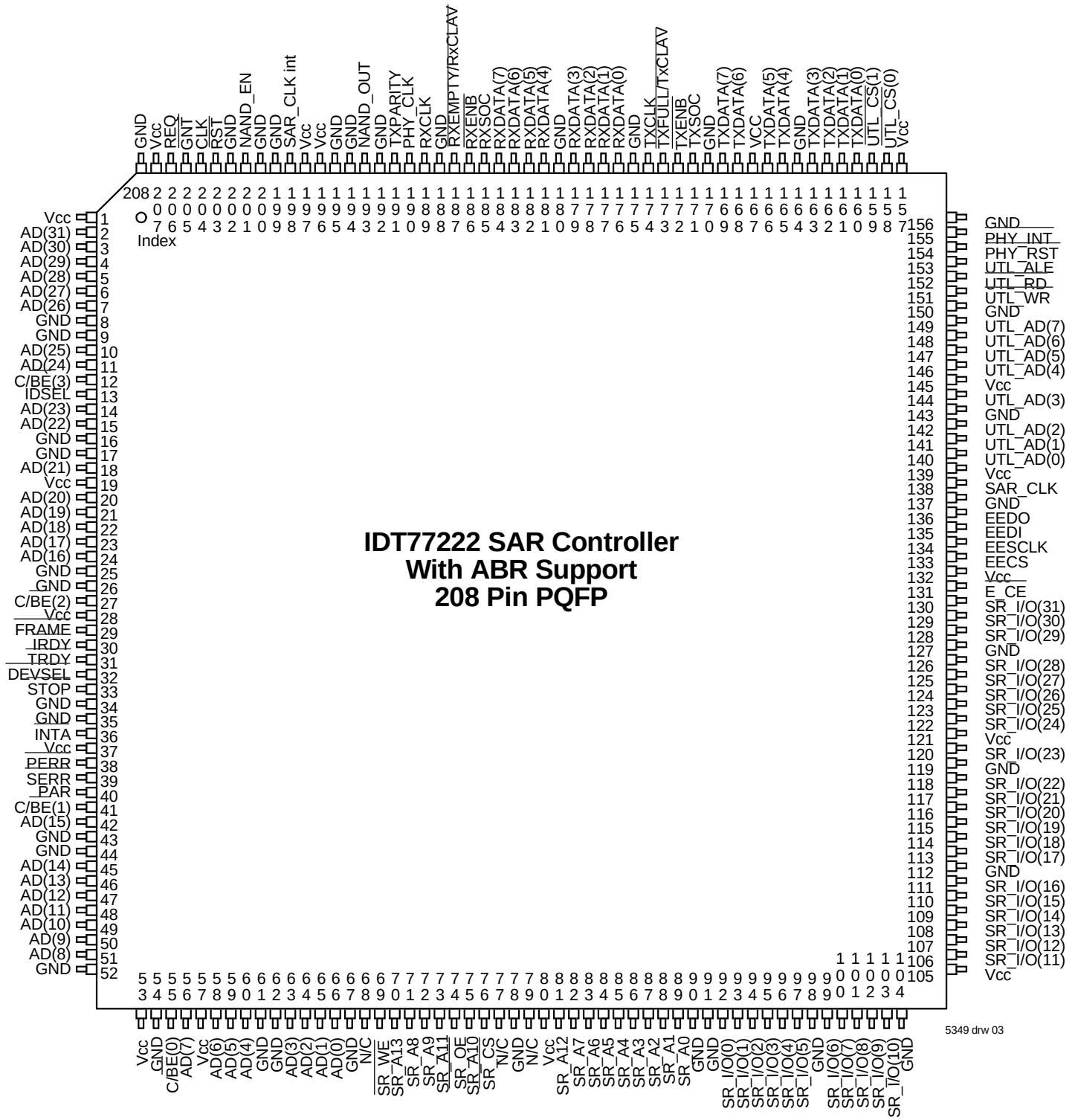
A Network Interface Card (NIC) or internetworking product based on the IDT77222 uses host memory, rather than local memory, to reassemble Convergence Sublayer Protocol Data Units (CS-PDUs) from ATM cell payloads received from the network. When transmitting, as CS-PDUs become ready, they are queued in host memory and segmented by the IDT77222 into ATM cell payloads. From this, the IDT77222 then creates complete 53-byte ATM cells which are sent through the network. The IDT77222's on-chip PCI bus master interface provides efficient, low latency DMA transfers with the host system, while its UTOPIA interface provides direct connection to PHY components used in 25.6 Mbps to 155 Mbps ATM networks.

The IDT77222 is fabricated using state-of-the-art CMOS technology, providing the highest levels of integration, performance and reliability, with the low-power consumption characteristics of CMOS.

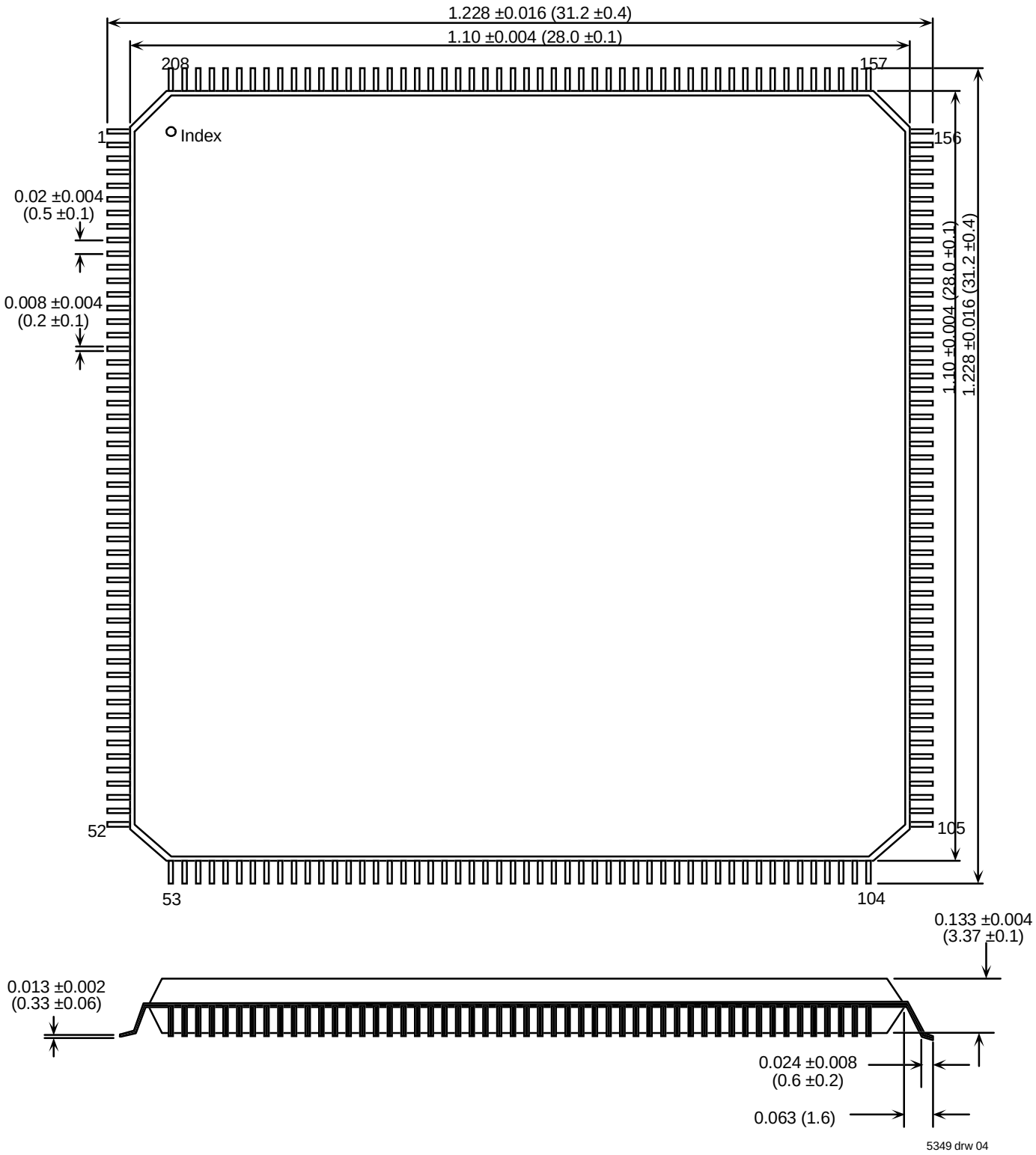


Block Diagram of the IDT77222

PACKAGE PINOUT



PACKAGE DRAWING



PIN DEFINITIONS

Pin #	Name	I/O	Bus Name	Description
1	VCC	I	power	
2	AD(31)	I/O	PCI	address/data line
3	AD(30)	I/O	PCI	address/data line
4	AD(29)	I/O	PCI	address/data line
5	AD(28)	I/O	PCI	address/data line
6	AD(27)	I/O	PCI	address/data line
7	AD(26)	I/O	PCI	address/data line
8	GND	I	power	
9	GND	I	power	
10	AD(25)	I/O	PCI	address/data line
11	AD(24)	I/O	PCI	address/data line
12	$\overline{C/BE(3)}$	I/O	PCI	bus command
13	IDSEL	I	PCI	bus ID select
14	AD(23)	I/O	PCI	address/data line
15	AD(22)	I/O	PCI	address/data line
16	GND	I	power	
17	GND	I	power	
18	AD(21)	I/O	PCI	address/data line
19	VCC	I	power	
20	AD(20)	I/O	PCI	address/data line
21	AD(19)	I/O	PCI	address/data line
22	AD(18)	I/O	PCI	address/data line
23	AD(17)	I/O	PCI	address/data line
24	AD(16)	I/O	PCI	address/data line
25	GND	I	power	
26	GND	I	power	
27	$\overline{C/BE(2)}$	I/O	PCI	bus command
28	VCC	I	power	
29	$\overline{Frame}$	I/O	PCI	cycle frame
30	$\overline{IRDY}$	I/O	PCI	initiator ready
31	$\overline{TRDY}$	I/O	PCI	target ready
32	$\overline{DEVSEL}$	I/O	PCI	target indicating address decode
33	$\overline{STOP}$	I/O	PCI	target requesting master to stop
34	GND	I	power	
35	GND	I	power	
36	$\overline{INTA}$	O	PCI	"interrupt" "A" "request"
37	VCC	I	power	
38	$\overline{PERR}$	I/O	PCI	data parity error
39	$\overline{SERR}$	O	PCI	system error
40	PAR	I/O	PCI	parity (for AD[0:31] and C/BE[0:3])
41	$\overline{C/BE(1)}$	I/O	PCI	bus command
42	AD(15)	I/O	PCI	address/data line
43	GND	I	power	
44	GND	I	power	
45	AD(14)	I/O	PCI	address/data line
46	AD(13)	I/O	PCI	address/data line
47	AD(12)	I/O	PCI	address/data line
48	AD(11)	I/O	PCI	address/data line

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PIN DEFINITIONS (CON'T.)

Pin #	Name	I/O	Bus Name	Description
49	AD(10)	I/O	PCI	address/data line
50	AD(9)	I/O	PCI	address/data line
51	AD(8)	I/O	PCI	address/data line
52	GND	I	power	
53	VCC	I	power	
54	GND	I	power	
55	C/$\overline{BE}$(0)	I/O	PCI	bus command
56	AD(7)	I/O	PCI	address/data line
57	VCC	I	power	
58	AD(6)	I/O	PCI	address/data line
59	AD(5)	I/O	PCI	address/data line
60	AD(4)	I/O	PCI	address/data line
61	GND	I	power	
62	GND	I	power	
63	AD(3)	I/O	PCI	address/data line
64	AD(2)	I/O	PCI	address/data line
65	AD(1)	I/O	PCI	address/data line
66	AD(0)	I/O	PCI	address/data line
67	GND	I	power	
68	N/C			No connect
69	$\overline{SR\_WE}$	O	SRAM	Write enable
70	SR_A13	O	SRAM	Address line
71	SR_A8	O	SRAM	Address line
72	SR_A9	O	SRAM	Address line
73	SR_A11	O	SRAM	Address line
74	$\overline{SR\_OE}$	O	SRAM	Output Enable control
75	SR_A10	O	SRAM	Address line
76	$\overline{SR\_CS}$	O	SRAM	Chip Select
77	N/C			No connect
78	GND	I	power	
79	N/C			No connect
80	VCC	I	power	
81	SR_A12	O	SRAM	Address line
82	SR_A7	O	SRAM	Address line
83	SR_A6	O	SRAM	Address line
84	SR_A5	O	SRAM	Address line
85	SR_A4	O	SRAM	Address line
86	SR_A3	O	SRAM	Address line
87	SR_A2	O	SRAM	Address line
88	SR_A1	O	SRAM	Address line
89	SR_A0	O	SRAM	Address line
90	GND	I	power	
91	GND	I	power	
92	SR_I/O(0)	I/O	SRAM	Data input/output line
93	SR_I/O(1)	I/O	SRAM	Data input/output line
94	SR_I/O(2)	I/O	SRAM	Data input/output line
95	SR_I/O(3)	I/O	SRAM	Data input/output line
96	SR_I/O(4)	I/O	SRAM	Data input/output line

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PIN DEFINITIONS (CON'T.)

Pin #	Name	I/O	Bus Name	Description
97	SR_I/O(5)	I/O	SRAM	Data input/output line
98	GND	I	power	
99	SR_I/O(6)	I/O	SRAM	Data input/output line
100	SR_I/O(7)	I/O	SRAM	Data input/output line
101	SR_I/O(8)	I/O	SRAM	Data input/output line
102	SR_I/O(9)	I/O	SRAM	Data input/output line
103	SR_I/O(10)	I/O	SRAM	Data input/output line
104	GND	I	power	
105	Vcc	I	power	
106	SR_I/O(11)	I/O	SRAM	Data input/output line
107	SR_I/O(12)	I/O	SRAM	Data input/output line
108	SR_I/O(13)	I/O	SRAM	Data input/output line
109	SR_I/O(14)	I/O	SRAM	Data input/output line
110	SR_I/O(15)	I/O	SRAM	Data input/output line
111	SR_I/O(16)	I/O	SRAM	Data input/output line
112	GND	I	power	
113	SR_I/O(17)	I/O	SRAM	Data input/output line
114	SR_I/O(18)	I/O	SRAM	Data input/output line
115	SR_I/O(19)	I/O	SRAM	Data input/output line
116	SR_I/O(20)	I/O	SRAM	Data input/output line
117	SR_I/O(21)	I/O	SRAM	Data input/output line
118	SR_I/O(22)	I/O	SRAM	Data input/output line
119	GND	I	power	
120	SR_I/O(23)	I/O	SRAM	Data input/output line
121	Vcc	I	power	
122	SR_I/O(24)	I/O	SRAM	Data input/output line
123	SR_I/O(25)	I/O	SRAM	Data input/output line
124	SR_I/O(26)	I/O	SRAM	Data input/output line
125	SR_I/O(27)	I/O	SRAM	Data input/output line
126	SR_I/O(28)	I/O	SRAM	Data input/output line
127	GND	I	power	
128	SR_I/O(29)	I/O	SRAM	Data input/output line
129	SR_I/O(30)	I/O	SRAM	Data input/output line
130	SR_1/O(31)	I/O	SRAM	Data input/output line
131	$\overline{E\_CE}$	O	EPROM	EPROM chip select
132	Vcc	I	power	
133	EECS	O	EEPROM	chip select
134	EESCLK	O	EEPROM	clock
135	EEDI	I	EEPROM	Data input
136	EEDO	O	EEPROM	Data output
137	GND	I	power	
138	SAR_CLK	I		SAR clock input
139	Vcc	I	power	
140	UTL_AD(0)	I/O	Utility	address/data bus
141	UTL_AD(1)	I/O	Utility	address/data bus
142	UTL_AD(2)	I/O	Utility	address/data bus
143	GND	I	power	
144	UTL_AD(3)	I/O	Utility	address/data bus

5349 tbl 03

PIN DEFINITIONS (CON'T.)

Pin #	Name	I/O	Bus Name	Description
145	VCC	I	power	
146	UTL_AD(4)	I/O	Utility	address/data bus
147	UTL_AD(5)	I/O	Utility	address/data bus
148	UTL_AD(6)	I/O	Utility	address/data bus
149	UTL_AD(7)	I/O	Utility	address/data bus
150	GND	I	power	
151	$\overline{\text{UTL\_WR}}$	O	Utility	write control
152	$\overline{\text{UTL\_RD}}$	O	Utility	read control
153	UTL_ALE	O	Utility	address latch enable
154	$\overline{\text{PHY\_RST}}$	O	PHY	rest control
155	$\overline{\text{PHY\_INT}}$	I	PHY	interrupt input from PHY
156	GND	I	power	
157	VCC	I	power	
158	$\overline{\text{UTL\_CS(0)}}$	O	Utility	chip select (0)
159	$\overline{\text{UTL\_CS(1)}}$	O	Utility	chip select (1)
160	TxData(0)	O	UTOPIA	transmit data bit 0
161	TxData(1)	O	UTOPIA	transmit data bit 1
162	TxData(2)	O	UTOPIA	transmit data bit 2
163	TxData(3)	O	UTOPIA	transmit data bit 3
164	GND	I	power	
165	TxData(4)	O	UTOPIA	transmit data bit 4
166	TxData(5)	O	UTOPIA	transmit data bit 5
167	VCC	I	power	
168	TxData(6)	O	UTOPIA	transmit data bit 6
169	TxData(7)	O	UTOPIA	transmit data bit 7
170	GND	I	power	
171	TxSOC	O	UTOPIA	transmit start of cell
172	$\overline{\text{TxEnb}}$	O	UTOPIA	transmit enable control
173	$\overline{\text{TxFull}}$/TxCLAV	I	UTOPIA	transmit buffer full
174	TxCLK	O	UTOPIA	transmit data sync clock
175	GND	I	power	
176	RxData(0)	I	UTOPIA	receive data bit 0
177	RxData(1)	I	UTOPIA	receive data bit 1
178	RxData(2)	I	UTOPIA	receive data bit 2
179	RxData(3)	I	UTOPIA	receive data bit 3
180	GND	I	power	
181	RxData(4)	I	UTOPIA	receive data bit 4
182	RxData(5)	I	UTOPIA	receive data bit 5
183	RxData(6)	I	UTOPIA	receive data bit 6
184	RxData(7)	I	UTOPIA	receive data bit 7
185	RxSOC	I	UTOPIA	receive start of cell
186	$\overline{\text{RxEnb}}$	O	UTOPIA	receive enable control
187	$\overline{\text{RxEmpty}}$/RxCLAV	I	UTOPIA	receive buffer empty
188	GND	I	power	
189	RxClk	O	UTOPIA	receive data sync clock
190	PHY_Clk	I	UTOPIA	Transmit sync clock input
191	TxParity	O	UTOPIA	transmit data parity bit
192	GND	I	power	

5349 tbl 04

PIN DEFINITIONS (CON'T.)

Pin #	Name	I/O	Bus Name	Description
193	NAND_OUT	I	power	NAND output chain
194	GND	I	power	
195	GND	I	power	
196	Vcc	I	power	
197	Vcc	I	power	
198	SAR_CLK int	O		SAR_Clk divided by 3
199	GND	I	power	
200	GND	I	power	
201	NAND_EN	I	power	NAND input chain
202	GND	I	power	
203	$\overline{RST}$	I	PCI	system bus reset
204	CLK	I	PCI	bus clock
205	GNT	I	PCI	bus grant signal from arbiter
206	$\overline{REQ}$	O	PCI	bus request
207	Vcc	I	power	
208	GND	I	power	

5349 tbl 05

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	-0.3	6.5	V
V_{IN}	Input Voltage	V_{SS} - 0.3	V_{CC} + 0.3	V
V_{OUT}	Output Voltage	V_{SS} - 0.3	V_{CC} + 0.3	V
T_{stg}	Storage Temperature	-55	125	deg.C

5349 tbl 06

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5.25	V
V_I	Input Voltage	0	V_{CC}	V
T_A	Operating temperature	0	70	deg.C
titr	Input TTL rise time	—	2	ns
titf	Input TTL rall time	—	2	ns

5349 tbl 07

CLOCKING

Symbol	Parameter	Rate	Min.	Max.	Unit
SAR_CLK	SAR clock input freq.	155Mb/s	77	80	MHz
		25Mb/s	25	80	MHz
PHY_CLK	PHY clock input freq.	155Mb/s	19.44	40	MHz
		25Mb/s	3	40	MHz
PCI_CLK	PCI clock input freq.	33MHz	0	33.3	MHz

5349 tbl 08

CAPACITANCE

Symbol	Parameter	Condition	Min.	Max.	Typical	Unit
C_{IN}	Input Capacitance	except PCI Bus	—	—	4	pF
C_{OUT}	Output Capacitance	all outputs	—	—	6	pF
C_{bid}	Bi-Directional Capacitance	all bi-directional pins	—	—	10	pF
C_{inpci}	PCI Bus Input Capacitance	PCI Bus inputs	—	10	—	pF
C_{clkpci}	PCI Bus Clock Input Capacitance	—	5	12	—	pF
C_{idsel}	PCI Bus ID Select Input Capacitance	—	—	8	—	pF

5349 tbl 09

DC OPERATING CONDITIONS

Symbol	Parameter	Condition	Min.	Max.	Typical	Unit
Vil	Low-level TTL input voltage	—	-0.7V	0.8	—	V
Vih	High-level TTL input voltage	—	2	V_{CC} + 0.2V	—	V
Vol	Low-level TTL output voltage	except PCI Bus	—	0.4	—	V
Vol	PCI Bus Low-level TTL output voltage	PCI Bus voltage	—	0.55	—	V
Voh	High-level TTL output voltage	—	2.4	—	—	V
Iol	Low-level TTL output current: SR_A(18-0)	V_{SS} + 0.4V	12	—	—	mA
Ioh	High-level TTL output current: SR_A(18-0)	2.4V	-4	—	—	mA
Iol	Low-level TTL output current: $\overline{RxEnb}$, RxClk, $\overline{TxSOC}$, TxData (7-0), $\overline{TxEnb}$, TxParity, TxClk, $\overline{WE}$, $\overline{OE}$, $\overline{CS}$, SR_D31-0	V_{SS} + 0.4V	6	—	—	mA
Ioh	High-level TTL output current: $\overline{RxEnb}$, RxClk, TxSoc, TxData7-0, $\overline{TxEnb}$, TxParity, TxClk, $\overline{SR\_WE}$, $\overline{SR}$, $\overline{OE}$, $\overline{SR\_CS}$, SR_I/O(31-0)	2.4V	-2	—	—	mA
Iol	Low-level TTL output current: UTL_AD(7-0), $\overline{UTL\_RD}$, $\overline{UTL\_WR}$, $\overline{UTL\_ALE}$, $\overline{UTL\_CS0/1}$, EESCLK, EECS, EEDO, $\overline{PHY\_RST}$	V_{SS} + 0.4V	3	—	—	mA
Ioh	High-level TTL output current: UTL_AD(7-0), $\overline{UTL\_RD}$, $\overline{UTL\_WR}$, UTL_ALE, $\overline{UTL\_CS0/1}$, EESCLK, EECS, EEDO, $\overline{PHY\_RST}$	2.4V	-1	—	—	mA
Iil	Input leakage current	$V_{SS} \leq V_{IN} \leq$ Vdd	-1	1	—	uA
Ityp	Dynamic Supply Current	—	—	300	250	mA

5349 tbl 10

AC OPERATING CONDITIONS

AC TEST CONDITIONS

Parameter	Non-PCI	PCI
Input Pulse Levels	VSS to 3.0V	VSS to 2.8V
Input Rise/Fall Times	< 7nsec	< 7nsec
Input Timing Ref. Level	1.5V	1.5V
Output Ref. Level	1.5V	1.5V
AC Test Load	Diag. 1 and 2	Diag. 3 and 4

5349 tbl 11

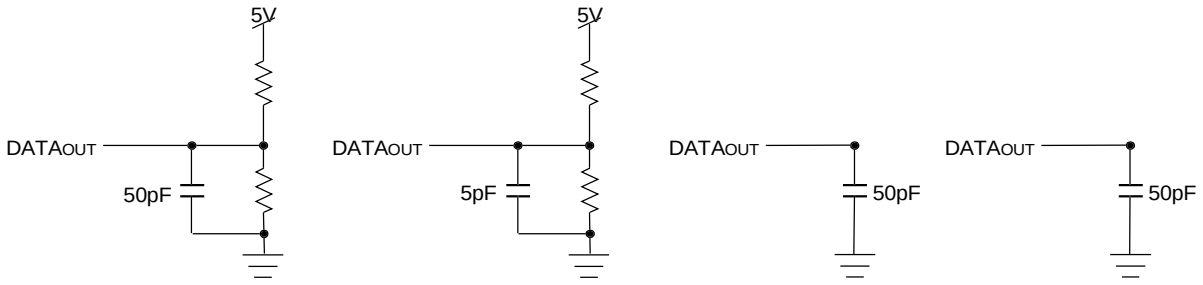

Diagram 1 Diagram 2 Diagram 3 Diagram 4

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PCI BUS (SEE FIGURE 1& 2)

Symbol	Parameter	Min.	Max.	Unit
tval	CLK to Output Signal Valid Delay: AD31-0, C/$\overline{BE}$3-0, PAR, $\overline{FRAME}$, $\overline{IRDY}$, $\overline{DEVSEL}$, $\overline{TRDY}$, $\overline{STOP}$, $\overline{PERR}$, $\overline{SERR}$	2	11	ns
tval(ptp)	CLK to Output Signal Valid Delay: $\overline{REQ}$	2	12	ns
ton	Float to Signal Active Delay: AD31-0, C/$\overline{BE}$3-0, PAR, $\overline{FRAME}$, $\overline{IRDY}$, $\overline{DEVSEL}$, $\overline{TRDY}$, $\overline{STOP}$, $\overline{PERR}$, $\overline{SERR}$	2	—	ns
toff	Signal Active to Float Delay: AD31-0, C/$\overline{BE}$3-0, PAR, $\overline{FRAME}$, $\overline{IRDY}$, $\overline{DEVSEL}$, $\overline{TRDY}$, $\overline{STOP}$, $\overline{PERR}$, $\overline{SERR}$	—	28	ns
tsu	Input Setup Time to CLK: AD31-0, C/$\overline{BE}$3-0, PAR, $\overline{FRAME}$, $\overline{IRDY}$, $\overline{DEVSEL}$, $\overline{TRDY}$, $\overline{STOP}$, $\overline{PERR}$, $\overline{SERR}$, $\overline{GNT}$	7	—	ns
tsu(ptp)	Input Setup Time to CLK: $\overline{GNT}$, ($\overline{REQ}$)	10(12)	—	ns
th	Input Hold Time from CLK: AD31-0, C/$\overline{BE}$3-0, PAR, $\overline{FRAME}$, $\overline{IRDY}$, $\overline{DEVSEL}$, $\overline{TRDY}$, $\overline{STOP}$, $\overline{PERR}$, $\overline{SERR}$, $\overline{GNT}$	0	—	ns
trst-pwr	Reset Active Time After Power Stable	1	—	ns
trst-clk	Reset Active Time After CLK Stable	100	—	ns
trst-off	Reset Active to Output Float Delay: AD31-0, C/$\overline{BE}$3-0, PAR, $\overline{FRAME}$, $\overline{IRDY}$, $\overline{DEVSEL}$, $\overline{TRDY}$, $\overline{STOP}$, $\overline{PERR}$, $\overline{SERR}$	—	40	ns
thigh	Clock high time	11n	—	ns
tlow	Clock low time	11n	—	ns

5349 tbl 12

UTOPIA BUS (SEE FIGURE 3)

Symbol	Parameter	Min.	Max.	Unit
t1	TxClk, RxClk Delay from PHY_CLK	—	5	ns
t2	TxData(7-0), TxSOC, $\overline{\text{TxEnb}}$, TxParity Output Valid from TxClk	1	15	ns
t3	$\overline{\text{TxFull}}$/TxCLAV Setup Time to TxClk	10	—	ns
t4	$\overline{\text{TxFull}}$/TxCLAVHold Time from TxClk	0	—	ns
t5	$\overline{\text{RxEnb}}$ Output Valid from RxClk	1	15	ns
t6	RxData(7-0), RxSOC Setup Time to RxClk	10	—	ns
t7	RxData(7-0), RxSOC Hold Time from RxClk	0	—	ns
t8	$\overline{\text{RxEmpty}}$/RxCLAV Setup Time to RxClk	10	—	ns
t9	$\overline{\text{RxEmpty}}$/RxCLAV Hold Time from TxClk	0	—	ns

5349 tbl 13

UTILITY BUS WRITE CYCLE (SEE FIGURE 4)

Symbol	Parameter	Min.	Max.	Unit
tw1	UTL_ALE Pulse Width	25	—	ns
tw2	$\overline{\text{UTL\_CS0/1}}$ Output Valid to UTL_ALE falling edge	25	—	ns
tw3	$\overline{\text{UTL\_WR}}$ Output Valid from UTL_ALE falling edge	—	80	ns
tw4	$\overline{\text{UTL\_CS0/1}}$ Pulse Width	275	—	ns
tw5	$\overline{\text{UTL\_WR}}$ Pulse Width	185	—	ns
tw6	UTL_ALE falling edge to $\overline{\text{UTL\_CS0/1}}$, $\overline{\text{UTL\_WR}}$ rising edge	245	—	ns
tw7	UTL_AD(7-0) Address Setup Time to UTL_ALE falling edge	30	—	ns
tw8	UTL_AD(7-0) Address Hold Time from UTL_ALE falling edge	10	—	ns
tw9	UTL_AD(7-0) Data Setup Time to $\overline{\text{UTL\_CS0/1}}$, $\overline{\text{UTL\_WR}}$ rising edge	185	—	ns
tw10	UTL_AD(7-0) Data Hold Time from $\overline{\text{UTL\_CS0/1}}$, $\overline{\text{UTL\_WR}}$ rising edge	10	—	ns

5349 tbl 14

UTILITY BUS READ CYCLE (SEE FIGURE 5)

Symbol	Parameter	Min.	Max.	Unit
tr1	UTL_ALE Pulse Width	25	—	ns
tr2	$\overline{\text{UTL\_CS0/1}}$ Output Valid to UTL_ALE falling edge	25	—	ns
tr3	$\overline{\text{UTL\_RD}}$ Output Valid from UTL_ALE falling edge	—	80	ns
tr4	$\overline{\text{UTL\_CS0/1}}$ Pulse Width	275	—	ns
tr5	$\overline{\text{UTL\_RD}}$ Pulse Width	185	—	ns
tr6	UTL_ALE falling edge to $\overline{\text{UTL\_CS0/1}}$, $\overline{\text{UTL\_RD}}$ rising edge	270	—	ns
tr7	UTL_AD(7-0) Address Setup Time to UTL_ALE falling edge	30	—	ns
tr8	UTL_AD(7-0) Address Hold Time from UTL_ALE falling edge	10	—	ns
tr9	UTL_AD(7-0) Data Setup Time to $\overline{\text{UTL\_CS0/1}}$, $\overline{\text{UTL\_RD}}$ rising edge	80	—	ns
tr10	UTL_AD(7-0) Data Hold Time from $\overline{\text{UTL\_CS0/1}}$, $\overline{\text{UTL\_RD}}$ rising edge	10	—	ns

5349 tbl 15

SRAM BUS WRITE CYCLE (SEE FIGURE 6)

Symbol	Parameter	Min.	Max.	Unit
t1	$\overline{SR\_CS}$ falling edge to $\overline{SR\_WE}$ falling edge	0	—	ns
t2	$\overline{SR\_WE}$ rising edge to $\overline{SR\_CS}$ rising edge	0	—	ns
t3	SR_A(18-0) Setup Time to $\overline{SR\_WE}$ falling edge	2	—	ns
t4	SR_A(18-0) Hold Time from $\overline{SR\_CS}$ rising edge	0	—	ns
t5	SR_I/O(31-0) Setup Time to $\overline{SR\_CS}$ rising edge	11	—	ns
t6	SR_I/O(31-0) Setup Time to $\overline{SR\_WE}$ rising edge	11	—	ns
t7	SR_I/O(31-0) Hold Time from $\overline{SR\_CS}$ rising edge	0	—	ns
t8	SR_I/O(31-0) Hold Time from $\overline{SR\_WE}$ rising edge	0	—	ns

5349 tbl 16

SRAM BUS READ CYCLE (SEE FIGURE 7)

Symbol	Parameter	Min.	Max.	Unit
t1	$\overline{SR\_CS}$ falling edge to $\overline{SR\_OE}$ falling edge	0	—	ns
t2	$\overline{SR\_OE}$ rising edge to $\overline{SR\_CS}$ rising edge	0	—	ns
t3	SR_I/O(31-0) Setup Time to $\overline{SR\_OE}$ rising edge	15	—	ns
t4	SR_I/O(31-0) Setup Time from $\overline{SR\_CS}$ rising edge	15	—	ns
t5	SR_I/O(31-0) Hold Time to $\overline{SR\_OE}$ rising edge	0	—	ns
t6	SR_I/O(31-0) Setup Time to $\overline{SR\_CS}$ rising edge	0	—	ns
t7	$\overline{SR\_CS}$ falling edge to SR_A(18-0) Valid	0	—	ns
t8	SR_A(18-0) to SR_I/O(31-0) Valid at SAR_CLK input	—	15	ns

5349 tbl 17

EPROM (SEE FIGURE 8)

Symbol	Parameter	Min.	Max.	Unit
t1	SR_I/O(7-0) Hold Time from $\overline{E\_CE}$ rising edge	0	—	ns
t2	$\overline{E\_CE}$ falling edge to SR_A(18-0) Valid	0	—	ns
t3	$\overline{E\_CE}$ rising edge to SR_A(18-0) Delay	0	—	ns
t4	$\overline{E\_CE}$ Pulse Width	345	—	ns
t5	SR_A(18-0) Change to SR_I/O(7-0) Valid	—	70	ns
t6	SR_A(18-0) to SR_A(18-0) Change	75	—	ns

5349 tbl 18

EEPROM (SEE FIGURE 9)

Symbol	Parameter	Min.	Max.	Unit	Comments
t1	SAR_CLK to Output Signal Valid Delay: EECS, EEDO, EECLK	100	—	ns	software controlled
t2	EEDI Input Setup Time to SAR_CLK	10	—	ns	software controlled
t3	EEDI Input Hold Time from SAR_CLK	0	—	ns	software controlled

5349 tbl 19

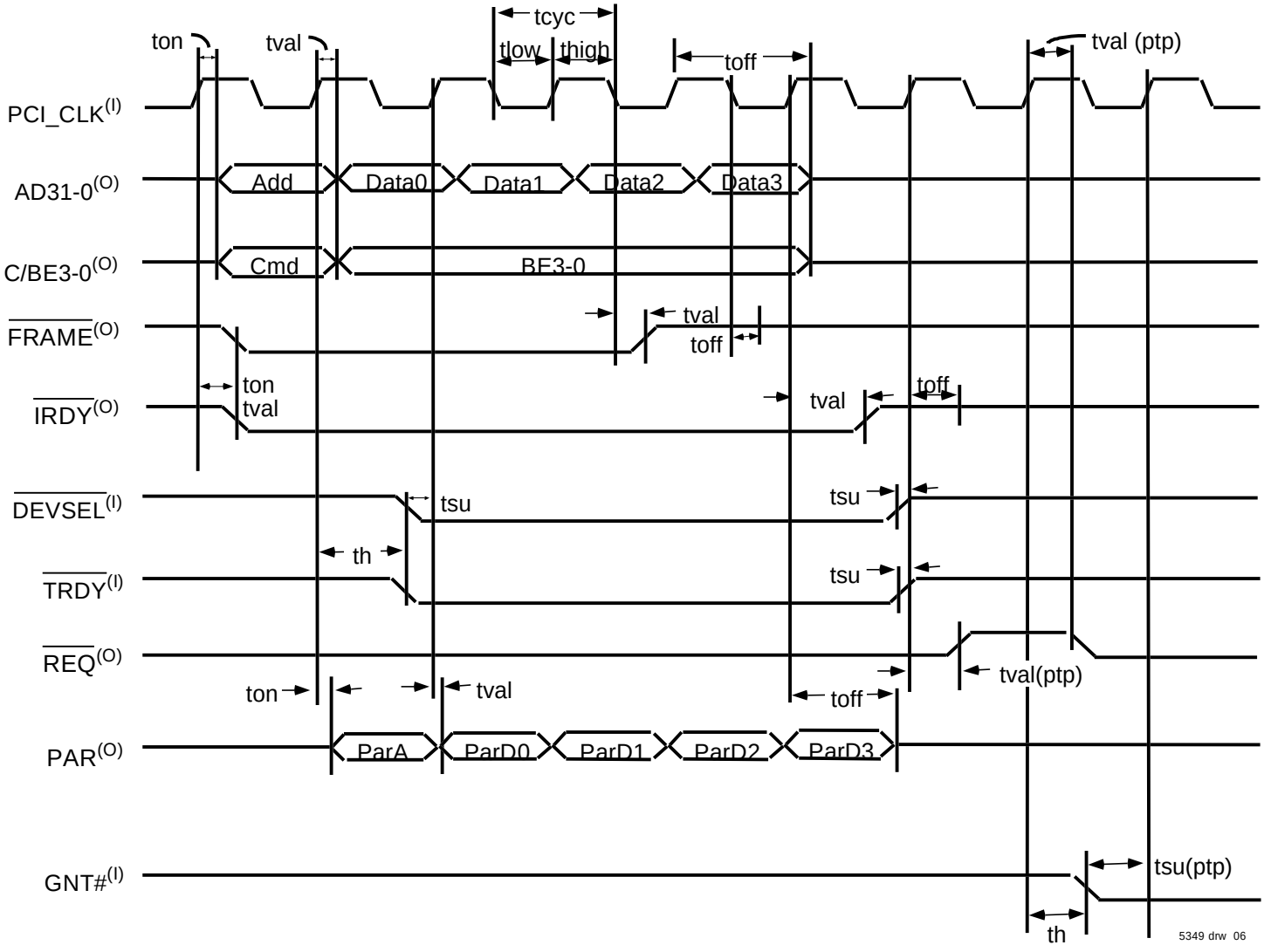


Figure 1. The IDT77222 as a PCI master (illustrates a 4-word write by the IDT77222 to host memory)

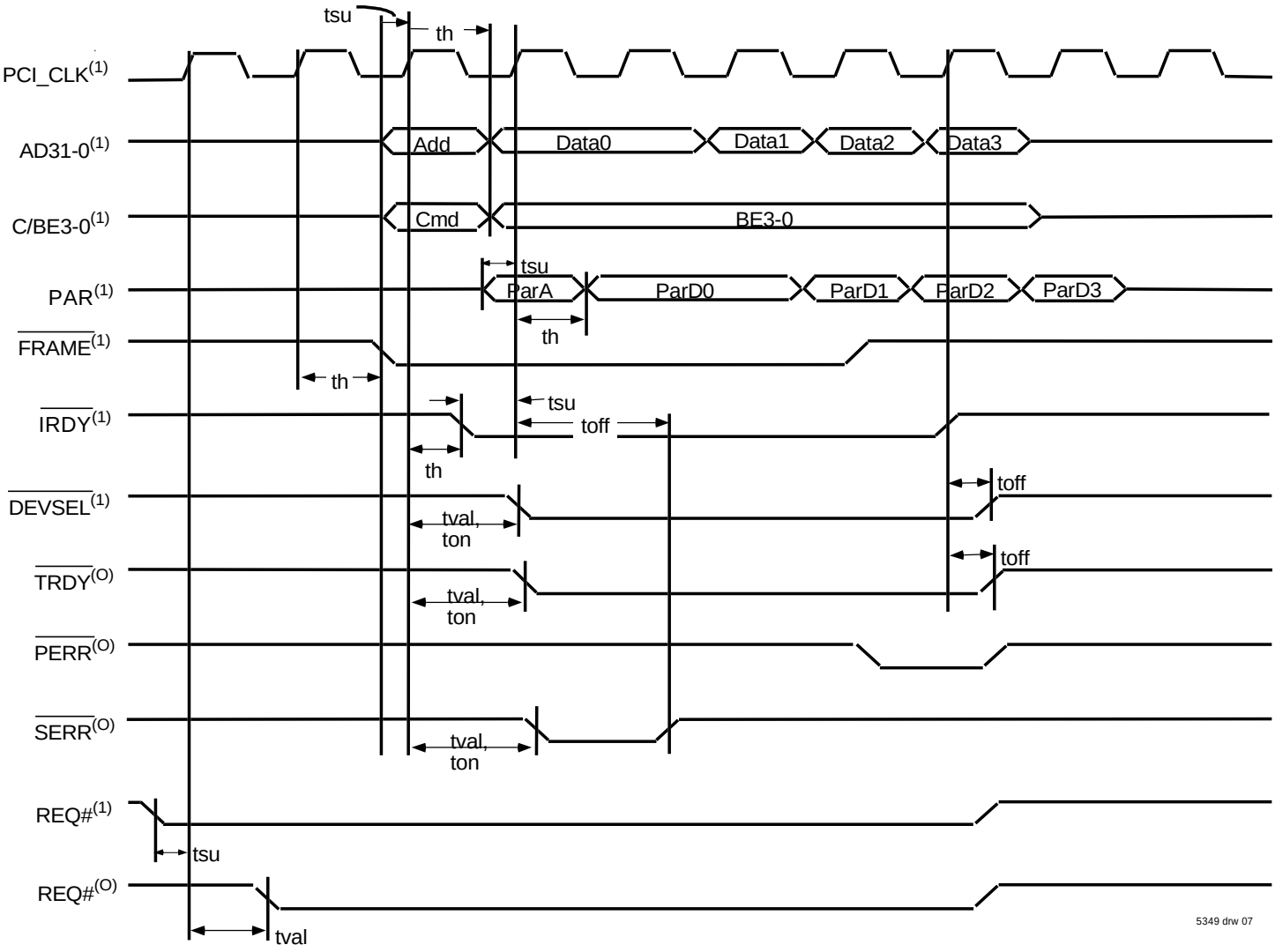


Figure 2. The IDT77222 as a PCI target
(illustrates a 4-word write operation by the host device driver to the IDT77222)

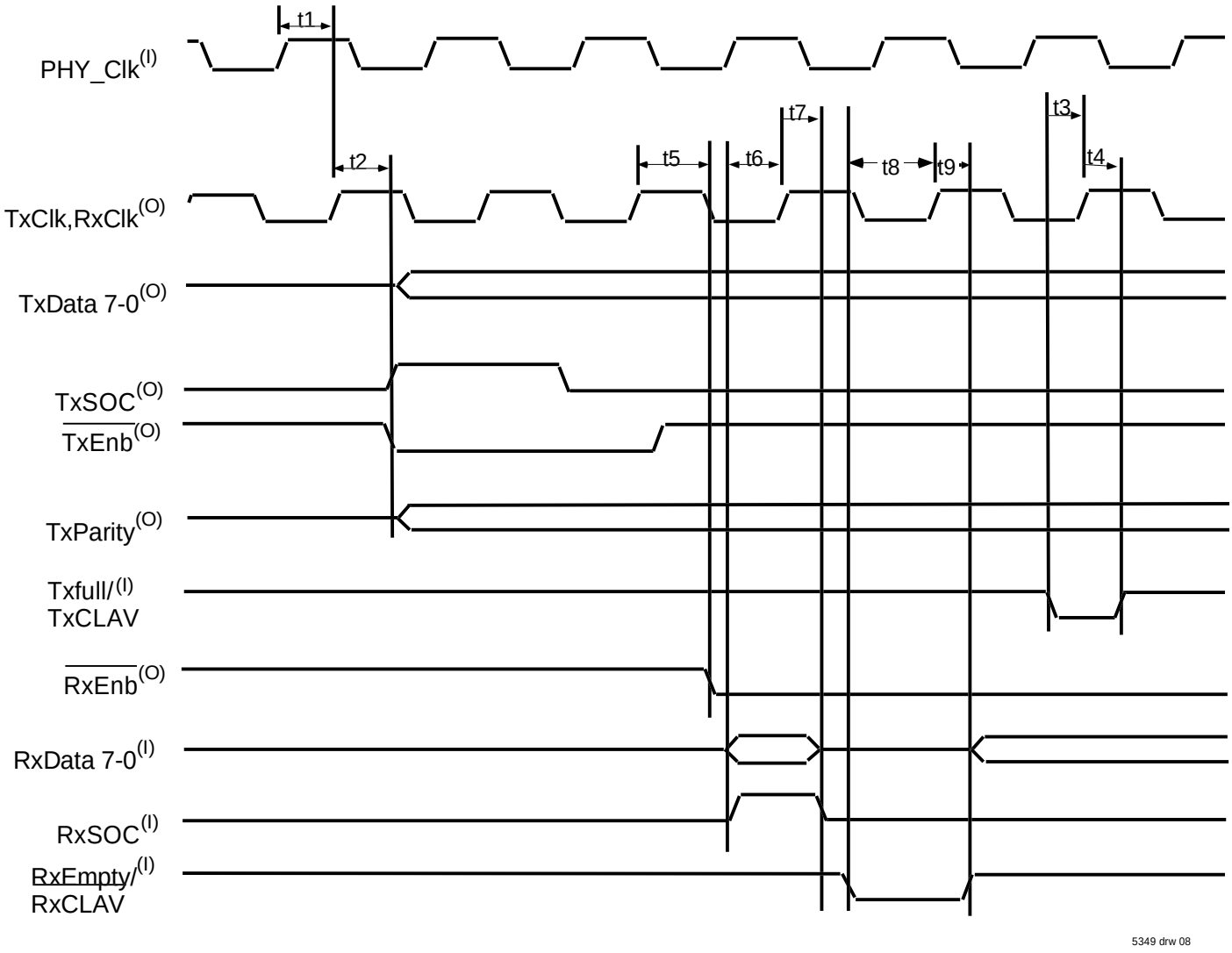


Figure 3. UTOPIA Bus Timing

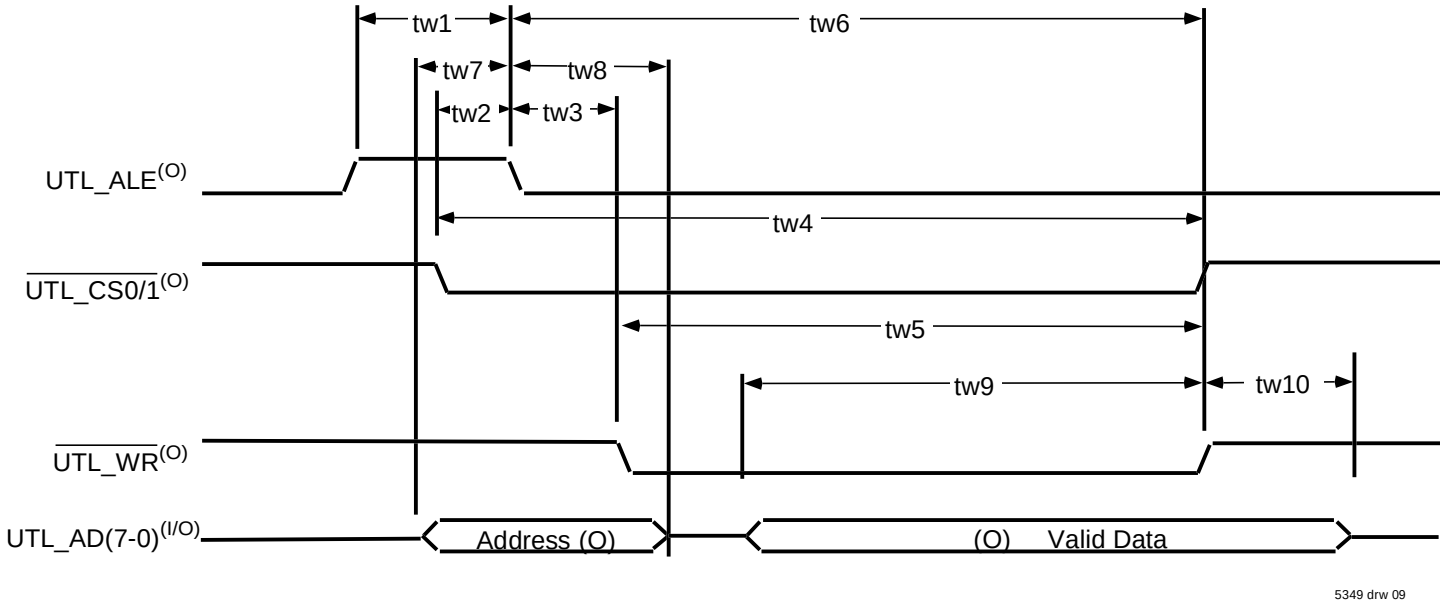


Figure 4. Utility Bus Write Cycle

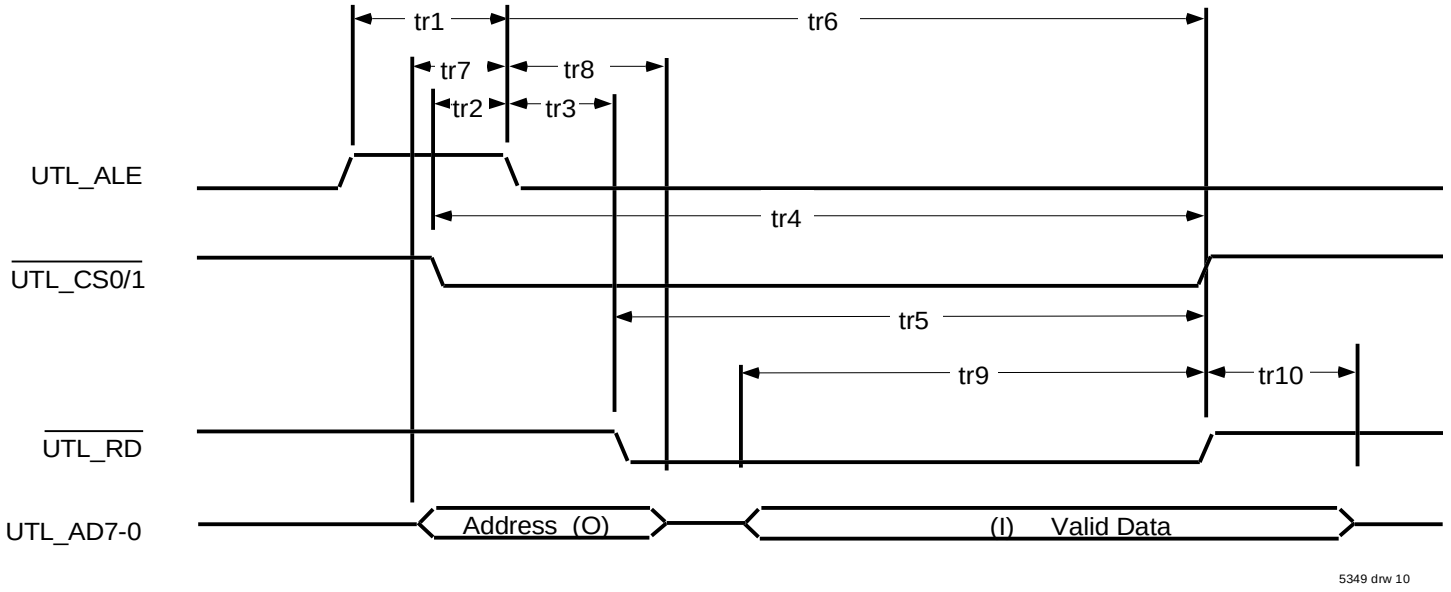


Figure 5. Utility Bus Read Cycle

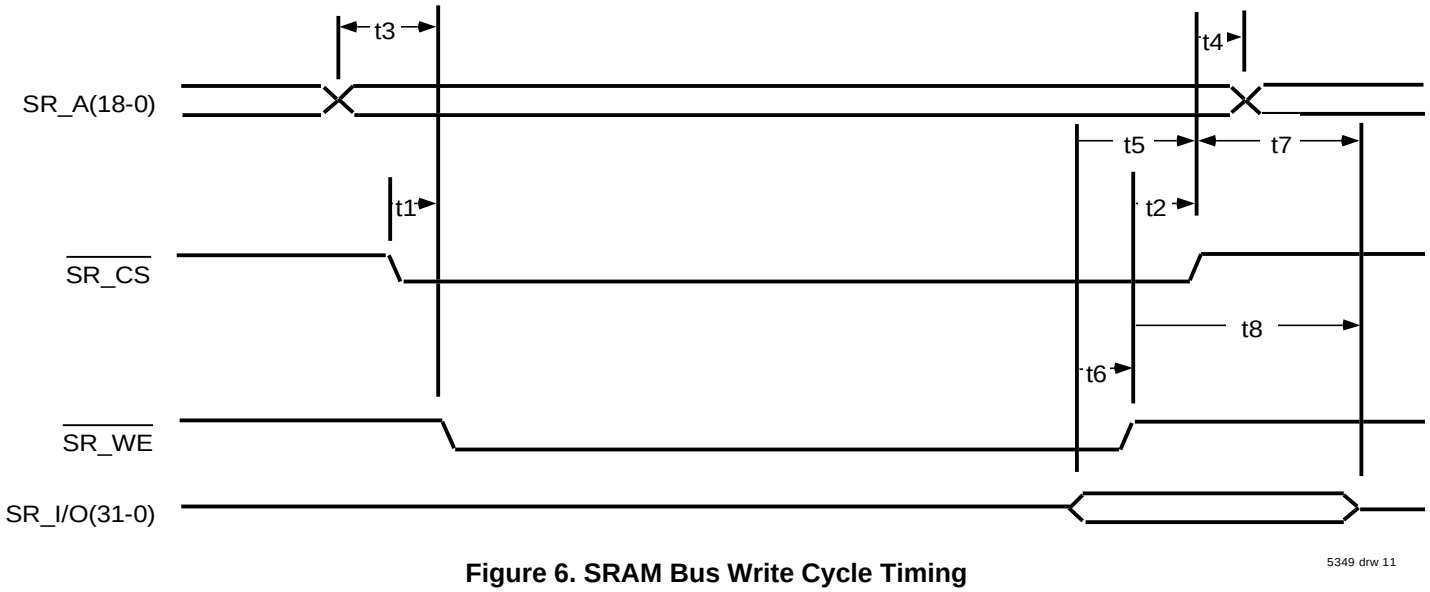


Figure 6. SRAM Bus Write Cycle Timing

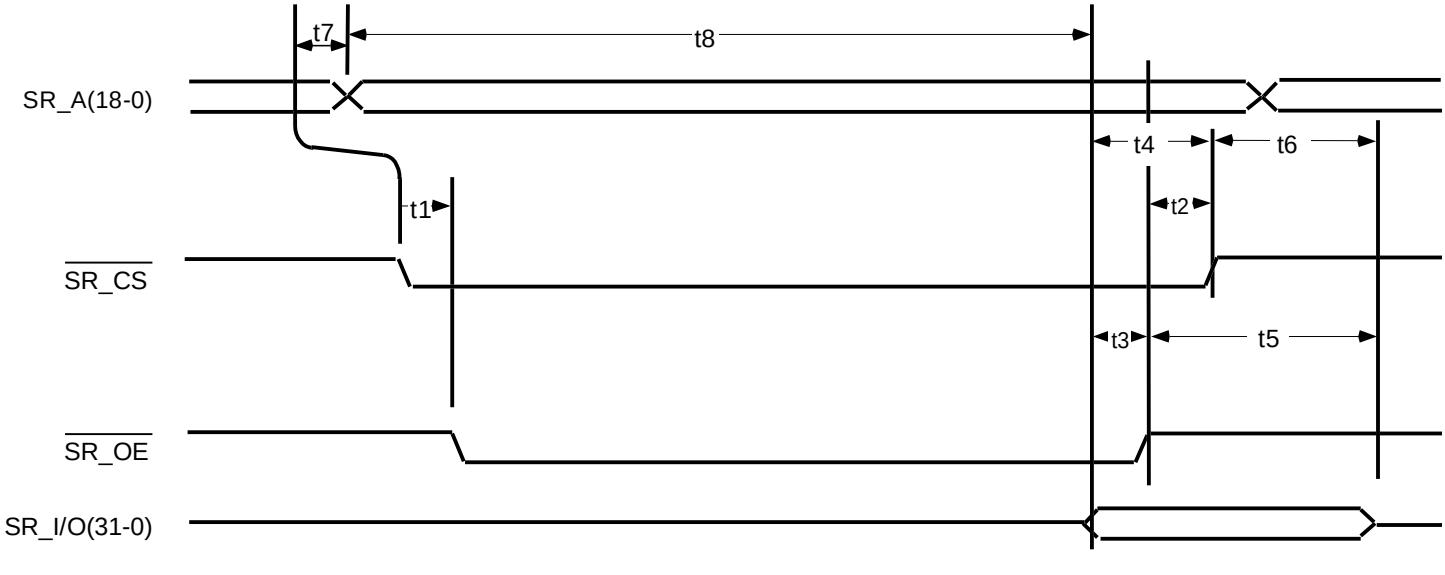


Figure 7. SRAM Bus Read Cycle Timing

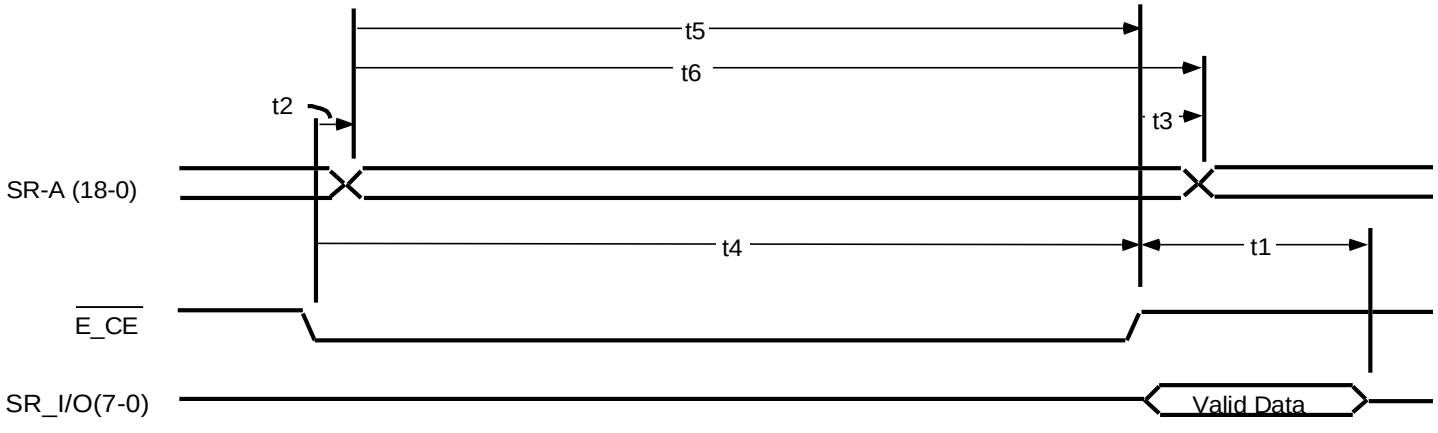


Figure 8. EPROM Timing

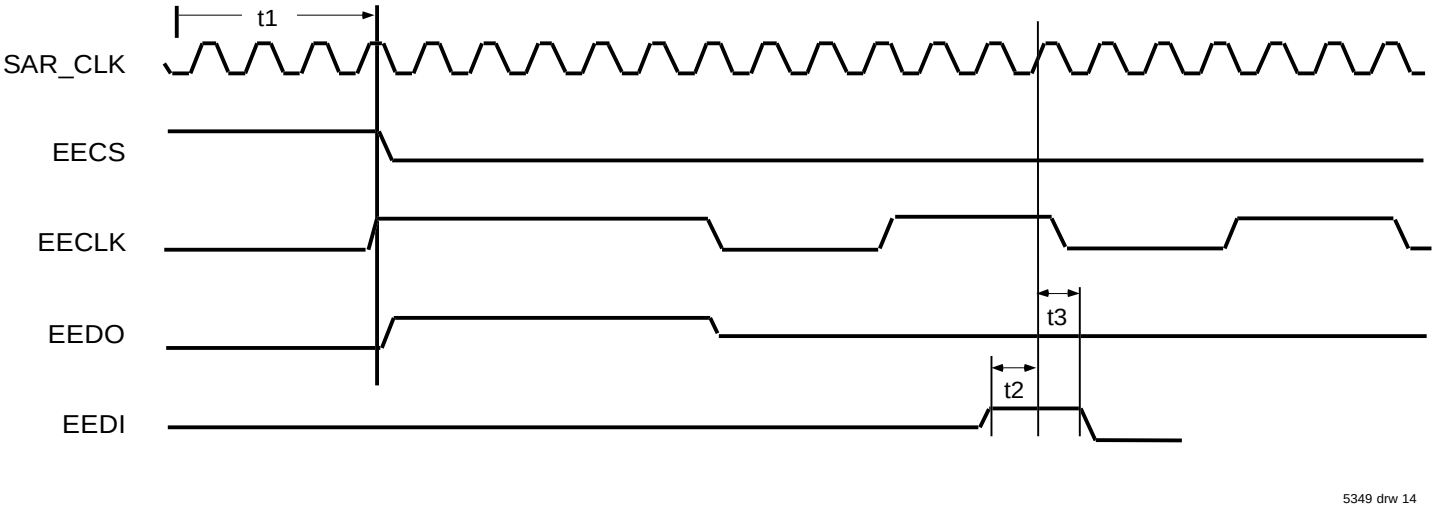
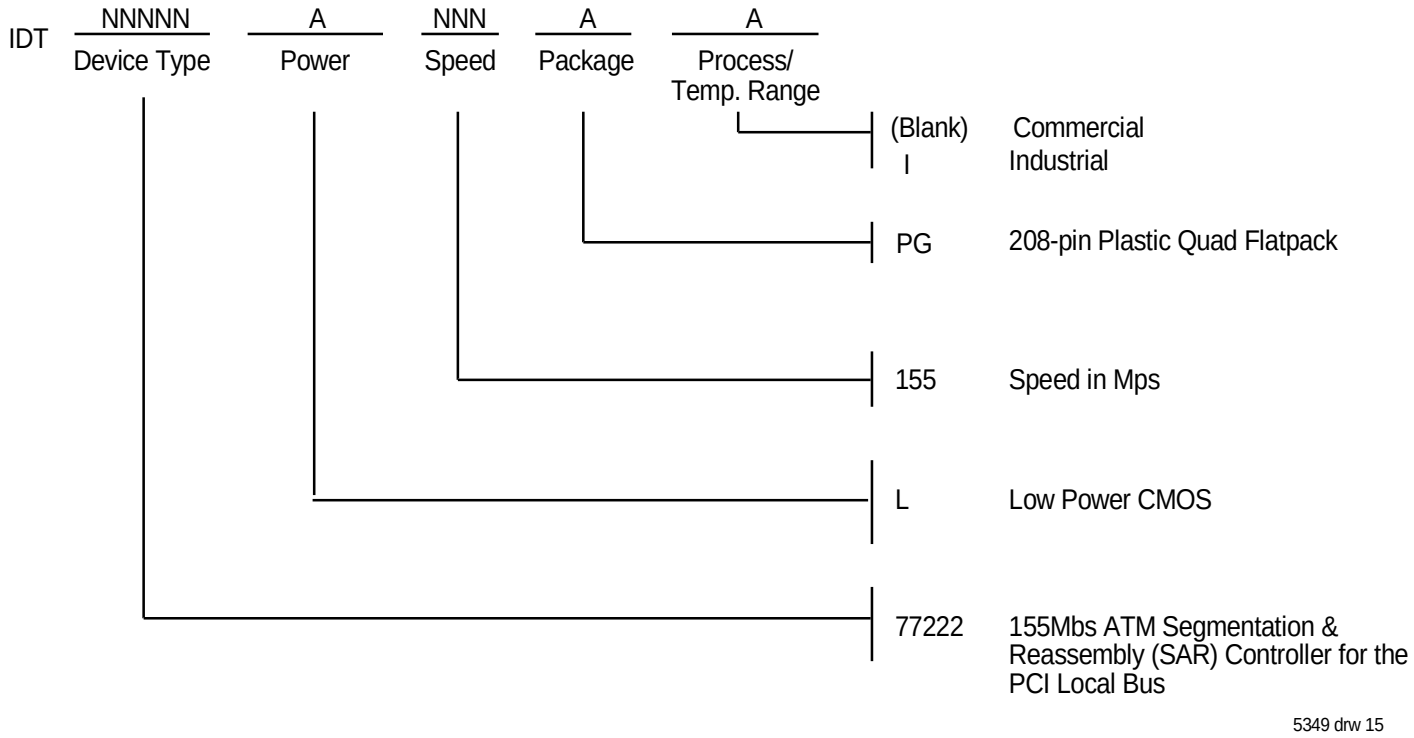


Figure 9. EEPROM Timing

´SOFTWARE AND SOFTWARE DRIVERS

IDT has contracted with several vendors who have writen software drivers for the IDT77222. Please contact your local sales representative for an updated lis, or e-mail atmhelp@idt.com.

ORDERING INFORMATION



Replacing the 77211 with the 77222:

The 77222 PG package is the same package as the 77211 PQF, the 77222 is a direct replacement to the 77211 SAR. To use the 77222 in a 155 Mbps application a 80 MHz oscillator is required (replace the 50 MHz oscillator used with the 77211).

PRELIMINARY DATASHEET: DEFINITION

"PRELIMINARY" datasheets contain descriptions for products that are in early release, including features and block diagrams.

Data Sheet Document History

6/24/98: Created new document
9/15/99: Updated software section

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