4

Electrical Specifications

Sections 4.1 through 4.6 specify the following:

- PCI electrical conformance
- Absolute maximum ratings
- Normal operating conditions
- Supply current and power dissipation
- The dc and ac specifications

4.1 PCI Electrical Specification Conformance

The DECchip 21130 PCI pins conform to the basic set of PCI electrical specifications in the *PCI Local Bus Specification, Revision 2.0,* including:

- Standard signaling

  Logic levels follow standard TTL thresholds to accommodate PCI drivers and receivers implemented with existing CMOS and TTL devices and processes.

- 33-10 support

  The 21130 supports a 33-MHz interconnection of up to ten PCI devices.

See the *PCI Local Bus Specification, Revision 2.0* for a complete description of the PCI I/O protocol and pinouac specifications.

4.2 Absolute Maximum Ratings

Table 4–1 lists the absolute maximum ratings for the 21130. These are stress ratings only; extended exposure to the maximum ratings may affect the reliability of the device.

Table 4–1 Absolute Maximum Ratings

Parameter	Minimum	Maximum
Storage temperature range	–TBS°C	+TBS°C
Supply voltage **Vdd**	–TBS V	TBS V
dc voltage on any pin	–TBS V	**Vdd** + TBS V

4.3 Normal Operating Conditions

Table 4–2 lists the normal operating conditions for the 21130.

Table 4–2 Normal Operating Conditions

Parameter	Minimum	Maximum
Junction temperature range	TBS°C	+TBS°C (TBS°C ambient rating) +TBS°C (TBS°C ambient rating)
Supply voltage **Vdd**	TBS V	TBS V
Power dissipation	—	TBS W*

*Airflow is required when power dissipation exceeds TBS W.

4.4 Supply Current and Power Dissipation

The supply current and power dissipation are as follows:

Idd	TBS A
Power	TBS W (maximum)

4.4.1 Test Conditions

The supply current and power dissipation test conditions are as follows:

Vdd	TBS V
Frame buffer clock frequency	TBS MHz (TBS°C ambient rating) TBS MHz (TBS°C ambient rating)

4.5 dc Specifications

Table 4–3 lists the pin characteristics. The pin output drivers are specified to produce TTL signaling levels; however, they are implemented as CMOS drivers and, as a result, actually drive the pins through the full voltage range (rail-to-rail).

Figure 4–1 shows the various clock domains.

Figure 4–1 Clock Domains

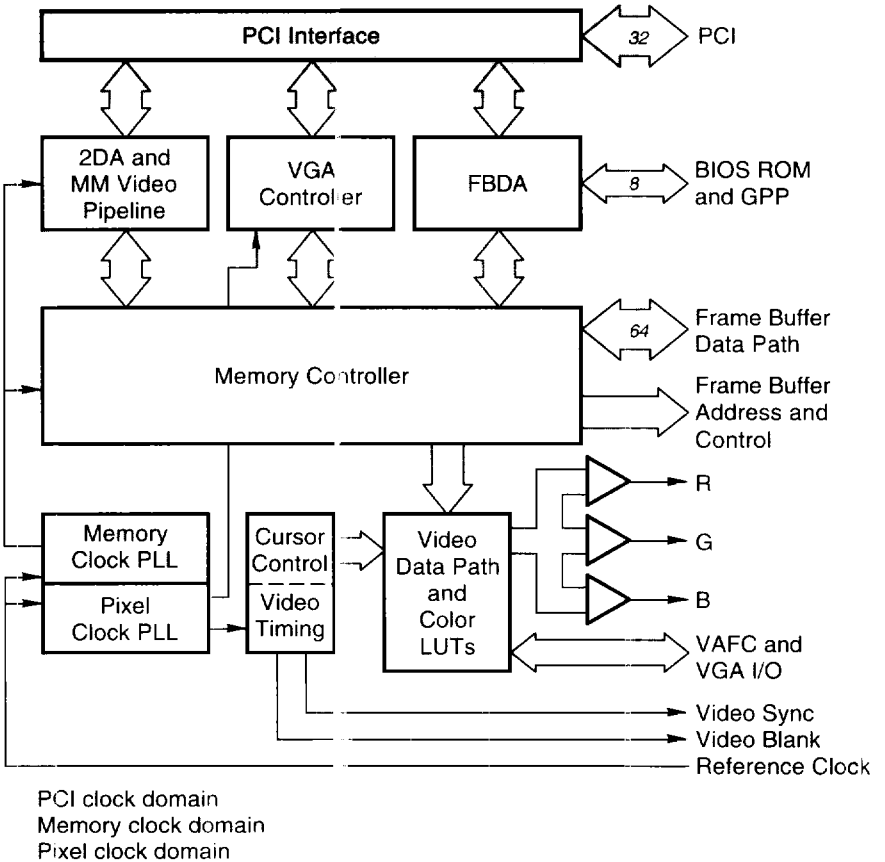


Table 4–3 Pin Characteristics

Signals	Clock Domain	Type	Signal Level	Notes
gp_int#	Async	I	TTL	—
test_in	Async	I	TTL	—
evideo#	Async	I	TTL	—
vafc_en#	Async	O	TTL	—
pci_rst#	Async PCI	I	TTL	—
pci_inta#	Async PCI	O	TTL	❶
pci_gnt#	**pci_clk**	I	TTL	—
pci_idsel	**pci_clk**	I	TTL	—
pci_clk	**pci_clk**	I	TTL	—
pci_ad<31:0>	**pci_clk**	I/O	TTL	—
pci_cbe<3:0>#	**pci_clk**	I/O	TTL	—
pci_devsel#	**pci_clk**	I/O	TTL	—
pci_frame#	**pci_clk**	I/O	TTL	—
pci_irdy#	**pci_clk**	I/O	TTL	—
pci_par	**pci_clk**	I/O	TTL	—
pci_stop#	**pci_clk**	I/O	TTL	—
pci_trdy#	**pci_clk**	I/O	TTL	—
pci_req#	**pci_clk**	O	TTL	—
xtal1	**mem_clk**	I	CMOS	—
xtal2	**mem_clk**	I	CMOS	—
memdata<63:0>	**mem_clk**	I/O	TTL	—
gp_data<7:0>	**mem_clk**	I/O	TTL	—
memaddr<8:0>	**mem_clk**	O	TTL	—
cas<7:0>#	**mem_clk**	O	TTL	—
gp_adr<16:0>	**mem_clk**	O	TTL	—
gp_rdsel#	**mem_clk**	O	TTL	—
gp_wrsel#	**mem_clk**	O	TTL	—
gp_cs#	**mem_clk**	O	TTL	—
gp_reset#	**mem_clk**	O	TTL	—
gp_stb#	**mem_clk**	O	TTL	—
grdy	**mem_clk**	O	TTL	—
oeb#	**mem_clk**	O	TTL	—
ras<2:0>#	**mem_clk**	O	TTL	—
rom_ce#	**mem_clk**	O	TTL	—
rom_oe#	**mem_clk**	O	TTL	—
rom_we#	**mem_clk**	O	TTL	—
wrb#	**mem_clk**	O	TTL	—

(continued on next page)

Table 4–3 (Cont.) Pin Characteristics

Signals	Clock Domain	Type	Signal Level	Notes
pix_clk	**pix_clk**	I	CMOS	—
xtal1	**pix_clk**	I	CMOS	—
vafc_vclk	**pix_clk**	I	TTL	—
ddc_data	**pix_clk**	I/O	CMOS	—
vafc_p<0:15>	**pix_clk**	I/O	TTL	—
vafc_dclk	**pix_clk**	O	TTL	—
blank#	**pix_clk**	O	TTL	—
hsync	**pix_clk**	O	TTL	—
vsync	**pix_clk**	O	TTL	—
red	**pix_clk**	O	—	❷
green	**pix_clk**	O	—	❷
blue	**pix_clk**	O	—	❷

Notes

❶ Pins are driven by an open-drain output driver.

❷ Pins are driven by analog outputs.

4.5.1 Operating Specifications

Table 4–4 lists the functional operating dc parameters for the 21130 under normal operating conditions. The normal operating conditions are specified in Table 4–2.

Note

In Table 4–4, currents into the chip (chip sinking) are denoted as positive (+) current. Currents from the chip (chip sourcing) are denoted as negative (–) current.

Table 4–4 dc Parameters

Symbol	Parameter	Minimum	Maximum	Unit	Notes
Vilc	Low-level input voltage for CMOS-level inputs	TBS × **Vdd**	—	V	—
Vihc	High-level input voltage for CMOS-level inputs	—	TBS × **Vdd**	V	—
Vilt	Low-level input voltage for TTL-level inputs	TBS	—	V	—
Viht	High-level input voltage for TTL-level inputs	—	TBS	V	—
Vol	Low-level output voltage	—	TBS	V	❶
Voh	High-level output voltage	TBS	—	V	❷
Ioz	Tristate leakage current	–TBS	TBS	µA	—
Cin	Input capacitance	—	TBS	pF	❸
Co	I/O or output-only pin capacitance	—	TBS	pF	❸

Notes

❶ Iol = TBS mA for **pci_clk** domain outputs (except **pci_inta#**).
Iol = TBS mA for **pci_inta#** and all other outputs.

❷ Ioh = –TBS mA for **pci_clk** domain outputs.
Ioh = –TBS mA for all other outputs.

❸ PCI pins.

4.6 ac Specifications

The ac specifications consist of input requirements and output responses. The input requirements include setup and hold times, pulse widths, and high and low times. Output responses are delays from clock to signal. The ac specifications are defined separately for each clock domain within the 21130. (See Table 4–3 for a list of signals and their respective clock domains.) All ac specifications apply to the 21130 under normal operating conditions (Table 4–2).

4.6.1 Parameters for PCI Clock Domain Signals

Figure 4–2 shows the ac parameter measurements for signals in the PCI clock domain, and Table 4–5 specifies the parameter values.

Figure 4–2 PCI Clock Domain Signal ac Parameter Measurements

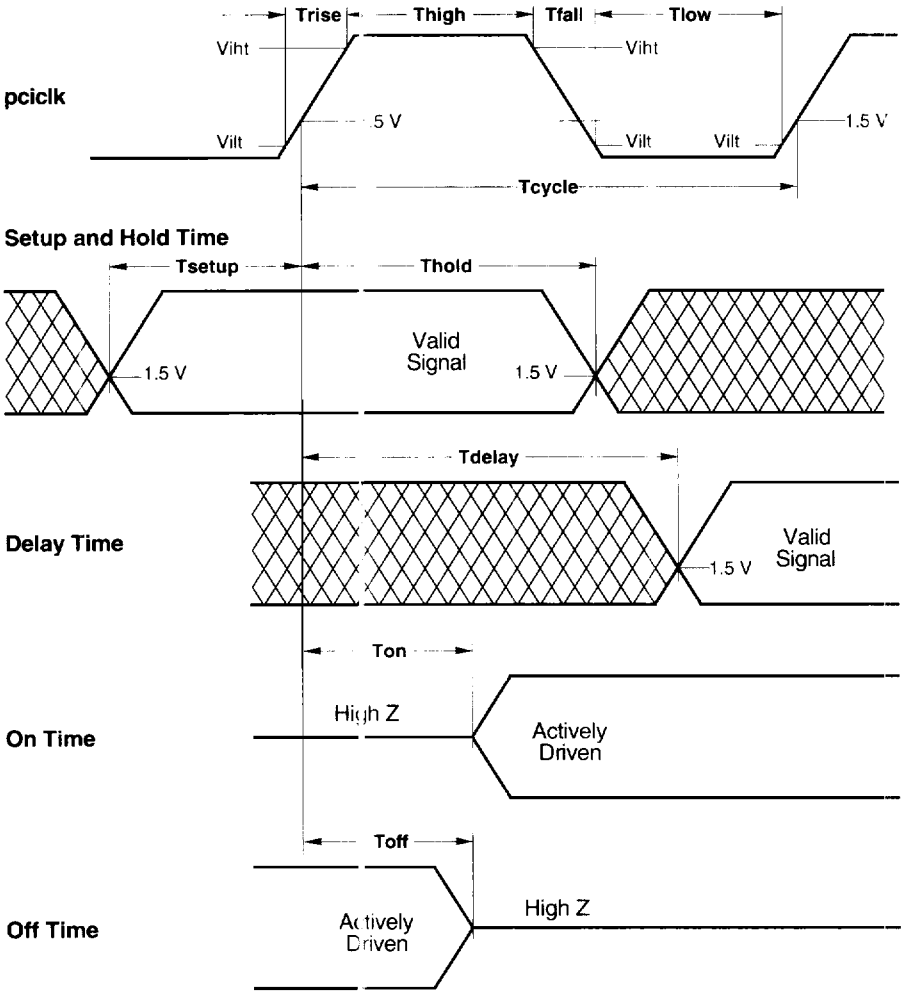


Table 4–5 PCI Clock Domain Signal ac Parameters

Symbol	Parameter	Signals	Minimum	Maximum	Unit
Tcycle	Clock cycle time	**pci_clk**	30	—	ns
Thigh	Clock high time	**pci_clk**	12	—	ns
Tlow	Clock low time	**pci_clk**	12	—	ns
Trise	Clock rise time	**pci_clk**	—	2	ns
Tfall	Clock fall time	**pci_clk**	—	2	ns
Trst	Reset low pulse width*	**pci_rst#**	1	—	ms
Trstclk	Clock active time to end of reset	**pci_rst#**	100	—	µs
Tdelay	Clock to signal valid delay†	**pci_ad<31:0>**	2	11	ns
		pci_cbe<3:0>#	2	11	ns
		pci_frame#	2	11	ns
		pci_trdy#	2	11	ns
		pci_irdy#	2	11	ns
		pci_stop#	2	11	ns
		pci_par	2	11	ns
		pci_devsel#	2	11	ns
		pci_req#	2	12	ns
Ton	High-Z to active delay	**pci_ad<31:0>**	2	—	ns
		pci_cbe<3:0>#	2	—	ns
		pci_frame#	2	—	ns
		pci_trdy#	2	—	ns
		pci_irdy#	2	—	ns
		pci_stop#	2	—	ns
		pci_par	2	—	ns
		pci_devsel#	2	—	ns
		pci_req#		—	ns
Toff	Active to high-Z delay	**pci_ad<31:0>**	—	28	ns
		pci_cbe<3:0>#	—	28	ns
		pci_frame#	—	28	ns
		pci_trdy#	—	28	ns
		pci_irdy#	—	28	ns
		pci_stop#	—	28	ns
		pci_par	—	28	ns
		pci_devsel#	—	28	ns
		pci_req#	—	28	ns

*< 0.8 V

†Minimum delay times are specified with unloaded outputs. Maximum delay times are specified with a 50-pF external pin load.

(continued on next page)

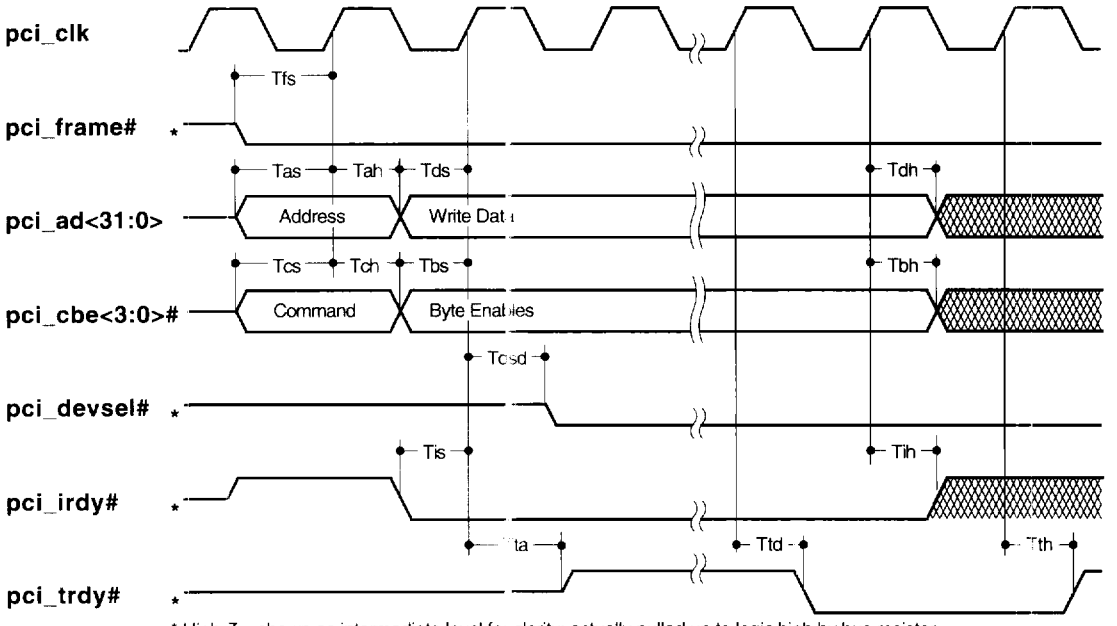
Table 4–5 (Cont.) PCI Clock Domain Signal ac Parameters

Symbol	Parameter	Signals	Minimum	Maximum	Unit
Tsetup	Setup time to clock	**pci_ad<31:0>**	7	—	ns
		pci_cbe<3:0>#	7	—	ns
		pci_frame#	7	—	ns
		pci_trdy#	7	—	ns
		pci_irdy#	7	—	ns
		pci_stop#	7	—	ns
		pci_par	7	—	ns
		pci_devsel#	7	—	ns
		pci_idsel	7	—	ns
		pci_gnt#	10	—	ns
Thold	Hold time	**pci_ad<31:0>**	0	—	ns
		pci_cbe<3:0>#	0	—	ns
		pci_frame#	0	—	ns
		pci_trdy#	0	—	ns
		pci_irdy#	0	—	ns
		pci_stop#	0	—	ns
		pci_par	0	—	ns
		pci_devsel#	0	—	ns
		pci_gnt#	0	—	ns
		pci_idsel	0	—	ns
Trstoff	Reset asserted to high-Z delay	**pci_ad<31:0>**	—	40	ns
		pci_cbe<3:0>#	—	40	ns
		pci_frame#	—	40	ns
		pci_trdy#	—	40	ns
		pci_irdy#	—	40	ns
		pci_stop#	—	40	ns
		pci_par	—	40	ns
		pci_devsel#	—	40	ns
		pci_req#	—	40	ns

4.6.2 PCI Cycle Timing

Figures 4–3 through 4–8 and Tables 4–6 through 4–11 describe the typical timing for selected PCI cycles with the 21130 as a target.

Figure 4–3 PCI Write — Cycle Start Timing



* High Z – shown as intermediate level for clarity; actually pulled up to logic high by bus resistor.

Table 4–6 PCI Write — Cycle Start Timing Parameters

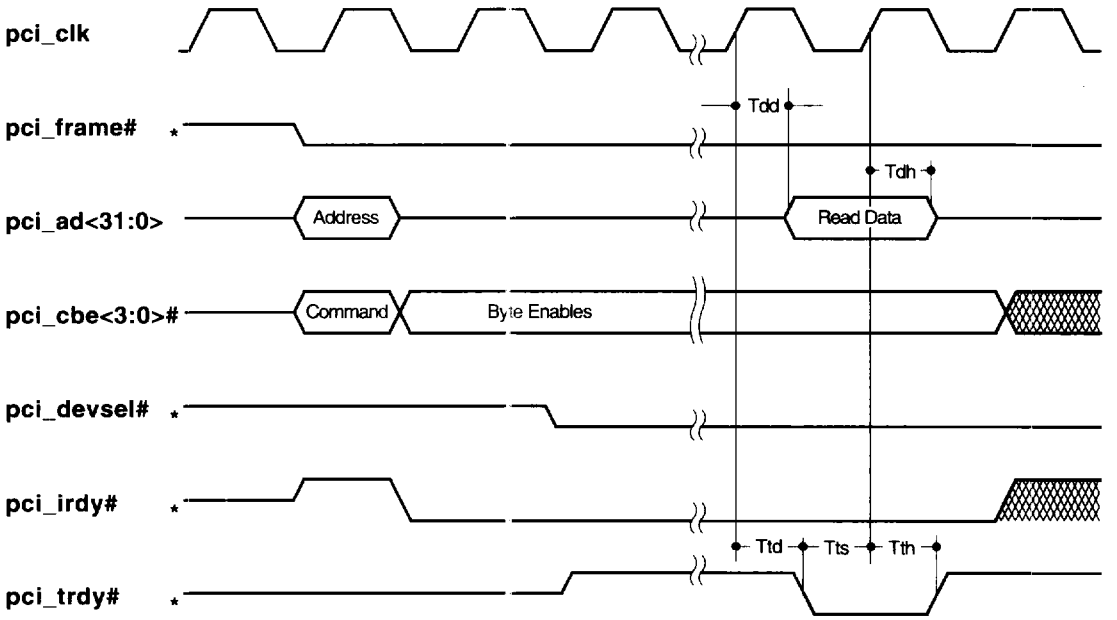
Parameter	Description	Minimum ns	Maximum ns
Tfs	**pci_frame#** setup to clock	7	—
Tas	Address setup to clock	7	—
Tah	Address hold from clock	0	—
Tds	Write data setup to clock	7	—
Tdh	Write data hold from clock	0	—

(continued on next page)

Table 4–6 (Cont.) PCI Write — Cycle Start Timing Parameters

Parameter	Description	Minimum ns	Maximum ns
Tcs	Command setup to clock	7	—
Tch	Command hold from clock	0	—
Tbs	Byte enables setup to clock	7	—
Tbh	Byte enables hold from clock	0	—
Tdsd	**pci_devsel#** clock to signal delay	2	11
Tis	**pci_irdy#** setup to clock	7	—
Tih	**pci_irdy#** hold from clock	0	—
Tta	**pci_trdy#** high Z to active delay	2	—
Ttd	**pci_trdy#** clock to signal delay	2	11
Tth	**pci_trdy#** hold from clock	0	—

Figure 4–4 PCI Read — Cycle Start Timing

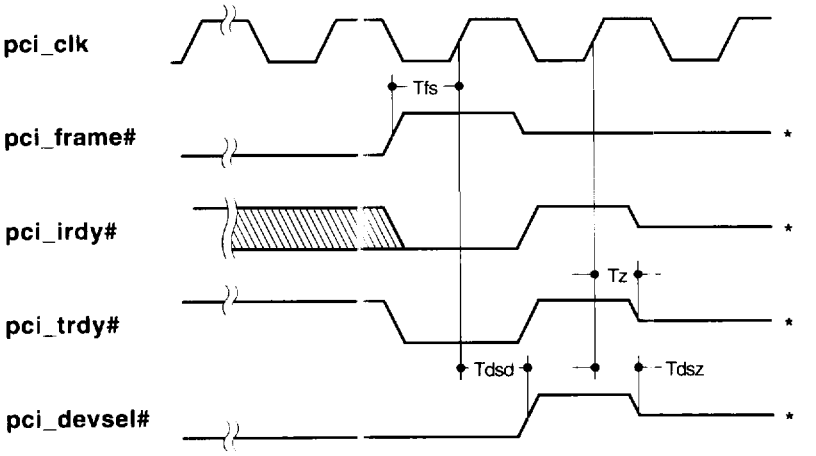


* High Z – shown as intermediate level for clarity; actually pulled up to logic high by bus resistor.

Table 4–7 PCI Read — Cycle Start Timing Parameters

Parameter	Description	Minimum ns	Maximum ns
Tdd	Read data clock to signal delay	2	11
Tdh	Read data hold from clock	0	—
Ttd	**pci_trdy#** clock to signal delay	2	11
Tts	**pci_trdy#** setup to clock	7	—
Tth	**pci_trdy#** hold from clock	0	—

Figure 4–5 PCI Read or Write — Cycle End Timing

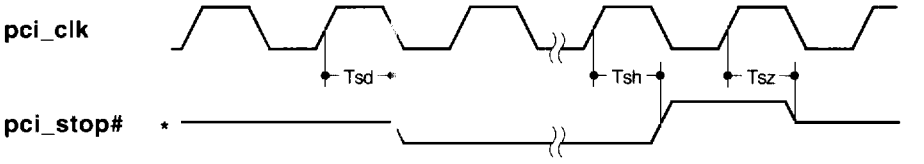


* High Z – shown as intermediate level for clarity; actually pulled up to logic high by bus resistor.

Table 4–8 PCI Read or Write — Cycle End Timing Parameters

Parameter	Description	Minimum ns	Maximum ns
Tfs	**pci_frame#** setup to clock	7	—
Ttz	**pci_trdy#** active to high-Z delay	—	28
Tdsd	**pci_devsel#** clock to signal delay	2	11
Tdsz	**pci_devsel#** active to high-Z delay	—	28

Figure 4–6 PCI Target Disconnect or Abort — pci_stop# Timing

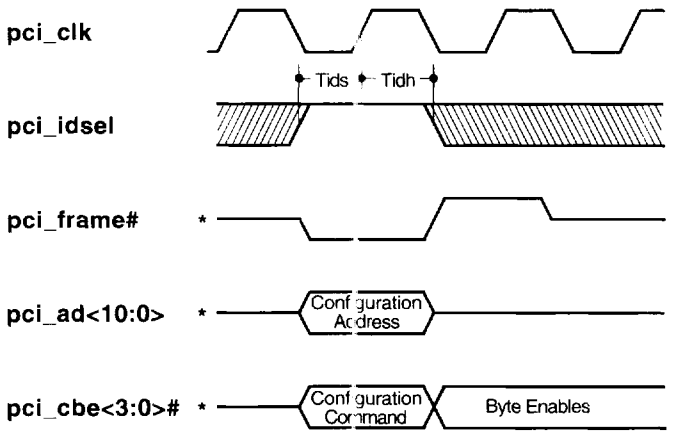


* High Z – shown as interme diate level for clarity; actually pulled up to logic high by bus resistor.

Table 4–9 PCI Target Disconnect or Abort — pci_stop# Timing Parameters

Parameter	Description	Minimum ns	Maximum ns
Tsd	**pci_stop#** clock to s gnal delay	2	11
Tsh	**pci_stop#** hold from clock	0	—
Tc	**pci_stop#** active to igh-Z delay	—	28

Figure 4–7 PCI Configuration Cycle — pci_idsel Timing



* High Z – shown as intermediate level for clarity; actually pulled up to high by bus resistor.

Table 4–10 PCI Configuration Cycle — pci_idsel Timing Parameters

Parameter	Description	Minimum ns	Maximum ns
Tids	**pci_idsel** setup to clock	7	—
Tidh	**pci_idsel** hold from clock	0	—

Figure 4–8 and Table 4–11 describe typical parity timing for the 21130 as a target. As a master, the timing is identical, but the 21130 drives address, command, and write data parity, and receives read data parity.

Figure 4–8 PCI Parity — pci_par Timing

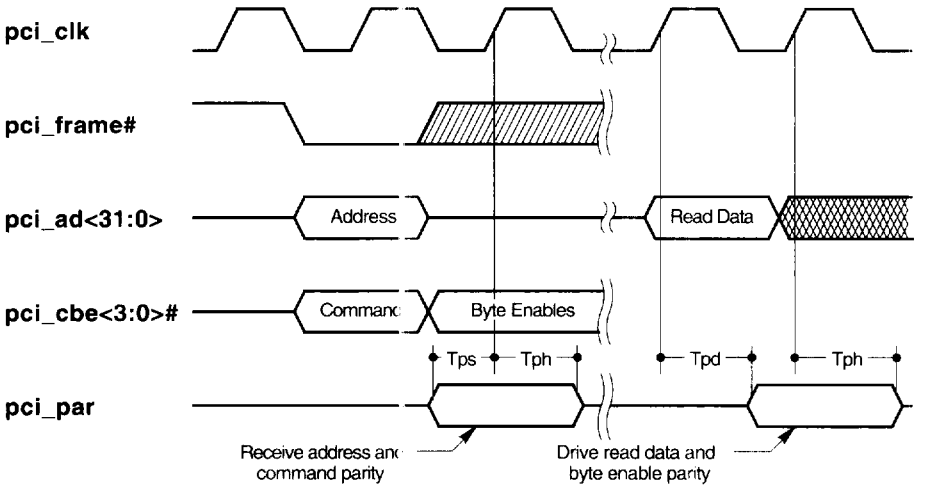


Table 4–11 PCI Parity — pci_par Timing Parameters

Parameter	Description	Minimum ns	Maximum ns
Tps	**pci_par** setup to clock	7	—
Tph	**pci_par** hold from clock	0	—
Tpd	**pci_par** clock to signal delay	2	11

4.6.3 Parameters for Memory Clock and Core Clock Domain Signals

Figure 4–9 shows the ac parameter measurements for signals in the memory clock (**mem_clk**) and core clock domains (the core clock is one-half the frequency of the memory clock). Table 4–12 specifies the parameter values.

Figure 4–9 Memory Clock and Core Clock Domain Signal ac Parameter Measurements

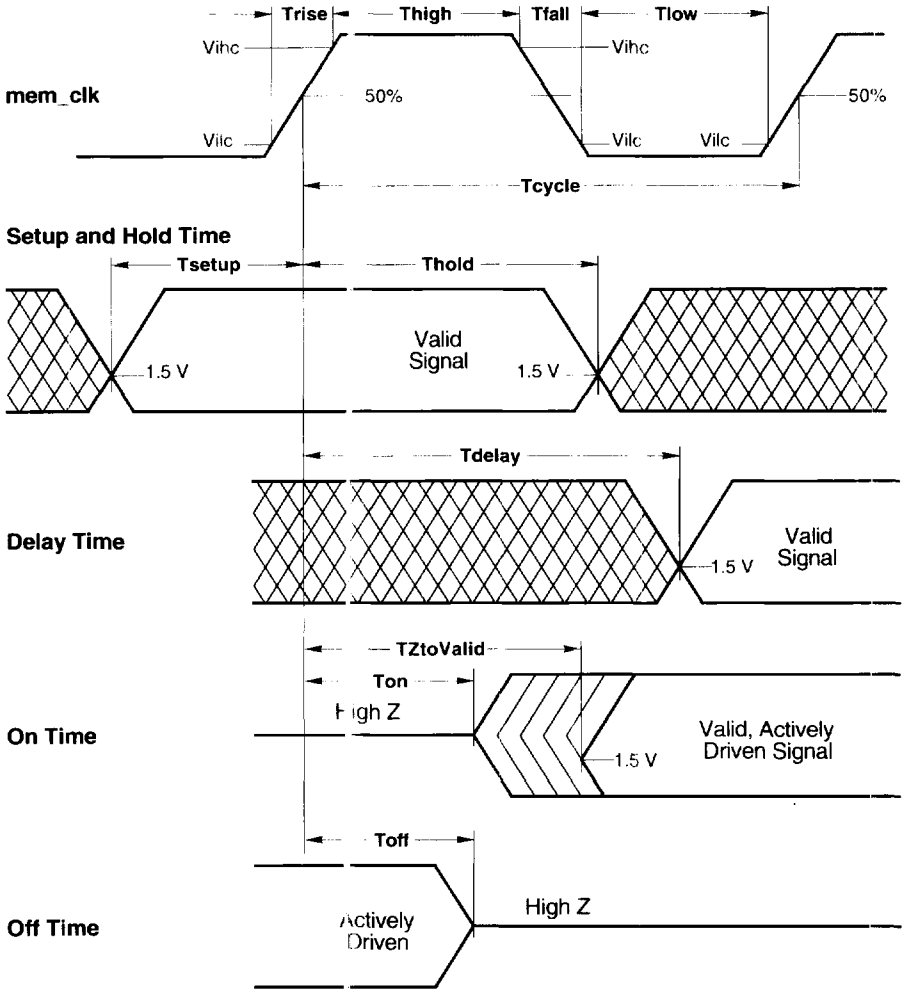


Table 4–12 Memory Clock and Core Clock Domain ac Parameters

Symbol	Parameter	Signals	Minimum ns	Maximum ns	Notes
Tcycle	Clock cycle time (66 MHz)	**mem_clk**	15.1	—	—
Thigh	Clock high time	**mem_clk**	6.0	—	—
Tlow	Clock low time	**mem_clk**	6.0	—	—
Trise	Clock rise time	**mem_clk**	—	1.7	—
Tfall	Clock fall time	**mem_clk**	—	1.7	—
Tdelay	Clock to signal valid delay	**memaddr<8:0>**	?.?	??.?	1
		cas<7:0>#	?.?	??.?	1
		gp_adr<16:0>	?.?	??.?	1
		gp_rdsel#	?.?	??.?	1
		gp_wrsel#	?.?	??.?	1
		gp_cs#	?.?	??.?	1
		gp_reset#	?.?	??.?	1
		gp_stb#	?.?	??.?	1
		grdy	?.?	??.?	1
		oeb#	?.?	??.?	1
		ras<2:0>#	?.?	??.?	1
		rom_ce#	?.?	??.?	1
		rom_oe#	?.?	??.?	1
		rom_we#	?.?	??.?	1
		wrb#	?.?	??.?	1
Tdelay	Clock to signal valid delay	**memdata<63:0>**	?.?	—	1
			—	??.?	1
			—	??.?	1
			—	??.?	1
		gp_data<7:0>	?.?	—	1
			—	??.?	1
			—	??.?	1
			—	??.?	1
TZtoValid	High-Z to valid delay time	**memdata<63:0>**	?.?	—	1
			—	??.?	1
			—	??.?	1
			—	??.?	1
		gp_data<7:0>	?.?	—	1
			—	??.?	1
			—	??.?	1
			—	??.?	1

(continued on next page)

Table 4–12 (Cont.) Memory Clock and Core Clock Domain ac Parameters

Symbol	Parameter	Signals	Minimum ns	Maximum ns	Notes
Toff	Driven to high-Z delay time	**memdata<63:0>**	?.?	?.?	—
		gp_data<7:0>	?.?	?.?	—
Ton	High-Z to driven delay time	**memdata<63:0>**	?.?	—	—
		gp_data<7:0>	?.?	—	—
Tsetup	Setup time	**memdata<63:0>**	?.?	—	—
		gp_data<7:0>	?.?	—	—
Thold	Hold time	**memdata<63:0>**	?.?	—	—
		gp_data<7:0>	?.?	—	—

Notes

❶ Values to be supplied

4.6.4 Memory Cycle Timing

Figures 4–10 through 4–13 and Tables 4–13 through 4–16 describe typical memory timing cycles.

Figure 4–10 Hyperpage Mode Memory Write Cycle Timing

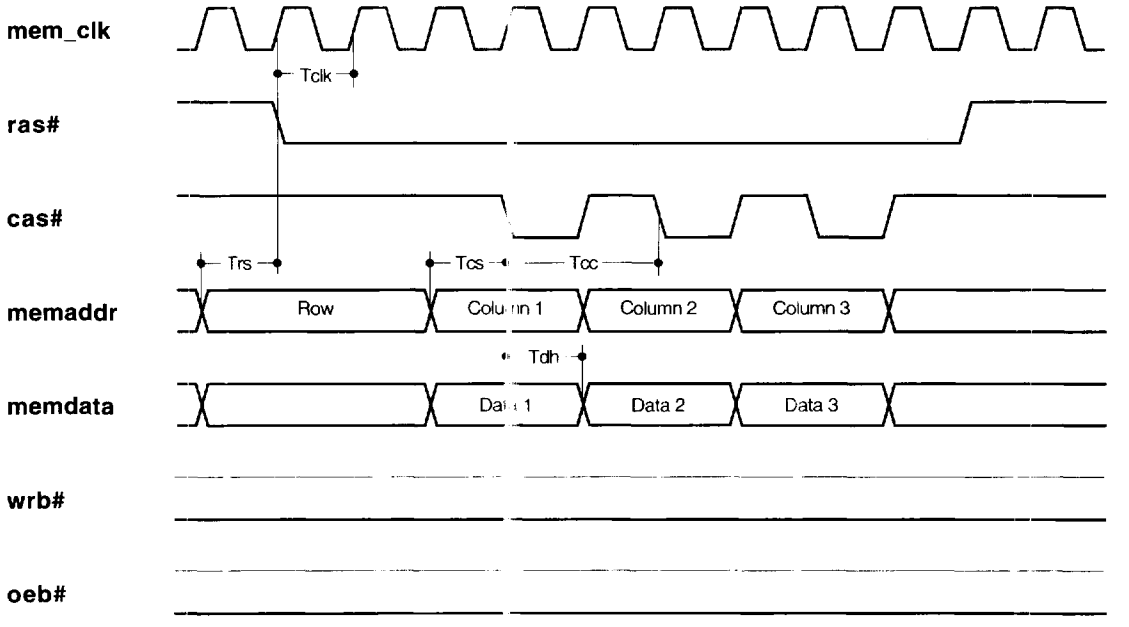


Table 4–13 Hyperpage Mode Memory Write Cycle Timing Parameters

Parameter	Description	Value
Tcc	Cycle Time	2Tclk
Trs	Row setup time	Usually 0
Tcs	Column setup time	Usually 0
Tdh	Data hold time	Must be <Tclk–2 ns

Figure 4–11 Hyperpage Mode Memory Read Cycle Timing

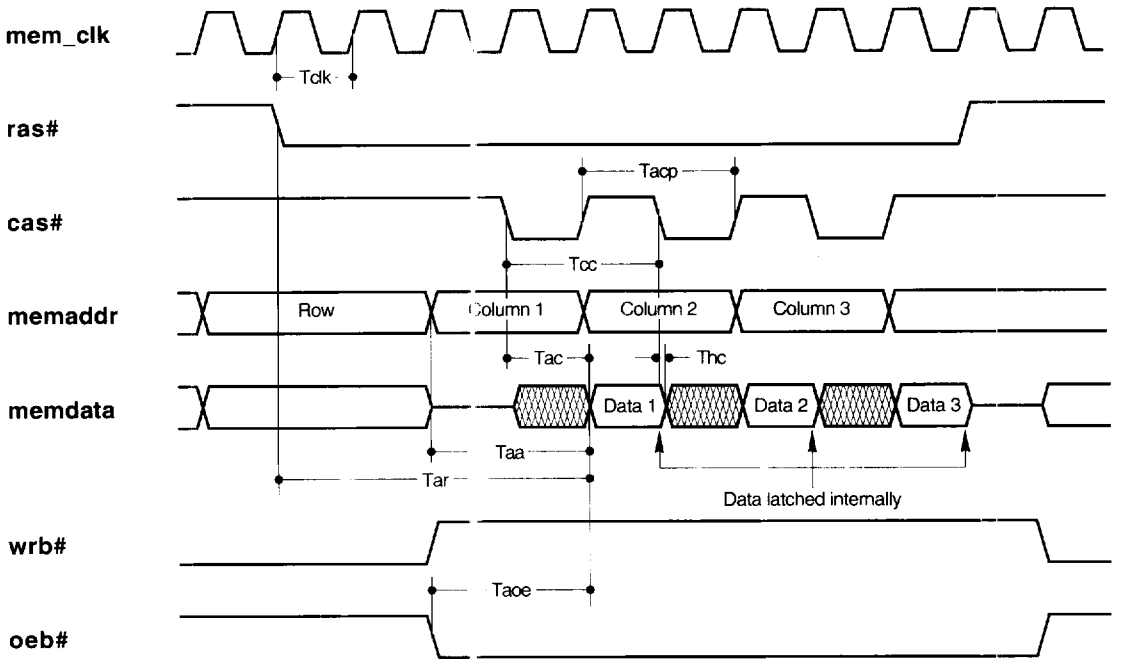


Table 4–14 Hyperpage Mode Memory Read Cycle Timing Parameters

Parameter	Description	Value
Tcc	Cycle Time	2Tclk
Tar	RAS access time	<5Tclk – 13 ns
Taa	Address access time	<3Tclk – 13.75 ns
Tac	CAS access time	<2Tclk – 12.75 ns
Tacp	Access time from CAS precharge	<3Tclk – 10.25 ns
Thc	Data hold time	≥0
Taoe	Output enable access time	≤2Tclk – 13.75 ns

Figure 4–12 Read-Modify-Write Memory Cycle Timing

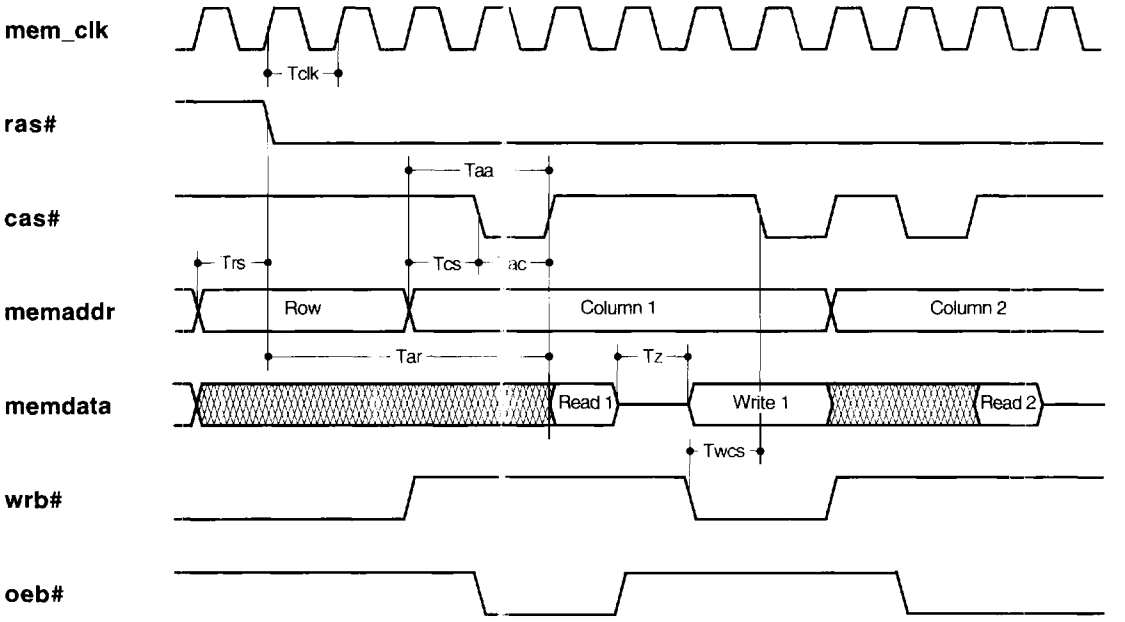


Table 4–15 Read-Modify-Write Memory Cycle Timing Parameters

Parameter	Description	Value
Tar	RAS access time	<5Tclk−13 ns
Taa	Address access time	<3Tclk−13.75 ns
Trs	Row setup time	Usually 0
Tcs	Column setup time	Usually 0
Tac	CAS access time	<2Tclk−12.75 ns
Tz	Bus turnaround time	= Tclk
Twcs	Write enable to CAS setup time	≤Tclk−2 ns

Figure 4–13 CAS-Before-RAS Memory Refresh Cycle Timing

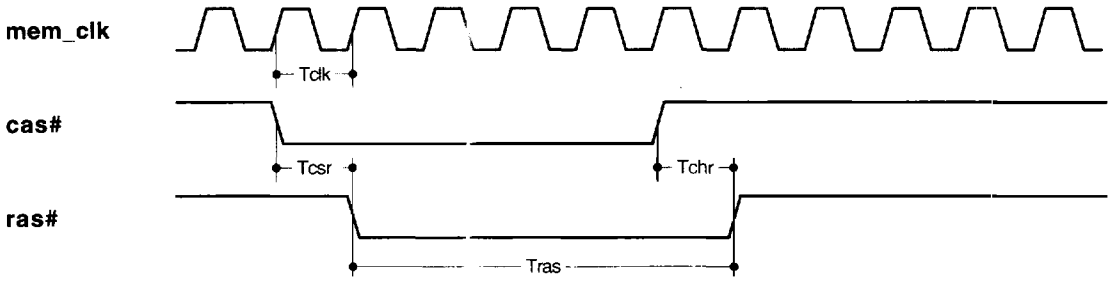


Table 4–16 CAS-Before-RAS Memory Refresh Cycle Timing Parameters

Parameter	Description	Value
Tcsr	CAS setup time before RAS	2Tclk
Tchr	RAS hold time after CAS	2Tclk
Tras	RAS assertion time	5Tclk

4.6.5 ROM and GPP Data Cycle Timing

Figure 4–14, Figure 4–15, and Table 4–17 describe typical timing for ROM and GPP data transfer cycles. Also see Figure 4–9 and Table 4–12 for ac parameter measurements.

Figure 4–14 ROM Data Cycle Timing

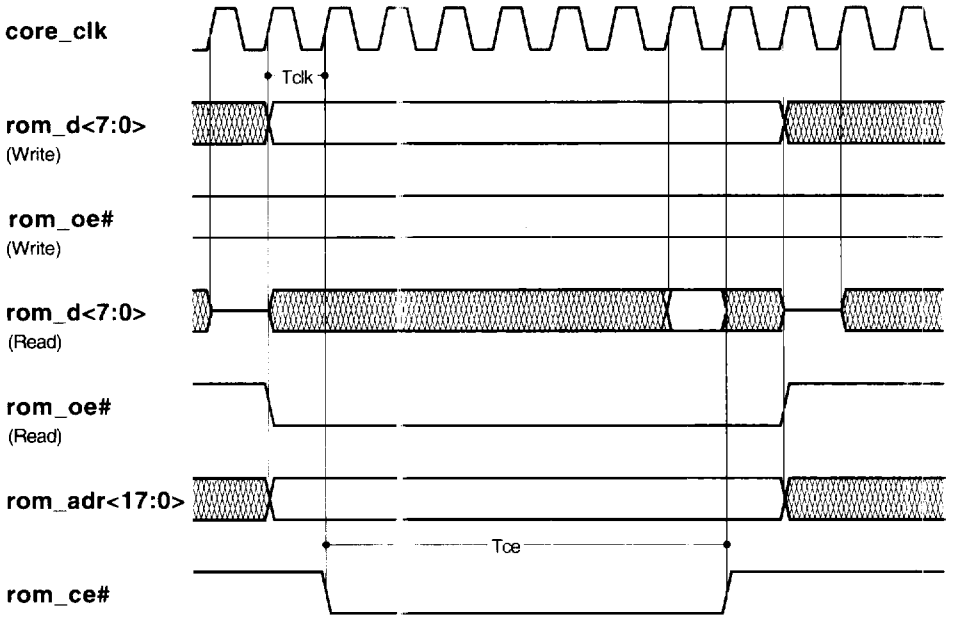
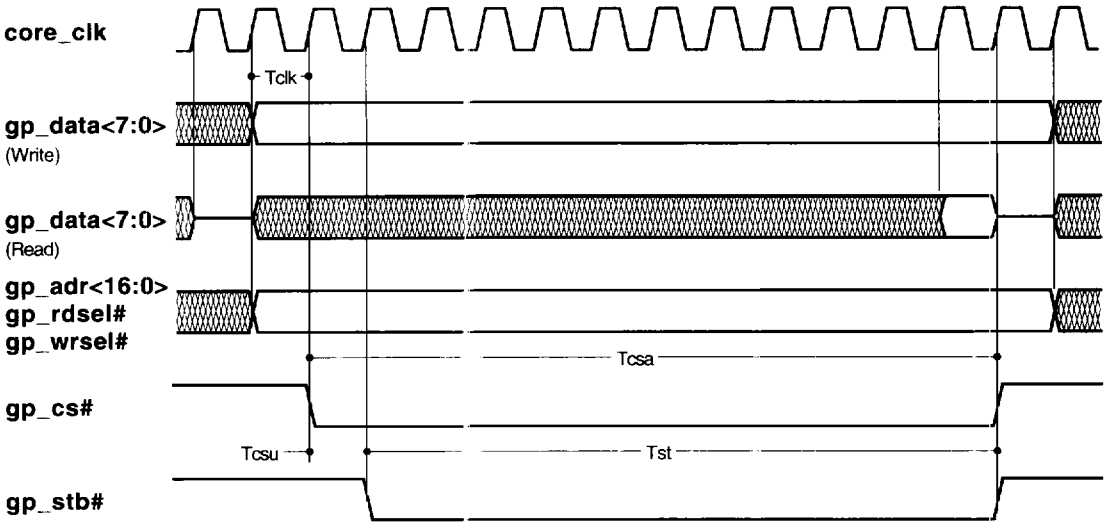


Table 4–17 ROM and GPP Data Cycle Timing Parameters

Parameter	Description	Value
Tclk	Clock cycle time (33 MHz)	30 ns
Tce	Chip enable assertion time	7Tclk
Tcsu	Chip select setup time	1Tclk
Tcsa	Chip select assertion time	12Tclk
Tst	Chip strobe assertion time	11Tclk

Figure 4–15 GPP Data Cycle Timing



4.6.6 Parameters for Pixel Clock and VAFC Clock Domain Signals

Figure 4–16 shows the ac parameter measurements for signals in the pixel clock (**pix_clk**) domain, and Figure 4–17 shows the ac parameter measurements for signals in the VAFC clock domain (the VAFC clock domain is a subset of the pixel clock domain). Table 4–18 specifies the parameter values.

Figure 4–16 Pixel Clock Domain Signal ac Parameter Measurements

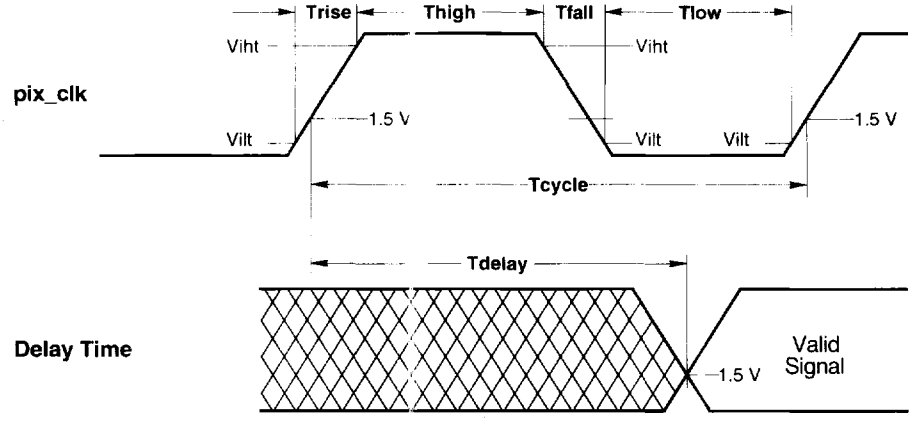
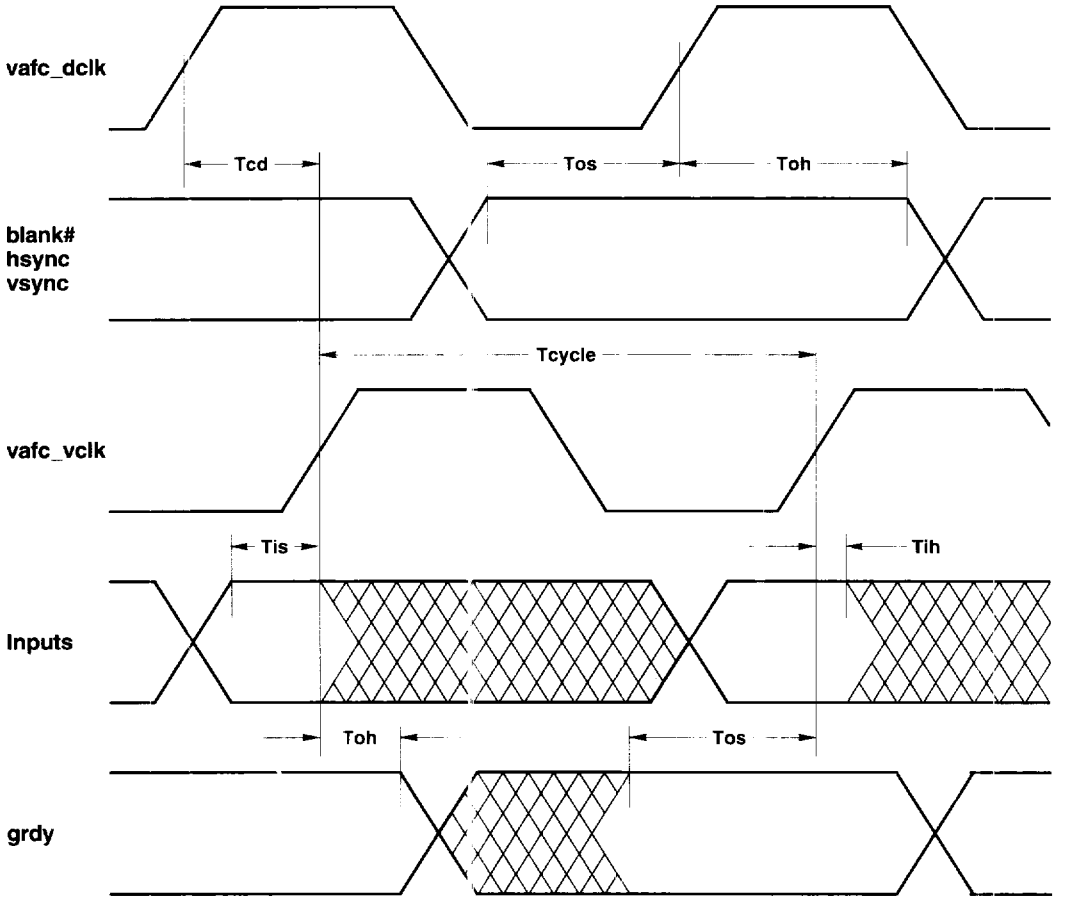


Figure 4–17 VAFC Clock Domain Signal ac Parameter Measurements



4.6 ac Specifications

Table 4–18 Pixel Clock and VAFC Clock Domain Signal ac Parameters

Symbol	Parameter	Signals	Minimum ns	Maximum ns	Notes
Tcycle	Clock cycle time (62.5 MHz)	**pix_clk**	16.0	—	❶
	Clock cycle time (37.5 MHz)	**vafc_dclk**	26.6	—	❷
	Clock cycle time (37.5 MHz)	**vafc_vclk**	26.6	—	❷
Thigh	Clock high time	**pix_clk**	6.5	—	—
		vafc_dclk	10.0	—	—
		vafc_vclk	10.0	—	—
Tlow	Clock low time	**pix_clk**	6.5	—	—
		vafc_dclk	10.0	—	—
		vafc_vclk	10.0	—	—
Trise	Clock rise time	**pix_clk**	—	3.0	—
	Rise time	**vafc_en#**	—	3.0	—
	Rise time	**evideo#**	—	3.0	—
Tfall	Clock fall time	**pix_clk**	—	3.0	—
	Fall time	**vafc_en#**	—	3.0	—
	Fall time	**evideo#**	—	3.0	—
Tcd	**vafc_dclk** to **vafc_vclk** delay	**vafc_dclk** **vafc_vclk**	5.0	20.0	❸
Tos	Output setup time	**blank#**	10.0	—	
		hsync	10.0	—	— —
		vsync	10.0	—	—
		grdy	10.0	—	—
		vafc_p<0:15>	10.0	—	—
Toh	Output hold time	**blank#**	2.0	—	
		hsync	2.0	—	— —
		vsync	2.0	—	—
		grdy	2.0	—	—
		vafc_p<0:15>	2.0	—	—
Tis	Input setup time	**vafc_p<0:15>**	10.0	—	—
Tih	Input hold time	**vafc_p<0:15>**	2.0	—	—

(continued on next page)

Table 4–18 (Cont.) Pixel Clock and VAFC Clock Domain Signal ac Parameters

Notes

❶ The frequency for **pix_clk** is 62.5 MHz.

❷ The maximum frequency for **vafc_dclk** and **vafc_vclk** is 37.5 MHz (75 MHz ÷ 2, based on 75 MHz for a standard VESA 1024 × 768 70-Hz mode). Operation of graphics or video controllers at higher frequencies is outside of VESA compatibility and correct operation is not guaranteed.

❸ For synchronous transfers, **vafc_vclk** must meet this parameter.

4.6.7 VAFC Cycle Timing

Figures 4–18 and 4–19 and Tables 4–19 and 4–20 describe typical VAFC timing cycles. The measurements are extracted from the *VESA Advanced Feature Connector (VAFC) Proposal, Version 1.0p, Revision 0.4.*

Figure 4–18 VAFC Request Cycle Timing

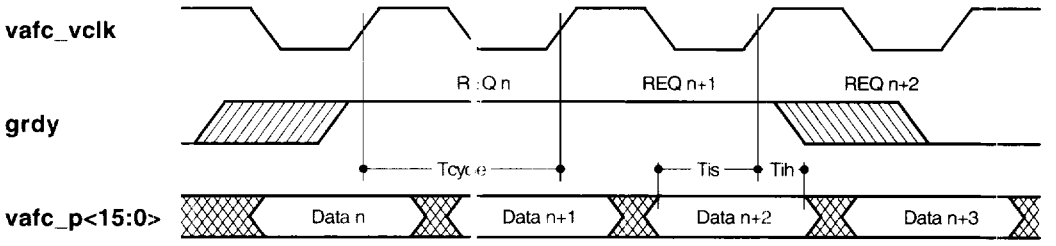


Table 4–19 VAFC Request Cycle Timing Parameters

Parameter	Description	Value
Tcycle	**vafc_vclk** cycle time	≥26.6 ns
Tis	**vafc_p<0:15>** setup time	≥10.0 ns
Tih	**vafc_p<0:15>** hold time	≥2.0 ns

Figure 4–19 VAFC Video Data Transfer Cycle Timing

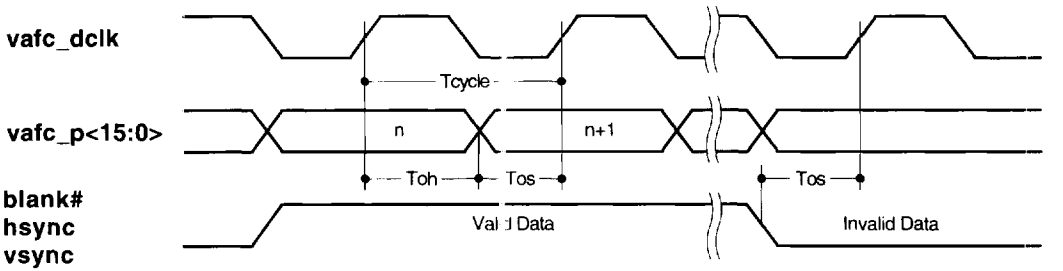


Table 4–20 VAFC Video Data Transfer Cycle Timing Parameters

Parameter	Description	Value
Tcycle	**vafc_dclk** cycle time	≥26.6 ns
Tos	Output setup time	≥10.0 ns
Toh	Output hold time	≥2.0 ns

Notes:

- **vafc_dclk** is driven from the graphics source and is typically a submultiple of the pixel clock.
- **blank#** defines the display area.
- During invalid data time, the DAC can send any data.
- **grdy** is not used in output modes.