



Am95C95

Magnetic Disk Controller

DISTINCTIVE CHARACTERISTICS

- Handles ESMD/ESDI and ST-506 Magnetic Disk Data Format
- User programmable disk formats
- On-chip Reed-Solomon Error Detection and Correction
- Minimal Rotational Latency Read/Write Operations
- 1:1 Sector Interleave Read/Write Operations
- 20 MHz System Clock
- Up to 32 MHz NRZ Serial Disk Data
- High Level Command Set
- Supports Intelligent SCSI-type Interfaces
- On-chip Buffer Management
- Direct support of DRAM Buffer (up to 4 MBytes)

GENERAL DESCRIPTION

The Magnetic Disk Data Controller (MDC) is a highly programmable magnetic disk data format controller designed for use in both standard and custom applications. The device has been optimized for applications utilizing an embedded SCSI disk data manager, but it easily supports other intelligent proprietary interfaces as well.

As an embedded controller, the MDC handles the timing of all disk read/write control signals, the transfer of NRZ data between the disk and buffer RAM, and the transfer of disk data between a parallel host interface and buffer RAM. The MDC performs all buffer management and arbitration associated with this transfer of data while maintaining data integrity through on-chip error detection and correction logic. In addition, the MDC can perform advanced data mapping operations during data transfer, simplifying the task of cache management. The MDC can handle up to 4 Mbytes of data buffer Dynamic RAM directly, including address multiplexing and refresh, with no external logic.

The MDC acts as an intelligent peripheral to a microprocessor or microcontroller. In an embedded SCSI disk controller application, the control CPU (referred to in this document as simply the CPU), interprets all SCSI commands and controls disk head positioning and head selection, while the MDC handles all data transfers. The CPU sets up and initiates MDC operation by modifying as few as 6 MDC registers. MDC registers are directly addressable, and can be read or written directly with either an iAPX multiplexed address/data bus, or a Motorola 68xxx type non-multiplexed bus interface.

The on-chip Reed-Solomon Error Detection And Correction (EDAC) logic enables the MDC to perform on-the-fly error correction during disk read operations while maintaining a zero sector interleave on the disk. The MDC performs such error correction without CPU intervention. The Reed-Solomon logic supports 2, 3 or 5 EDAC interleaves within a sector data field and either single- or double-burst correction capability.

The diagram illustrates the internal architecture of the 386i system. At the top, the **Host Interface (i.e., SCSI)** and **Buffer RAM** are connected to the system bus. The **CPU** is connected to the system via **Data 8** and **Address 8** lines. The system bus is connected to the **Host Interface** and **Buffer RAM**. The **Host Interface** is connected to the **Host Burst Generator** and the **Arbiter**. The **Buffer RAM** is connected to the **Arbiter** and the **DRAM Control**. The **Arbiter** is connected to the **DRAM Control**, **Refresh Generator**, **FIFO Burst Generator**, and **FIFO**. The **DRAM Control** is connected to the **Refresh Generator** and the **FIFO Burst Generator**. The **Refresh Generator** is connected to the **FIFO Burst Generator**. The **FIFO Burst Generator** is connected to the **FIFO**. The **FIFO** is connected to the **Header RAM**, **EDAC Logic**, **CRC Logic**, and **Cmd Status**. The **Header RAM** is connected to the **EDAC Logic**, **CRC Logic**, and **Cmd Status**. The **EDAC Logic** is connected to the **CRC Logic** and **Cmd Status**. The **CRC Logic** is connected to the **Cmd Status**. The **Cmd Status** is connected to the **Writable Control Store**. The **Writable Control Store** is connected to the **RG**, **WG**, **INDEX**, **AMC**, **AMF**, **FAULT**, **GENO1**, **GENO2**, and **GENIO**. The **Writable Control Store** is also connected to the **Host Interface** and **Buffer RAM**. The **Host Interface** is connected to the **Host Burst Generator** and the **Arbiter**. The **Buffer RAM** is connected to the **Arbiter** and the **DRAM Control**. The **Arbiter** is connected to the **DRAM Control**, **Refresh Generator**, **FIFO Burst Generator**, and **FIFO**. The **DRAM Control** is connected to the **Refresh Generator** and the **FIFO Burst Generator**. The **Refresh Generator** is connected to the **FIFO Burst Generator**. The **FIFO Burst Generator** is connected to the **FIFO**. The **FIFO** is connected to the **Header RAM**, **EDAC Logic**, **CRC Logic**, and **Cmd Status**. The **Header RAM** is connected to the **EDAC Logic**, **CRC Logic**, and **Cmd Status**. The **EDAC Logic** is connected to the **CRC Logic** and **Cmd Status**. The **CRC Logic** is connected to the **Cmd Status**. The **Cmd Status** is connected to the **Writable Control Store**. The **Writable Control Store** is connected to the **RG**, **WG**, **INDEX**, **AMC**, **AMF**, **FAULT**, **GENO1**, **GENO2**, and **GENIO**. The **Writable Control Store** is also connected to the **Host Interface** and **Buffer RAM**. The **Host Interface** is connected to the **Host Burst Generator** and the **Arbiter**. The **Buffer RAM** is connected to the **Arbiter** and the **DRAM Control**. The **Arbiter** is connected to the **DRAM Control**, **Refresh Generator**, **FIFO Burst Generator**, and **FIFO**. The **DRAM Control** is connected to the **Refresh Generator** and the **FIFO Burst Generator**. The **Refresh Generator** is connected to the **FIFO Burst Generator**. The **FIFO Burst Generator** is connected to the **FIFO**. The **FIFO** is connected to the **Header RAM**, **EDAC Logic**, **CRC Logic**, and **Cmd Status**. The **Header RAM** is connected to the **EDAC Logic**, **CRC Logic**, and **Cmd Status**. The **EDAC Logic** is connected to the **CRC Logic** and **Cmd Status**. The **CRC Logic** is connected to the **Cmd Status**. The **Cmd Status** is connected to the **Writable Control Store**. The **Writable Control Store** is connected to the **RG**, **WG**, **INDEX**, **AMC**, **AMF**, **FAULT**, **GENO1**, **GENO2**, and **GENIO**. The **Writable Control Store** is also connected to the **Host Interface** and **Buffer RAM**.

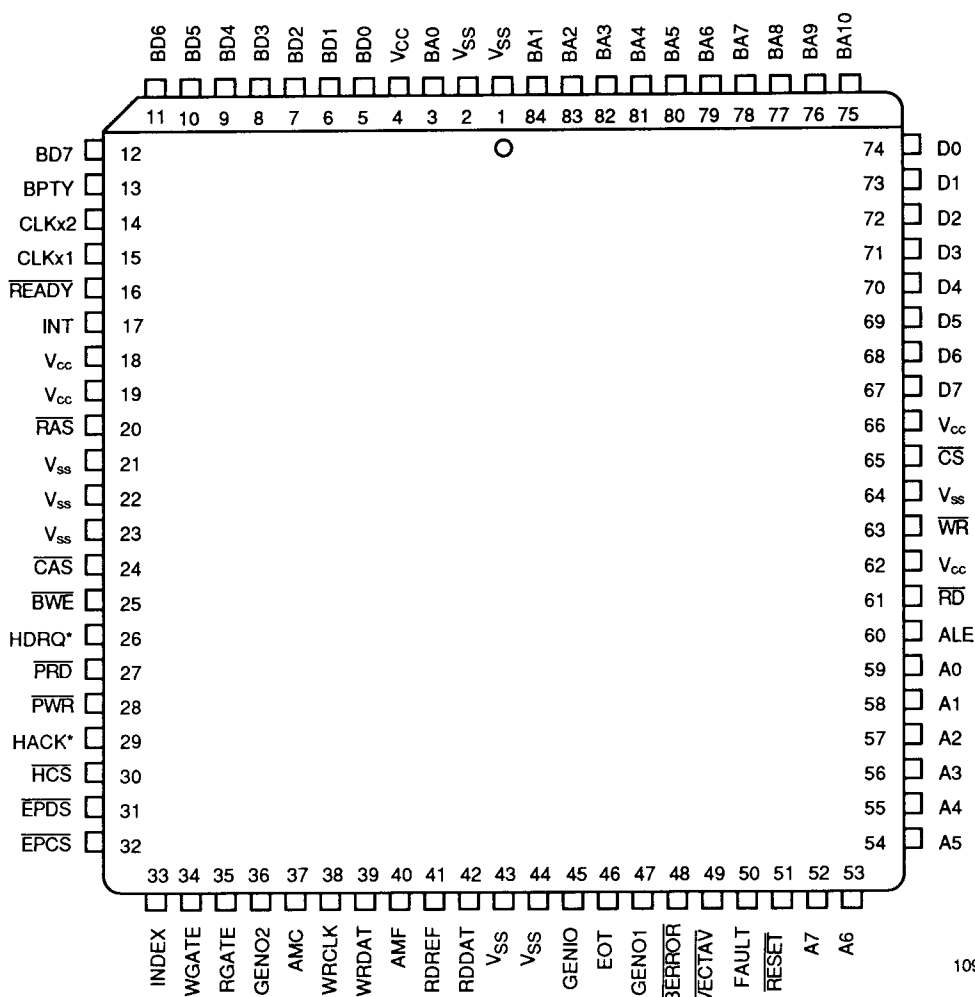
The diagram illustrates the architecture of the Am95C95-based SCSI controller. It features a central **Microcontroller** block, which is a dashed rectangle containing three sub-components: **CPU RAM/ROM**, **CPU (8/16 Bits)**, and **Disk Interface**. These three components are interconnected by a **CPU BUS**. The **Microcontroller** is connected to the **MDC (Am95C95)** block via an **8-bit** bus. The **MDC** block is connected to the **Host Interface (SCSI) (Am33C93A)** block via a **Buffer Bus (Parity Optional)** with a width of **8+Pty**. The **Host Interface** block is connected to the **SCSI Bus**. The **MDC** block is also connected to the **Data Encoder and Decoder** block via a bidirectional bus. The **Data Encoder and Decoder** block is connected to the **Disk R/W Logic** block via a bidirectional bus. The **Disk R/W Logic** block is connected to the **Disk** (represented by a cylinder symbol) via a bidirectional bus. The **External Buffer Memory (DRAMs)** block is connected to the **Buffer Bus** via a bidirectional bus.

Am95C95

RELATED AMD PRODUCTS

Part Number	Description
Am33C93A	SCSI Controller
Am53C80	SCSI Controller
Am805x	Microcontroller
Am80C521	CMOS Microcontroller
Am80188	Microprocessor
Am95C94	Advanced Burst Error Processor

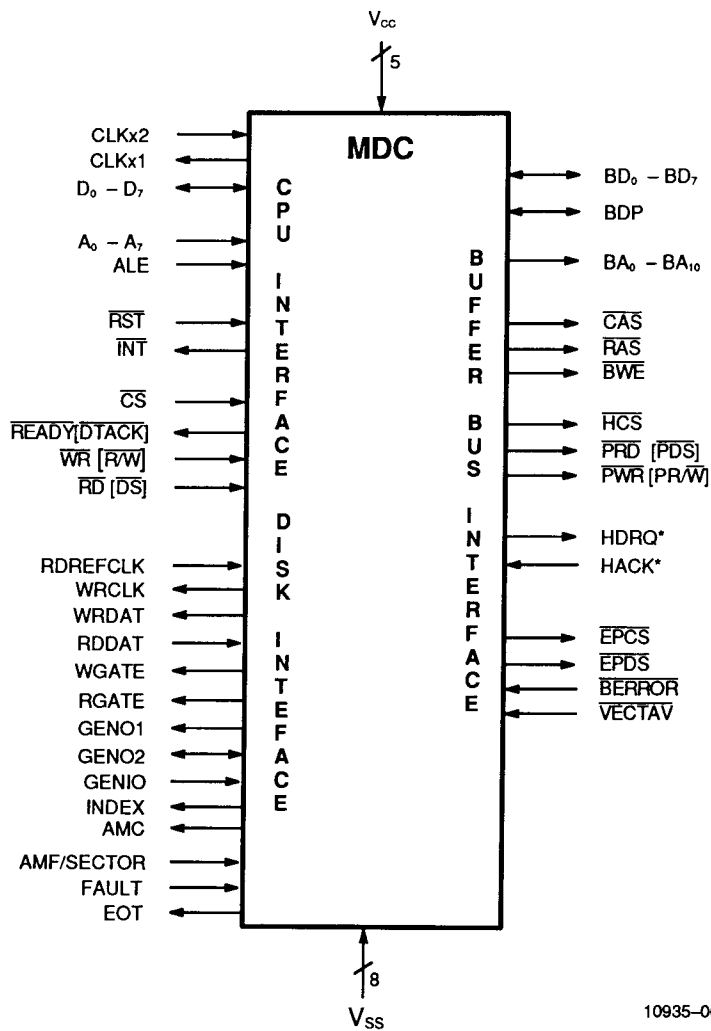
CONNECTION DIAGRAM



10935-003A

* These pins have programmable polarity.

LOGIC DIAGRAM



10935-004A

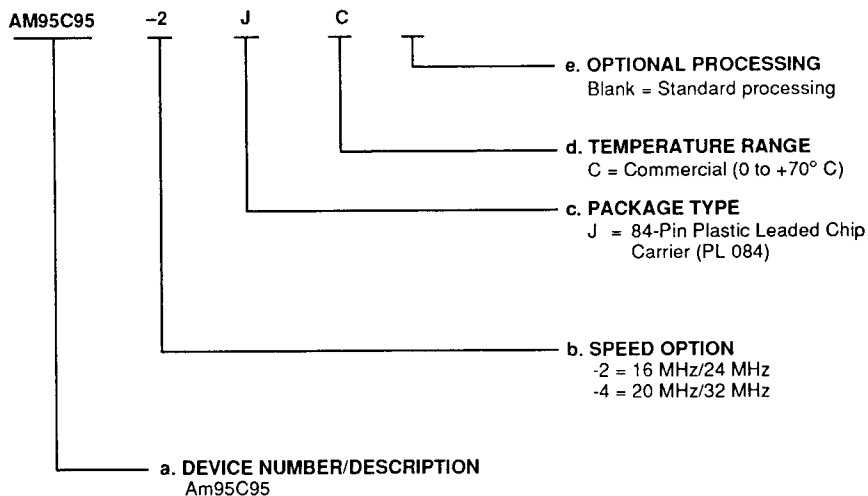
* These pins have programmable polarity.

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing



Valid Combinations	
AM95C95-2JC	JC
AM95C95-4JC	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

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Advanced Micro Devices, Inc. 901 Thompson Place, P.O. Box 3453, Sunnyvale, CA 94088, USA
Tel: (408) 732-2400 • TWX: 910-339-9280 • TELEX: 34-6306 • TOLL FREE: (800) 538-8450
APPLICATIONS HOTLINE TOLL FREE: (800) 222-9323 • (408) 749-5703

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