MSM6992

HIGH PERFORMANCE DIGITAL SIGNAL PROCESSOR

GENERAL DESCRIPTION

The MSM6992 is a very high performance general purpose 22-bit floating-point digital signal processor (DSP). The MSM6992 is fabricated by using OKI's low power consumption CMOS silicon gate technology.

The MSM6992 is capable of high-speed execution of floating-point arithmetic operations (16-bit mantissa and 6-bit exponent part) and 16-bit fixed-point arithmetic operations. Devices will be available with 125nS & 100nS machine cycle time.

The MSM6992 incorporates a 1K-word × 32-bit programmable ROM and two 128-word × 22 bit data RAMs that can alos be used as a single page of 256 words.

The program and data memories can both be expanded externally up to 64K words via dedicated data and address lines.

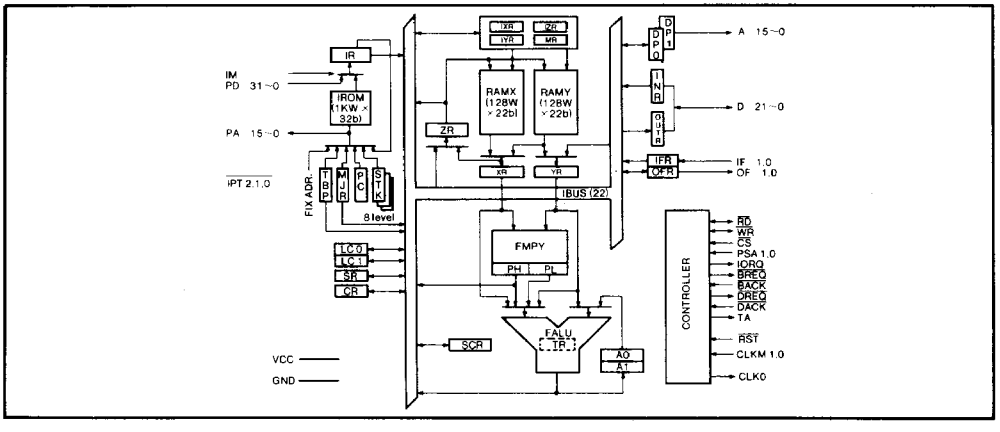
The MSM6992 is capable of functioning in the master mode as a multiprocessor or in the slave mode as a microcomputer I/O processor, hence this device can be readily incorporated into large scale systems with highly flexible system configurations.

Major MSM6992 applications include analysis for speech recognition and speech analysis/synthesis in speech processing equipment, high speed modems, codec, and echo cancellers in communication equipment. This device can also be effectively used for meter control, robotics and in audio equipment.

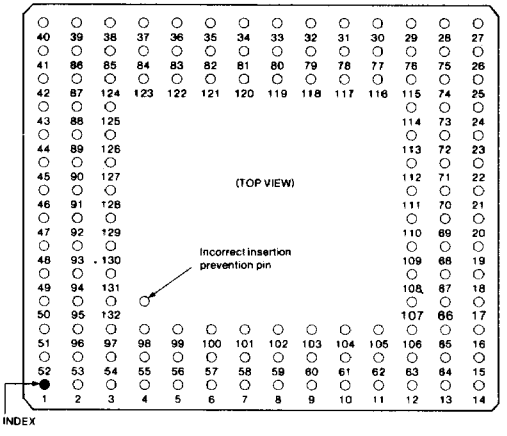
FEATURES

- Instruction cycle
  100nS/125nS
- Arithmetic formats
  - Floating-point arithmetic 16E6
  - Fixed-point arithmetic 16-bit
  - Logical arithmetic 22-bit
- Built-in 1K-word × 32-bit instruction RAM (Also usable as data ROM)
- Built-in 1K-word × 32-bit instruction ROM
- 32-bit wide horizontal microinstruction
- 64K-word program memory area
- 64K-word data memory area
- Multiprocessor interface
- Microcomputer interface (8-bit & 16-bit)
- DMA controller connection capability
- Maximum 15-bit shift function (left or right)
- Double loop function
- +5V power supply
- Low power consumption, 400 mW
- 132-pin ceramic PGA package
- 2μm silicon gate CMOS

BLOCK DIAGRAM



PIN CONFIGURATION



Pin No.	Pin name	I/O	Pin No.	Pin Name	I/O	Pin No.	Pin name	I/O	Pin No.	Pin Name	I/O
1	$\overline{DREQ}$	O	34	D18	I/O	67	PD5	I	100	TA	O
2	PSA0	I	35	D15	I/O	68	PD3	I	101	PD28	I
3	CLK0	O	36	D13	I/O	69	PA0	O	102	PD25	I
4	*	I	37	D10	I/O	70	PA1	O	103	PD21	I
5	IM	I	38	D8	I/O	71	PA4	O	104	PD17	I
6	PD30	I	39	D5	I/O	72	PA6	O	105	PD15	I
7	PD29	I	40	NC	–	73	PA8	O	106	PD13	I
8	GND	–	41	D2	I/O	74	GND	–	107	PD10	I
9	PD24	I	42	GND	–	75	PA15	O	108	PD7	I
10	PD22	I	43	A2	O	76	$\overline{IPT0}$	I	109	PD4	I
11	PD19	I	44	VCC	–	77	*	I	110	PD0	I
12	VCC	–	45	A6	O	78	*	I	111	PA2	O
13	PD14	I	46	A7	O	79	OF0	O	112	VCC	–
14	NC	–	47	NC	–	80	GND	–	113	PA9	O
15	PD11	I	48	A12	O	81	D17	I/O	114	PA11	O
16	PD8	I	49	A14	O	82	D14	I/O	115	PA14	O
17	PD6	I	50	$\overline{RD}$	I/O	83	D11	I/O	116	$\overline{IPT1}$	I
18	GND	–	51	$\overline{BREQ}$	O	84	VCC	–	117	VCC	–
19	PD2	I	52	$\overline{DACK}$	I	85	D7	I/O	118	OF1	O
20	PD1	I	53	$\overline{CS}$	I	86	D3	I/O	119	D19	I/O
21	NC	–	54	VCC	–	87	D0	I/O	120	D16	I/O
22	PA3	O	55	MCLK0	I	88	A0	O	121	D12	I/O
23	PA5	O	56	$\overline{RST}$	I	89	A3	O	122	D9	I/O
24	PA7	O	57	PD31	I	90	A5	O	123	D6	I/O
25	PA10	O	58	PD27	I	91	A9	O	124	D4	I/O
26	PA12	O	59	PD26	I	92	A10	O	125	D1	I/O
27	PA13	O	60	PD23	I	93	A13	O	126	A1	O
28	$\overline{IPT2}$	I	61	PD20	I	94	IF1	I	127	A4	O
29	*	I	62	PD18	I	95	GND	–	128	A8	O
30	IF0	I	63	PD16	I	96	$\overline{BACK}$	I	129	A11	O
31	*	I	64	PD12	I	97	NC	–	130	A15	O
32	D21	I/O	65	PD9	I	98	PSA1	I	131	$\overline{WR}$	I/O
33	D20	I/O	66	NC	I	99	MCLK1	I	132	IORQ	O

Note: Pins marked by an * must be connected to ground.

PIN DESCRIPTION

Pin symbol	I/O	Function
$PA_{15} \sim PA_0$	O	Program memory address output pins • These pins address external program memory. • On reset this address goes to zero.
$PD_{31} \sim PD_0$	I	Program memory data input pins • Input to external program memory data.
IM	I	Internal ROM selector input pin • This signal is used to select between internal or external program memory. for internal program mode IM="1" for external program mode IM="0"
$A_{15} \sim A_0$	O (3-state)	Data memory address output pins • Designates the external data memory and external I/O addresses.
$D_{21} \sim D_0$	I/O (3-state)	Data memory data input/output pins • Parallel input and output of external data memory, microprocessor, or I/O bus data.
$\overline{IPT_{2,1,0}}$	I	3-level interrupt input pins (active low) • Interrupts accepted during the "sequence" operations. • Interrupts are accepted if interrupt level is greater than interrupt priority set in control register and fixed address corresponding to interrupt level is passed to program memory address bus. Interrupt priorities are: $\overline{IPT_2} > \overline{IPT_1} > \overline{IPT_0}$
$IF_1 \sim IF_0$	I	Universal input flag pins • Inputs to set flag in IFR register.
$OF_1 \sim OF_0$	I	Universal output flag pins • Output of OFR latch.
$\overline{RD}$	I/O (3-state)	Read control input/output pin (active low) • Output of external data memory and I/O device read control signals when in master mode. • Input of read control signals from the host MPU and other DSPs when in slave mode.
$\overline{WR}$	I/O (3-state)	Write control input/output pin (active low) • Output of external data memory and I/O device write control signals when in master mode. • Input of write control signals from the host MPU and other DSPs when in slave mode.
$\overline{CS}$	I	Chip select input pin (active low) • MSM6992 is in slave mode when this signal is active and the input/output data. Port ($D_{21} \sim D_0$) is enabled.
$PSA_1 \sim PSA_0$	I	Port select address input pin • INR/OUTR ports connected to data input/output pins are selected according to the host MPU data bit length when MSM6992 is in slave mode.

PSA1	PSA0	Host CPU		
		8-bit	16-bit	MSM6992
0	0	INR 21~16 ↔ $D_5 \sim D_0$ OUTR 21~16	INR 21~16 ↔ $D_5 \sim D_0$ OUTR 21~16	INR 21~0 ↔ $D_{21} \sim D_0$ OUTR 21~0
0	1	INR 15~8 ↔ $D_7 \sim D_0$ OUTR 15~8	INR 15~0 ↔ $D_{15} \sim D_0$ OUTR 15~0	INR 21~0 ↔ $D_{21} \sim D_0$ OUTR 21~0
1	0	INR 7~0 ↔ $D_7 \sim D_0$ OUTR 7~8	NOP	INR 21~0 ↔ $D_{21} \sim D_0$ OUTR 21~0
1	1	NOP	NOP	INR 21~0 ↔ $D_{21} \sim D_0$ OUTR 21~0

PIN DESCRIPTION (CONT.)

Pin symbol	I/O	Function
IORQ	O (3-state)	I/O request output pin • This signal indicates whether the write or read operation is with respect to external data memory or I/O device. I/O request when IORQ = "1" Data memory request when IORQ = "0"
$\overline{BREQ}$	O	Bus request output pin (active low) • Signal to request external data bus. • Access requests passed to external devices are invalid when this DSP is accessed by external MPU ($\overline{CS}$ = "0").
$\overline{BACK}$	I	Bus acknowledge input pin (active low) • Signal to indicate that external data bus is available. • The DSP has access to bus if request signal is sent to external device ($\overline{BREQ}$ = "0") and the $\overline{BACK}$ signal is active, that is, a full "hand shake" must take place.
$\overline{DREQ}$	O	DMA request output pin (active low) • Data transfer request signal for data transfer between external memory and the DSP when in DMA mode. • $\overline{DREQ}$ is reset after transfer of one word of data has been completed to maximize utilization of system bus.
$\overline{DACK}$	I	DMA acknowledge input pin (active low) • Input signal indicating DMA cycle is enabled by external DMA control.
TA	O	Table data access indicator • TA = "1" when data is read from the program memory.
$\overline{RST}$	I	Reset input pin (active low) • This signal initializes all internal states of DSP. • The reset signal must be applied for a period greater than one machine cycle. • If reset input signal is applied for more than five machine cycles, internal clock synchronization is effected in addition to internal initialization.
MCLK0,1	I	Master clock input pin • Master clock obtained by input of external clock (50 ±10% duty) with frequency four times the machine cycle
CLKO	O	Internal system clock output pin
V_{CC}	–	+5V power supply pin
GND	–	Ground pin

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Limit	Unit
Supply voltage	V_{CC}	GND Basis	−0.5 ~ +7.0	V
Input voltage	V_{IN}		−0.5 ~ V_{CC}+0.5	V
Output voltage	V_{OUT}		−0.5 ~ V_{CC}+0.5	V
Storage temperature	T_{stg}		−65 ~ +150	°C
Power dissipation	P_d	Ta = 25°C		W

Operating Range

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Operating temperature	T_{OP}	0	25	70	°C
"H" input voltage	V_{IH}	2.2		V_{CC}+0.3	V
"L" input voltage	V_{IL}	−0.3		0.8	V

DC Characteristics

(V_{CC} = 5V ±5%, Ta=0~70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input leak current	I_{LI}	$0 \leqq V_{IN} \leqq V_{CC}$	−10		10	μA
Output leak current	I_{LO}	$0 \leqq V_{OUT} \leqq V_{CC}$	−10		10	μA
"H" output current	V_{OH}	I_{OH} = −400μA	2.4			V
"L" output current	V_{OL}	I_{OL} = 2.0mA			0.4	V
Stand-by supply current	Iccs	$0 \leqq V_I \leqq V_{CC}$		15		mA
Operation supply current	Icco	tφMC=31.25nS		80		mA

Capacitance

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_{IN}	f = 1MHz			10	pF
Output capacitance	C_{OUT}				20	pF

AC Characteristics

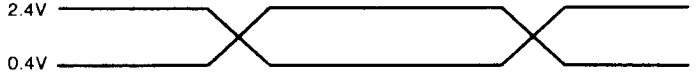
● Clock Timing

($Ta = 0 \sim 70°C$, $V_{DD} = 5V \pm 5\%$)

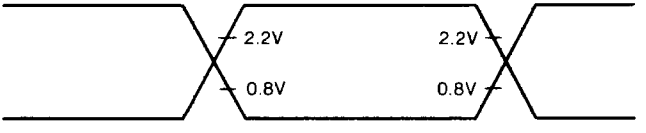
Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{\phi MC}$	MCLK cycle time		31.25	–	DC	ns
$t_{\phi MH}$	MCLK high level pulse width		13	–	–	ns
$t_{\phi ML}$	MCLK low level pulse width		13	–	–	ns
$t_{\phi Mr}$	MCLK rise time	Voltage at timing measurement point = 0.8V & 2.2V	–	–	5	ns
$t_{\phi Mf}$	MCLK fall time		–	–	5	ns
$t_{\phi C}$	CLKO cycle time		125	–	–	ns
$t_{\phi H}$	CLKO high level pulse width		T-10	–	–	ns
$t_{\phi L}$	CLKO low level pulse width		3T-20	–	–	ns
$t_{\phi r}$	CLKO rise time	Voltage at timing measurement point = 0.8V & 2.2V	–	–	10	ns
$t_{\phi f}$	CLKO fall time		–	–	10	ns
t_{RSTS}	$\overline{RST}$ set-up to MCLK↓		10	–	–	ns
t_{RSTH}	$\overline{RST}$ hold after MCLK↓		10	–	–	ns
t_{RSTW}	$\overline{RST}$ pulse width		$2t_{\phi MC}$* $4t_{\phi MC}$	–	–	ns

$T = t_{\phi C}/4$ * Refer to User's Manual.

Note 1: AC test input waveform



Note 2: Voltage at AC timing measurement point



External Instruction Operation

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{PAD}	$PA_{15} \sim PA_0$ output delay		–	–	55	ns
t_{PAH}	$PA_{15} \sim PA_0$ hold after CLKO↓		−5	–	–	ns
t_{PDS}	$PD_{31} \sim PD_0$ set-up to CLKO↓		24	–	–	ns
t_{PDH}*	$PD_{31} \sim PD_0$ hold after CLKO↓		T	–	–	ns
t_{TAD}	TA Output delay		–	–	60	ns
t_{TAH}	TA hold after CLKO↓		–	–	40	ns

* When using MSM6992 at low speed, it is necessary to latch memory output once to satisfy hold time.

Write/Read Operation (Master mode)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{AD}	$A_{15} \sim A_0$ delay		–	–	50	ns
t_{AH}	$A_{15} \sim A_0$ hold after CLKO↓		−5	–	–	ns
t_{WA}	$A_{15} \sim A_0$ hold after WR↑		−15	–	–	ns
t_{WRD}	$\overline{WR}$ output delay		–	–	T+20	ns
t_{WRH}	$\overline{WR}$ hold after CLKO↓		–	–	20	ns
t_{WW}	$\overline{WR}$ pulse width		3T-20	–	–	ns
t_{DOD}	$D_{21} \sim D_0$ output delay	C_L=100pF	–	–	T+40	ns
t_{DOH}	$D_{21} \sim D_0$ hold after CLKO↓	C_L=100pF	0	–	–	ns
t_{RDD}	$\overline{RD}$ output delay CLKO↓		–	–	T+20	ns
t_{RDH}	$\overline{RD}$ hold after CLKO↓		–	–	20	ns
t_{RR}	$\overline{RD}$ pulse width		3T-20	–	–	ns
t_{DIS}	$D_{21} \sim D_0$ set-up to CLKO	C_L=100pF	35	–	–	ns
t_{DIH}	$D_{21} \sim D_0$ hold after CLKO↓	C_L=100pF	0	–	–	ns
t_{IOQD}	IORQ output delay		–	–	60	ns
t_{IOQH}	IORQ hold after CLKO↓		–	–	40	ns

Read/Write Operation (Slave mode)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{AR}	$\overline{CS}$, $PSA_{0,1}$ setup to $\overline{RD}\downarrow$		0	–	–	ns
t_{RA}	$\overline{CS}$, $PSA_{0,1}$ hold after $\overline{RD}\uparrow$		20	–	–	ns
t_{RR}	$\overline{RD}$ pulse width		50	–	–	ns
t_{RD}	$D_{21} \sim D_0$ access from $\overline{RD}\downarrow$	C_L=100pF	–	–	60	ns
t_{DF}	$D_{21} \sim D_0$ float after $\overline{RD}\uparrow$	C_L=100pF	10	–	100	ns
t_{AW}	$\overline{CS}$, $PSA_{0,1}$ setup to $\overline{WR}\downarrow$		20	–	–	ns
t_{WA}	$\overline{CS}$, $PSA_{0,1}$ hold after $\overline{WR}\uparrow$		20	–	–	ns
t_{WW}	$\overline{WR}$ pulse width		50	–	–	ns
t_{DW}	$D_{21} \sim D_0$ setup to $\overline{WR}\uparrow$	C_L=100pF	20	–	–	ns
t_{WD}	$D_{21} \sim D_0$ hold after $\overline{WR}\uparrow$	C_L=100pF	30	–	–	ns
t_{CS}	$\overline{CS}$ setup to CLKO$\downarrow$		40	–	–	ns
t_{CH}	$\overline{CS}$ hold after CLKO$\downarrow$		0	–	–	ns
t_{DS}	$D_{21} \sim D_0$ setup to CLKO$\downarrow$	C_L=100pF	40	–	–	ns
t_{DH}	$D_{21} \sim D_0$ hold after CLKO$\downarrow$	C_L=100pF	0	–	–	ns

DMA Write/Read Operation

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{DRQ}	$\overline{DREQ}$ output delay (CLKO$\downarrow$)		–	–	30	ns
t_{AKQ}	$\overline{DREQ}$ output delay ($\overline{DACK}\downarrow$)		–	–	8T+30	ns
t_{AKS}	$\overline{DACK}$ setup to CLKO$\downarrow$		30	–	–	ns
t_{AKH}	$\overline{DACK}$ hold after CLKO$\downarrow$		10	–	–	ns
t_{AKC}	$\overline{DACK}$ setup to $\overline{RD}/\overline{WR}$		0	–	–	ns
t_{CAK}	$\overline{DACK}$ hold after $\overline{RD}/\overline{WR}$		20	–	–	ns
t_{RW}	$\overline{RD}/\overline{WR}$ pulse width		50	–	–	ns
t_{DC}	$D_{21} \sim D_0$ setup to $\overline{WR}\uparrow$	CL=100pF	20	–	–	ns
t_{CD}	$D_{21} \sim D_0$ hold after $\overline{WR}\downarrow$	C_L=100pF	30	–	–	ns
t_{RD}	$D_{21} \sim D_0$ access from $\overline{RD}\downarrow$	C_L=100pF	–	–	60	ns
t_{DF}	$D_{21} \sim D_0$ float after $\overline{RD}\uparrow$	C_L=100pF	10	–	100	ns

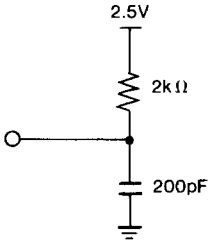
BREQ & BACK Timing

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{BRQ}	$\overline{BREQ}$ output delay (CLKO↓)		–	–	50	ns
t_{BQK}	$\overline{BREQ}$ output delay ($\overline{BACK}$↓)		–	–	8T+50	ns
t_{BKS}	$\overline{BACK}$ setup to CLKO↓		30	–	–	ns
t_{BKH}	$\overline{BACK}$ hold after CLKO↓		10	–	–	ns
t_{ZDA}	Address enable delay ($\overline{BACK}$↓)		–	–	4T+60	ns
t_{DZA}	Address disable delay ($\overline{BACK}$↑)		–	–	4T+60	ns
t_{ZDB}	Data Bus enable delay ($\overline{BACK}$↓)	C_L=100pF	–	–	5T+60	ns
t_{DZB}	Data Bus disable delay ($\overline{BACK}$↑)	C_L=100pF	–	–	4T+60	ns

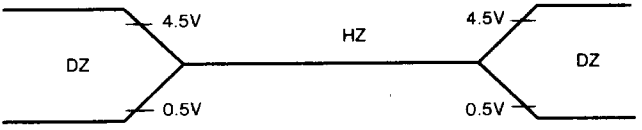
Interrupt & Port Timing

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{IPS}	$\overline{ITP}_0$ ~ $\overline{ITP}_2$ setup to CLKO↓		40	–	–	ns
t_{IPH}	$\overline{ITP}_0$ ~ $\overline{ITP}_2$ hold after CLKO↓		10	–	–	ns
t_{IFS}	IF_0 ~ IF_1 setup to CLKO↓		40	–	–	ns
t_{IFH}	IF_0 ~ IF_1 hold after CLKO↓		10	–	–	ns
t_{OFD}	OF_0 ~ OF_1 output delay		–	–	50	ns

Note 3: Output HZ and DZ test load circuit

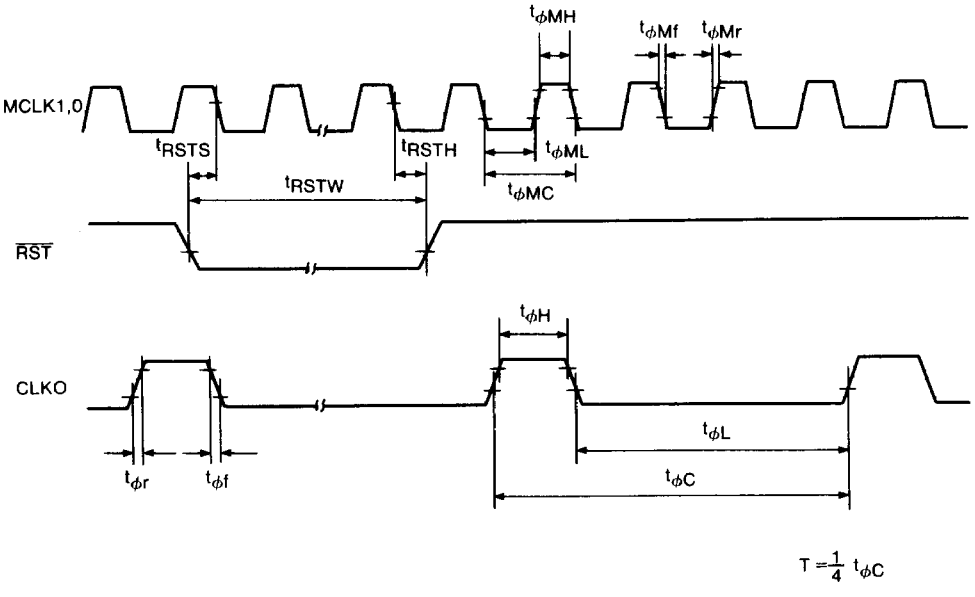


Note 4: Voltages at HZ and DZ timing measurement points

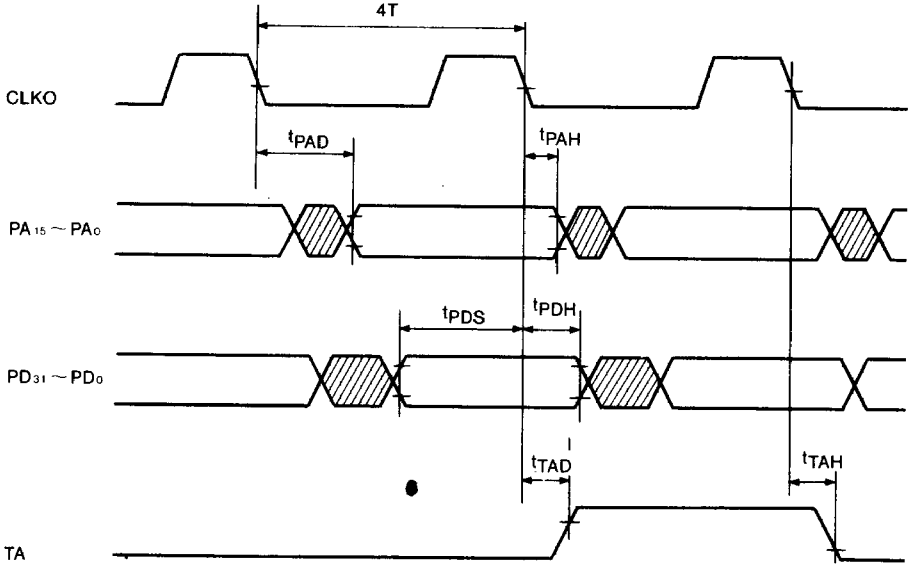


TIMING CHARTS

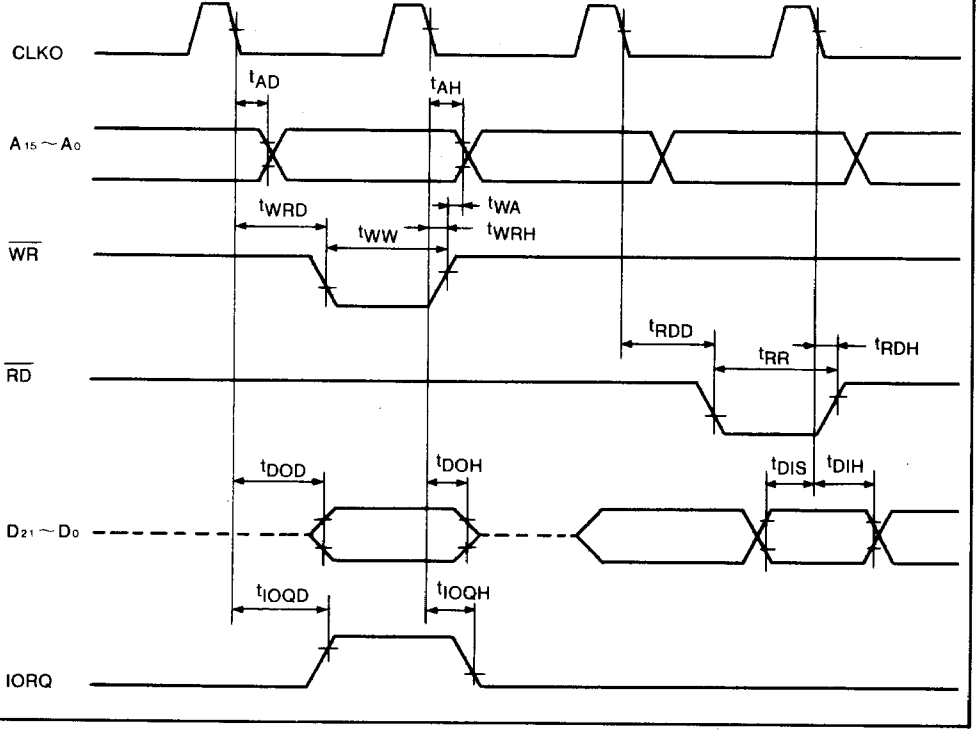
Clock



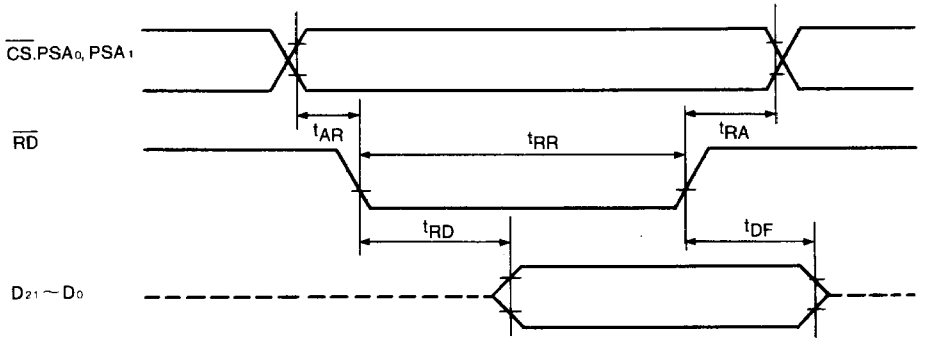
External Instruction Operation



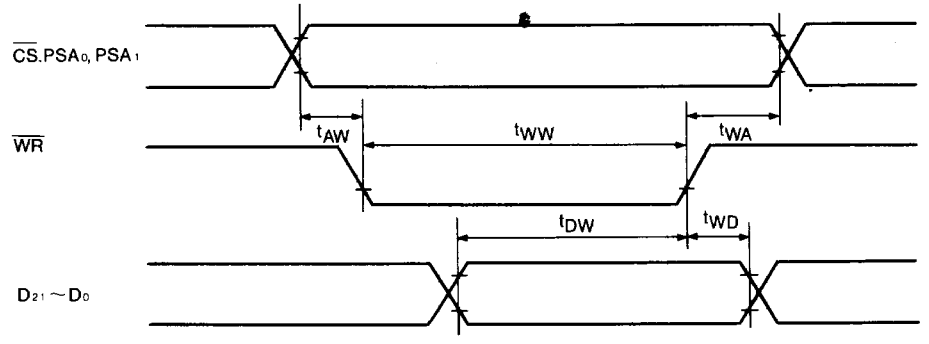
Write/Read Operation (Master mode)



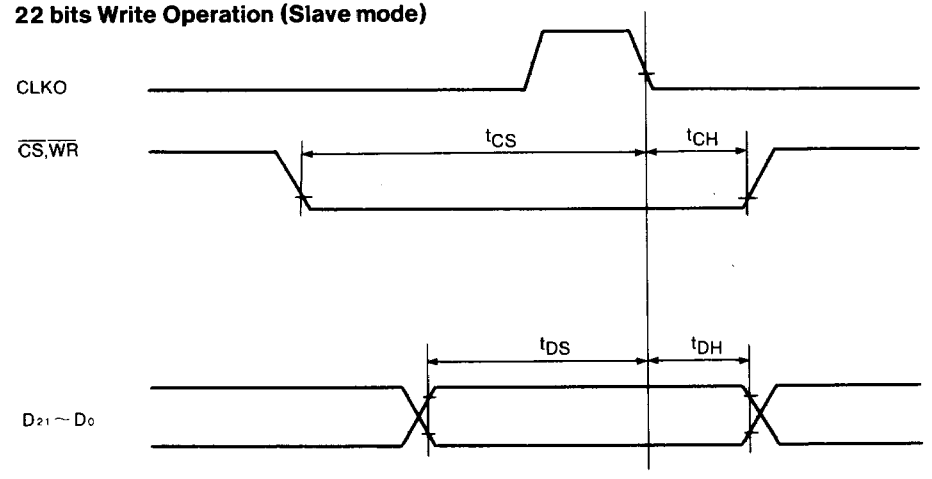
Read Operation (Slave mode)



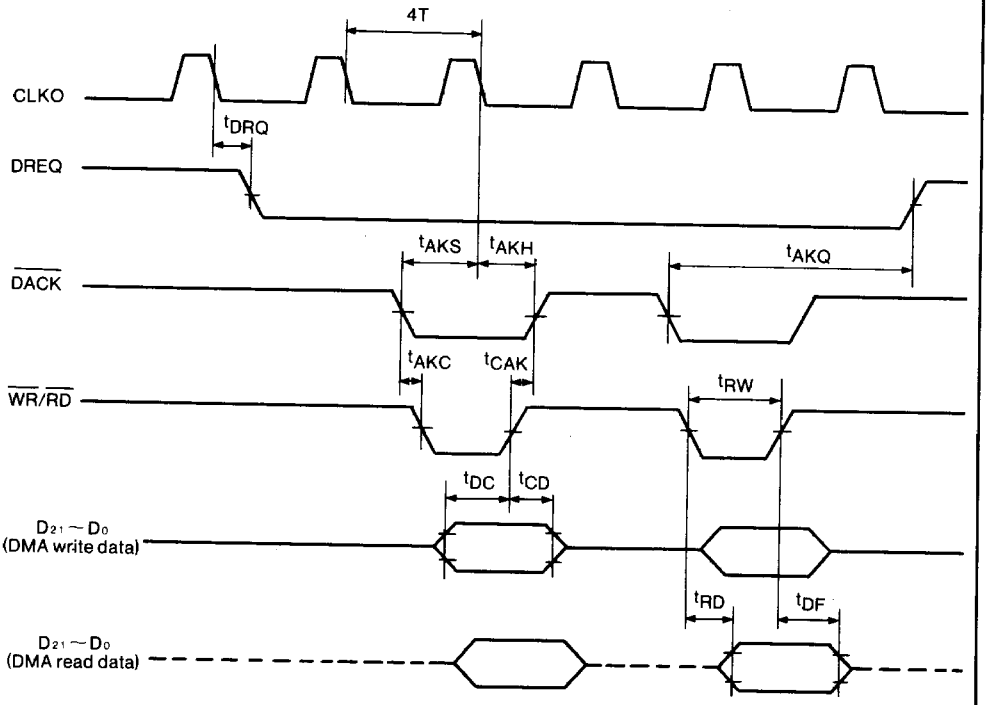
8, 16 bits Write Optation (Slave mode)



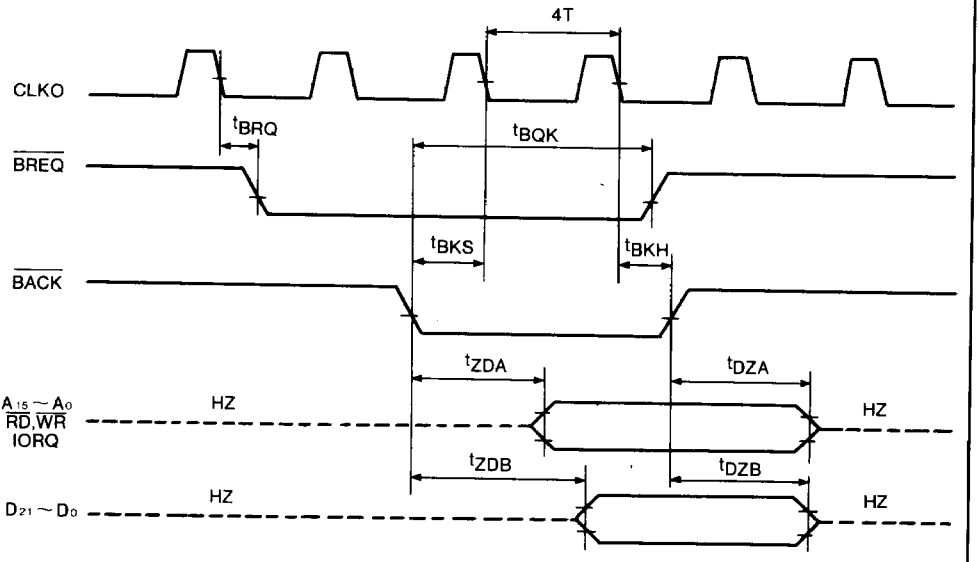
22 bits Write Operation (Slave mode)



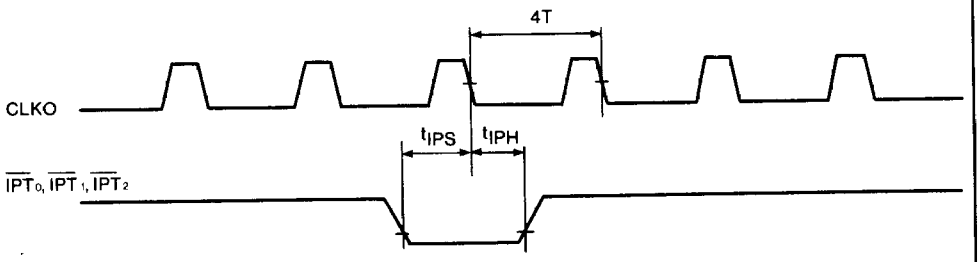
DMA Write/Read Operation BREQ & BACK Timing



BREQ & BACK Timing



Interrupt Timin



Port Input/Output Timing