

# BCD-to-Seven Segment Latch/Decoder/Driver for Liquid Crystals

## CMOS MSI (Low-Power Complementary MOS)

The MC14544B BCD-to-seven segment latch/decoder/driver is designed for use with liquid crystal readouts, and is constructed with complementary MOS (CMOS) enhancement mode devices. The circuit provides the functions of a 4-bit storage latch and an 8421 BCD-to-seven segment decoder and driver. The device has the capability to invert the logic levels of the output combination. The phase (Ph), blanking (BI), and latch disable (LD) inputs are used to reverse the truth table phase, blank the display, and store a BCD code, respectively. For liquid crystal (LC) readouts, a square wave is applied to the Ph input of the circuit and the electrically common backplane of the display. The outputs of the circuit are connected directly to the segments of the LC readout. The Ripple Blanking Input (RBI) and the Ripple Blanking Output (RBO) can be used to suppress either leading or trailing zeroes.

For other types of readouts, such as light-emitting diode (LED), incandescent, gas discharge, and fluorescent readouts, connection diagrams are given on this data sheet.

Applications include instrument (e.g., counter, DVM etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Latch Storage of Code
- Blanking Input
- Readout Blanking on All Illegal Input Combinations
- Direct LED (Common Anode or Cathode) Driving Capability
- Supply Voltage Range = 3.0 V to 18 V
- Capability for Suppression of Non-significant zero
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

### MAXIMUM RATINGS\* (Voltages referenced to V<sub>SS</sub>)

Rating	Symbol	Value	Unit
DC Supply Voltage	V <sub>DD</sub>	- 0.5 to + 18	V
Input Voltage, All Inputs	V <sub>in</sub>	- 0.5 to V <sub>DD</sub> + 0.5	V
DC Input Current per Pin	I <sub>in</sub>	± 10	mAdc
Operating Temperature Range	T <sub>A</sub>	- 55 to + 125	°C
Power Dissipation, per Package†	P <sub>D</sub>	500	mW
Storage Temperature Range	T <sub>stg</sub>	- 65 to + 150	°C
Maximum Continuous Output Drive Current (Source or Sink) per Output	I <sub>OHmax</sub> I <sub>OLmax</sub>	10	mAdc
Maximum Continuous Output Power* (Source or Sink) per Output	P <sub>OHmax</sub> P <sub>OLmax</sub>	70	mW

\* P<sub>OHmax</sub> = I<sub>OH</sub> (V<sub>OH</sub> - V<sub>DD</sub>) and P<sub>OLmax</sub> = I<sub>OL</sub> (V<sub>OL</sub> - V<sub>SS</sub>)

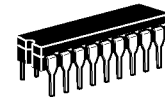
† Maximum Ratings are those values beyond which damage to the device may occur.

‡ Temperature Derating:

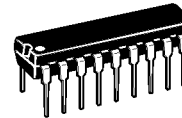
Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: - 12 mW/°C From 100°C To 125°C

## MC14544B



**L SUFFIX**  
CERAMIC  
CASE 726



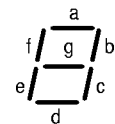
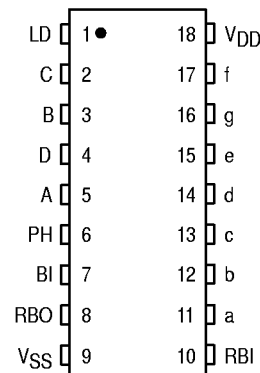
**P SUFFIX**  
PLASTIC  
CASE 707

### ORDERING INFORMATION

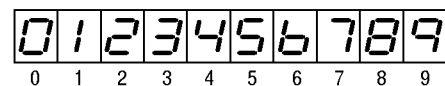
MC14XXXBCP Plastic  
MC14XXXBCL Ceramic

T<sub>A</sub> = - 55° to 125°C for all packages.

### PIN ASSIGNMENT



### DISPLAY



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range V<sub>SS</sub> ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>DD</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V<sub>SS</sub> or V<sub>DD</sub>). Unused outputs must be left open.

**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	"1" Level V <sub>in</sub> = 0 or V <sub>DD</sub>	V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95		—
			10	9.95	—	9.95	10	—	9.95		—
			15	14.95	—	14.95	15	—	14.95		—
Input Voltage # (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	"0" Level V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	"1" Level (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5		—
			10	7.0	—	7.0	5.50	—	7.0		—
			15	11	—	11	8.25	—	11		—
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 0.5 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	Source I <sub>OH</sub>	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc	
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—		
		10	—	—	—	-10.1	—	—	—		
		10	-1.6	—	-1.3	-2.25	—	-0.9	—		
		15	-4.2	—	-3.4	-8.8	—	-2.4	—		
	Sink I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—		
		10	1.6	—	1.3	2.25	—	0.9	—		
		10	—	—	—	10.1	—	—	—		
		10	—	—	—	10.1	—	—	—		
		15	4.2	—	3.4	8.8	—	2.4	—		
Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc	
Input Capacitance	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package) V <sub>in</sub> = 0 or V <sub>DD</sub> , I <sub>out</sub> = 0 μA	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μAdc	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (1.6 μA/kHz) f + I <sub>DD</sub>							μAdc	
		10	I <sub>T</sub> = (3.1 μA/kHz) f + I <sub>DD</sub>								
		15	I <sub>T</sub> = (4.7 μA/kHz) f + I <sub>DD</sub>								

#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 V min @ V<sub>DD</sub> = 5.0 V  
 2.0 V min @ V<sub>DD</sub> = 10 V  
 2.5 V min @ V<sub>DD</sub> = 15 V

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V<sub>DD</sub> in V, and f in kHz is input frequency.

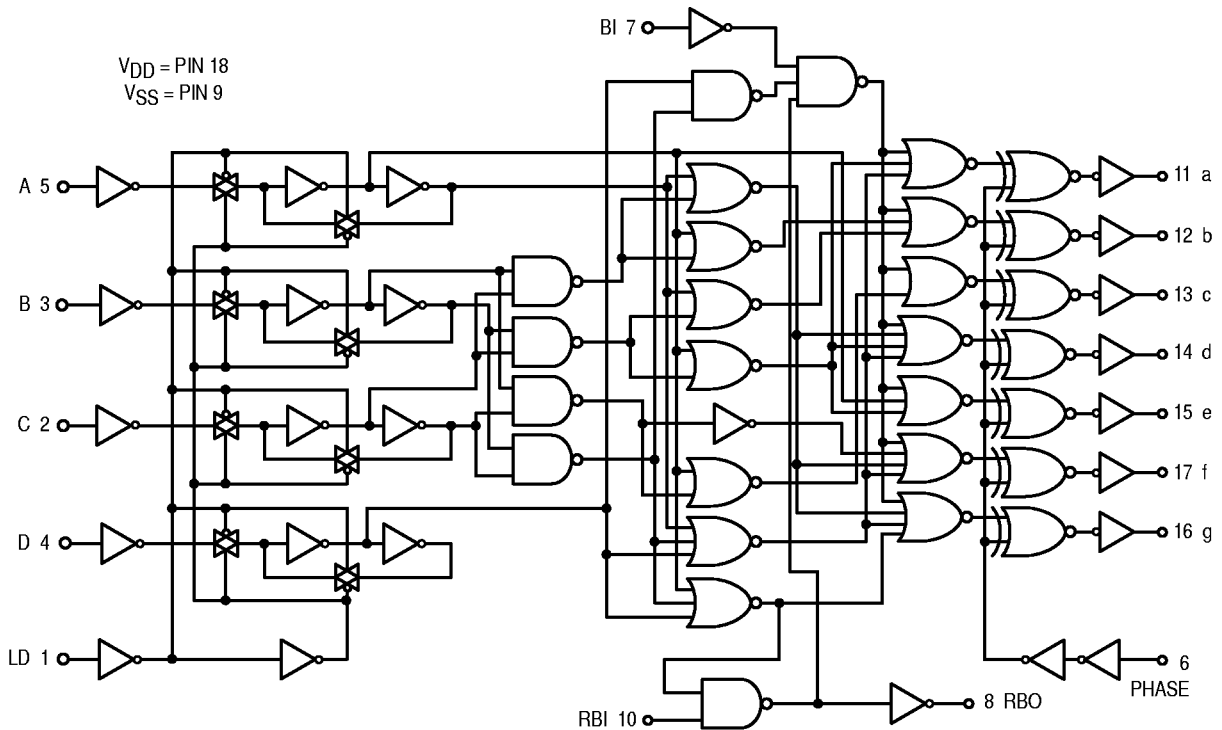
\* The formulas given are for the typical characteristics only at 25°C.

**SWITCHING CHARACTERISTICS\*** ( $C_L = 50 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	V <sub>DD</sub>	Min	Typ	Max	Unit
Output Rise Time $t_{TLH} = (3.0 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{TLH} = (1.5 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{TLH} = (1.1 \text{ ns/pF}) C_L + 10 \text{ ns}$	$t_{TLH}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 12.5 \text{ ns}$	$t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Turn-Off Delay Time $t_{PLH} = (1.7 \text{ ns/pF}) C_L + 520 \text{ ns}$ $t_{PLH} = (0.66 \text{ ns/pF}) C_L + 217 \text{ ns}$ $t_{PLH} = (0.5 \text{ ns/pF}) C_L + 160 \text{ ns}$	$t_{PLH}$	5.0 10 15	— — —	605 250 185	1210 500 370	ns
Turn-On Delay Time $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 420 \text{ ns}$ $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 172 \text{ ns}$ $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 130 \text{ ns}$	$t_{PHL}$	5.0 10 15	— — —	505 205 155	1650 660 495	ns
Setup Time	$t_{su}$	5.0 10 15	0 0 0	-40 -15 -10	— — —	ns
Hold Time	$t_h$	5.0 10 15	80 30 20	40 15 10	— — —	ns
Latch Disable Pulse Width (Strobing Data)	$t_{WH}$	5.0 10 15	250 100 80	125 50 40	— — —	ns

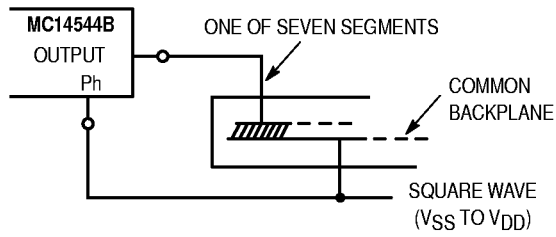
\* The formulas given are for the typical characteristics only.

**LOGIC DIAGRAM**

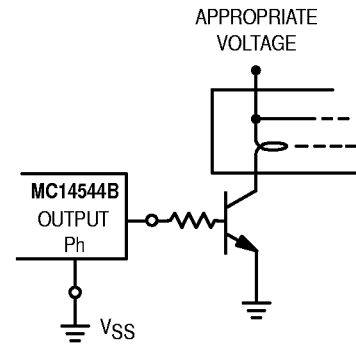


## CONNECTIONS TO VARIOUS DISPLAY READOUTS

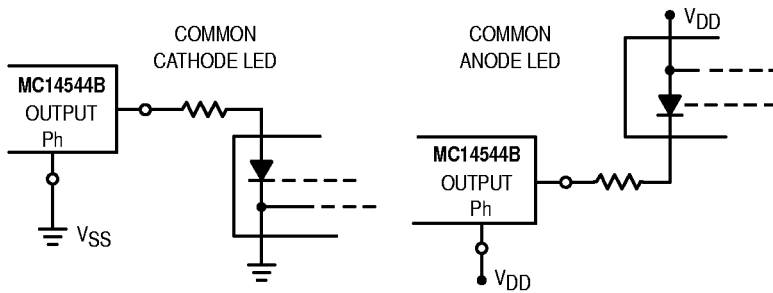
### LIQUID CRYSTAL (LC) READOUT



### INCANDESCENT READOUT

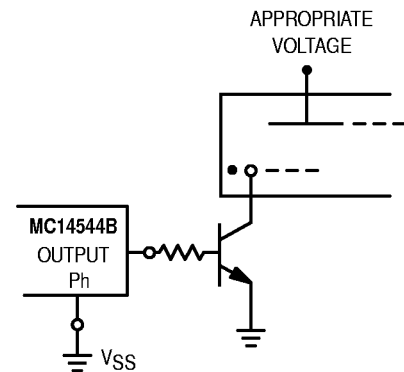


### LIGHT EMITTING DIODE (LED) READOUT



NOTE: Bipolar transistors may be added for gain (for  $V_{DD} \leq 10\text{ V}$  or  $I_{out} \geq 10\text{ mA}$ ).

### GAS DISCHARGE READOUT



### TRUTH TABLE

Inputs				Outputs												
RBI	LD	BI	Ph*	D	C	B	A	RBO	a	b	c	d	e	f	g	Display
X	X	1	0	X	X	X	X	#	0	0	0	0	0	0	0	Blank
1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	Blank
0	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
X	1	0	0	0	0	0	1	0	0	1	1	0	0	0	0	1
X	1	0	0	0	0	0	1	0	0	1	1	0	1	0	1	2
X	1	0	0	0	0	0	1	1	0	1	1	1	0	0	1	3
X	1	0	0	0	0	1	0	0	0	1	1	0	0	1	1	4
X	1	0	0	0	0	1	0	1	0	1	1	0	1	1	1	5
X	1	0	0	0	0	1	1	0	0	1	1	1	1	1	1	6
X	1	0	0	0	0	1	1	1	0	1	0	0	0	0	0	7
X	1	0	0	0	1	0	0	0	0	1	1	1	1	1	1	8
X	1	0	0	0	1	0	0	1	0	1	1	1	0	1	1	9
X	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0	Blank
X	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	Blank
X	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	Blank
X	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	Blank
X	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	Blank
X	0	0	0	X	X	X	X	#	**						**	
†	†	†	1	†				†	Inverse of Output Combinations Above						Display as above	

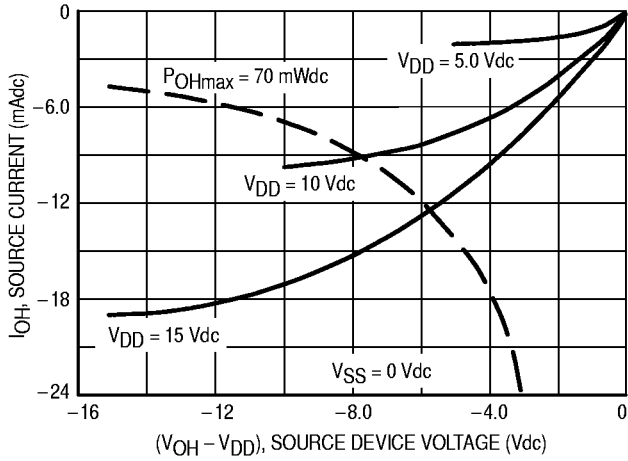
X = Don't Care

† Above Combinations

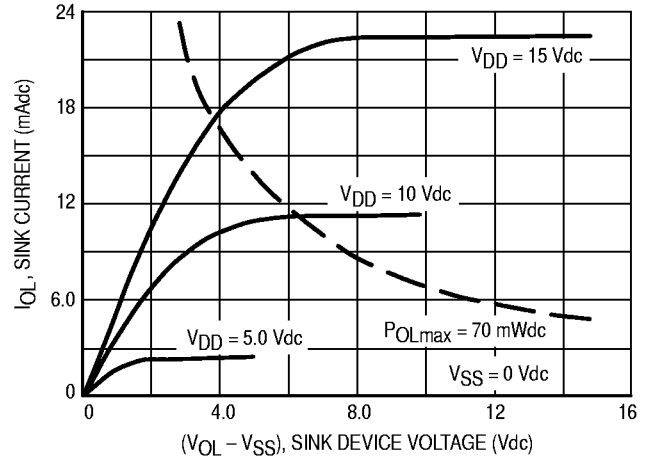
\* For liquid crystal readouts, apply a square wave to Ph. For common cathode LED readouts, select Ph = 0. For common anode LED readouts, select Ph = 1.

\*\* Depends upon the BCD Code previously applied when LD = 1.

#  $RBO = RBI \cdot (\bar{A} \bar{B} \bar{C} \bar{D})$



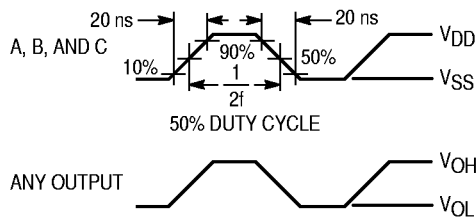
**Figure 1. Typical Output Source Characteristics**



**Figure 2. Typical Output Sink Characteristics**

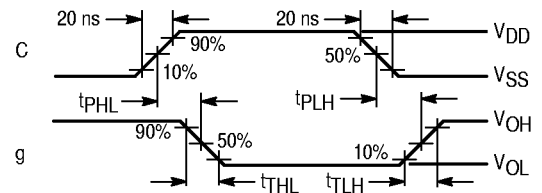
Inputs BI and Ph low, and Inputs D and LD high.  
f in respect to a system clock.

All outputs connected to respective  $C_L$  loads.

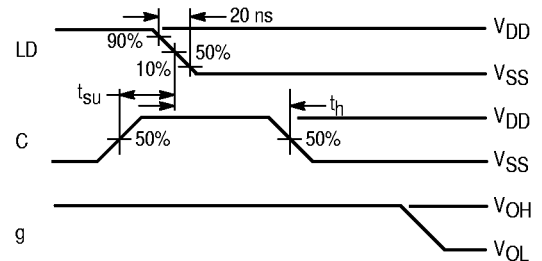


**Figure 3. Dynamic Power Dissipation Signal Waveforms**

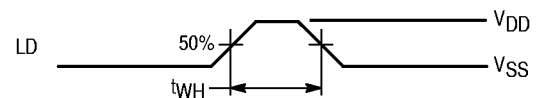
(a) Inputs D, Ph, and BI low, and Inputs A, B, and LD high.



(b) Inputs D, Ph, and BI low, and Inputs A and B high.



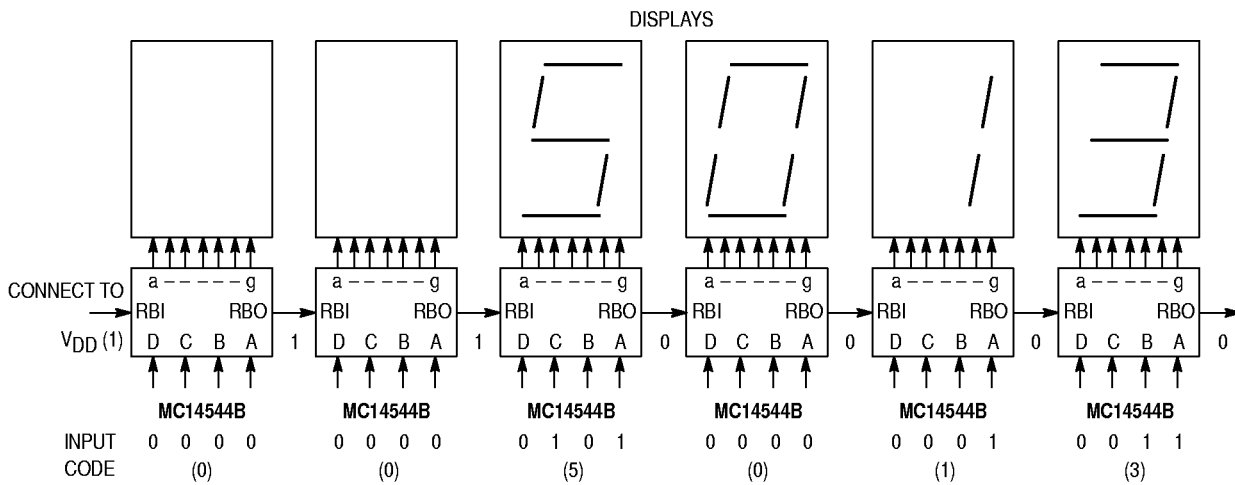
(c) Data DCBA strobed into latches



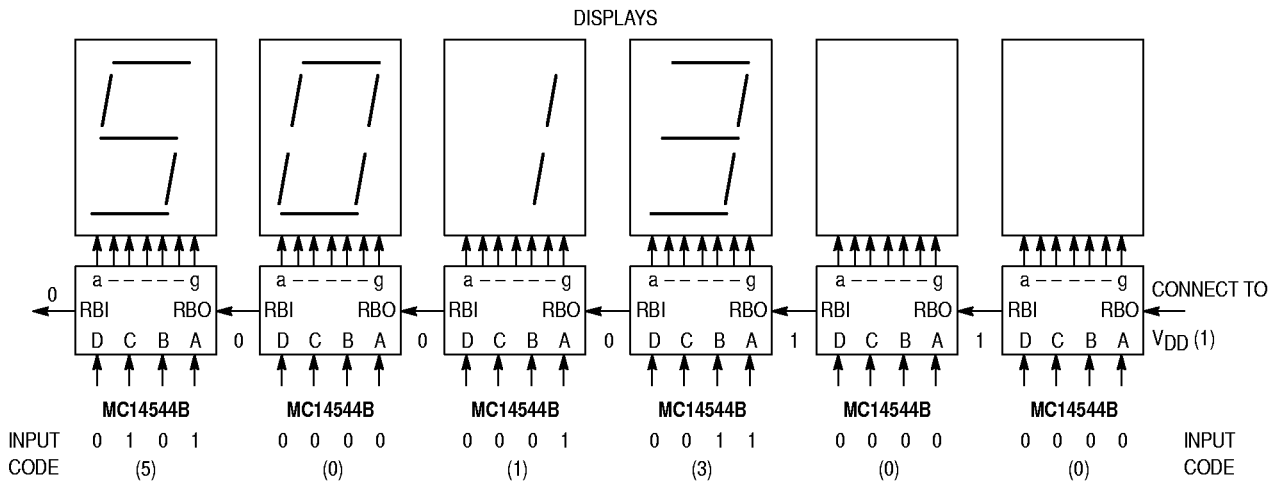
**Figure 4. Dynamic Signal Waveforms**

# TYPICAL APPLICATIONS FOR RIPPLE BLANKING

## LEADING EDGE ZERO SUPPRESSION

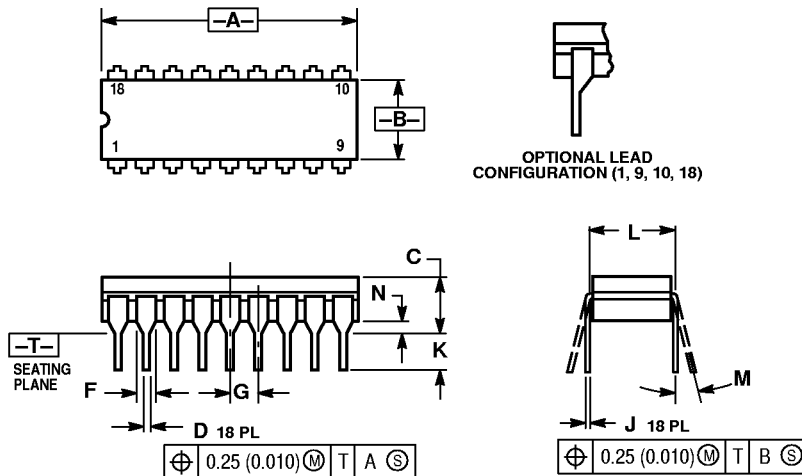


## TRAILING EDGE ZERO SUPPRESSION



## OUTLINE DIMENSIONS

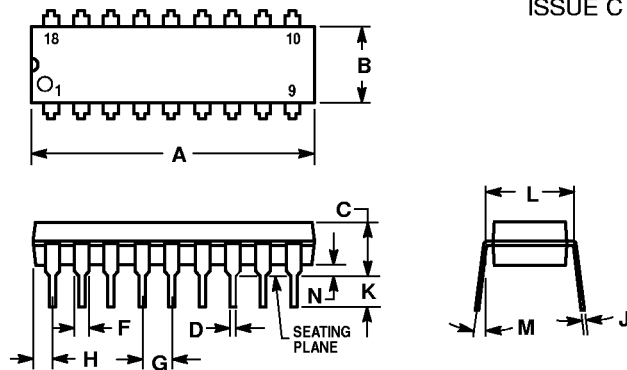
### L SUFFIX CERAMIC DIP PACKAGE CASE 726-04 ISSUE G



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIMENSION F FOR FULL LEADS. HALF LEADS OPTIONAL AT LEAD POSITIONS 1, 9, 10, AND 18.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.880	0.910	22.35	23.11
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.021	0.38	0.53
F	0.055	0.070	1.40	1.78
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.20	0.30
K	0.125	0.170	3.18	4.32
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

### P SUFFIX PLASTIC DIP PACKAGE CASE 707-02 ISSUE C



- NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
  2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

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MC14544B/D

