

TYPES SN54AS195, SN74AS195 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

D2661, DECEMBER 1983

- Parallel-to-Serial, Serial-to-Parallel Conversions
- Parallel Synchronous Loading
- J and \bar{K} Inputs to First Stage
- Right-Shift Only with Complementary Outputs on Last Stage
- Direct Overriding Clear
- Dependable Texas Instruments Quality and Reliability

description

These 4-bit registers feature parallel inputs, parallel outputs, J- \bar{K} serial inputs, shift/load control input, and a direct overriding clear. The registers have two modes of operation:

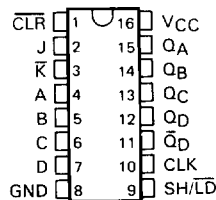
- Parallel (broadside) load
- Shift (in the direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading serial data flow is inhibited.

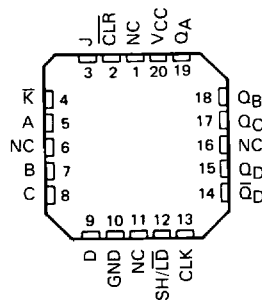
Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J- \bar{K} inputs. These inputs permit the first stage to perform as a J- \bar{K} , D-, or T-type flip-flop as shown in the function table.

The SN54AS195 is characterized for operation over the full military range of -55°C to 125°C . The SN74AS195 is characterized for operation from 0°C to 70°C .

SN54AS195 . . . J PACKAGE
SN74AS195 . . . N PACKAGE
(TOP VIEW)



SN54AS195 . . . FH PACKAGE
SN74AS195 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

2

ALS AND AS CIRCUITS

3

PRODUCT PREVIEW

This page contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS
INSTRUMENTS

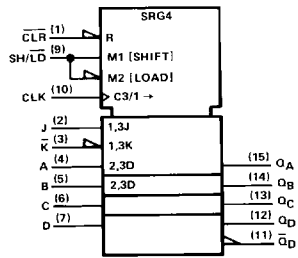
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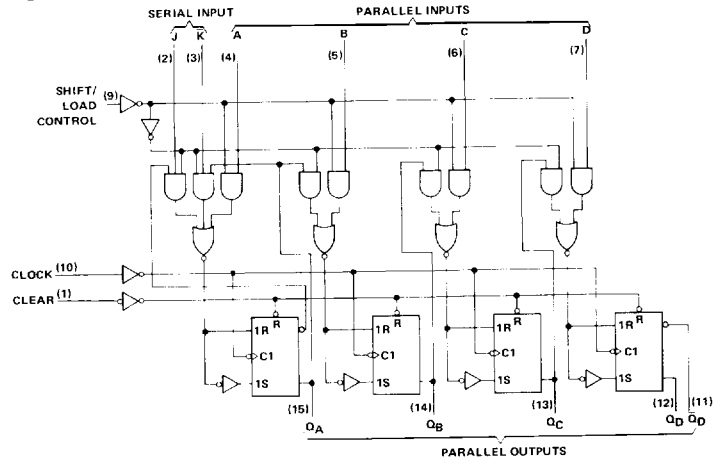
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TYPES SN54AS195, SN74AS195
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

logic symbol



logic diagram (positive logic)



Pin numbers shown are for J and N packages.

FUNCTION TABLE

CLEAR	SHIFT/LOAD	CLOCK	INPUTS				OUTPUTS				
			SERIAL J K	PARALLEL A B C D	QA	QB	QC	QD	QD-bar		
L	X	X	X X	X X X X	L	L	L	L	L	L	
H	L	↑	X X	a b c d	a	b	c	d	d	d	
H	H	L	X X	X X X X	QA0	QB0	QC0	QD0	QD0	QD0	
H	H	↑	L H	X X X X	QA0	QA0	QBn	QCn	QCn	QDn	
H	H	↑	L L	X X X X	L	QA0	QBn	QCn	QCn	QDn	
H	H	↑	H H	X X X X	H	QA0	QBn	QCn	QCn	QDn	
H	H	↑	H L	X X X X	QA0	QA0	QBn	QCn	QCn	QDn	

2 ALS AND AS CIRCUITS

typical clear, shift, and load sequences

