HD100182

9-bit Wallace Tree Adder

The HD100182 is a 9-bit Wallace tree adder. It is designed to assist in performing high-speed hardware multiplication.

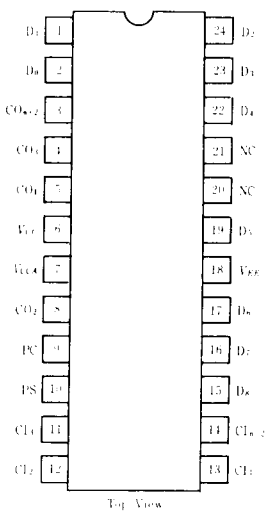
The device is designed to add 9-bits of data 1-bit-slice wide and handle the carry-ins from the previous slices.

The HD100182 is easily expanded and still maintains four levels of delay regardless of input string length.

In conjunction with the HD100183 Recode Multiplier, the HD100179 Carry Lookahead, and the HD100180 High-speed Adder, the HD100182 assists in performing parallel multiplication of two signed numbers to produce a signed two's complement product.

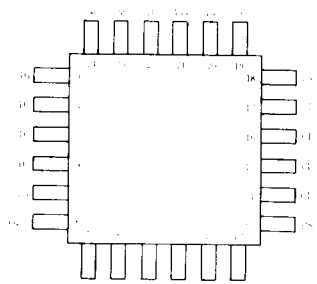
■PIN ARRANGEMENT

● **HD100182**



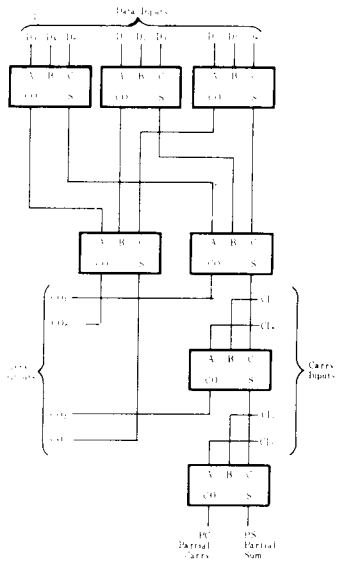
Top View

● **HD100182F**

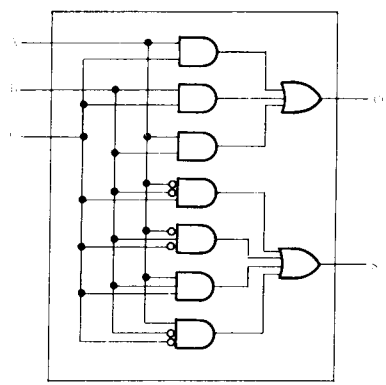


Top View

■LOGIC DIAGRAM



● **Adder Logic Diagram**



● **Adder Truth Table**

Inputs			Outputs	
A	B	C	S	CO
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

■DC CHARACTERISTICS (V_{EE} = −4.2 to −4.8V, V_{CC} = V_{CCA} = GND, Ta = 0 to +85℃)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		125	180	260	mA
Input Current	I_{IH}	V_{IN} = $V_{IH\ max}$	CI_1 ~ CI_{n-2}, CI_{n-2}, D_1, D_3 ~ D_6, D_8			300	μA
			D_0, D_2, D_7			250	μA

Note) As for other items, refer to the "Common DC Characteristics".

■AC CHARACTERISTICS (V_{EE} = −2.2 to −2.8V, V_{CC} = V_{CCA} = 2.0V)

●HD100182

Item	Symbol	Test Condition		0℃ min	0℃ max	25℃ min	25℃ typ	25℃ max	85℃ min	85℃ max	Unit
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveform	D_n→CO_{n-2}	1.20	4.30	1.40	2.15	4.50	1.50	4.50	ns
			D_n→CO_1	1.20	4.50	1.30	2.20	4.70	1.40	4.70	
			D_n→CO_2	2.00	5.80	2.20	3.00	6.10	2.30	6.10	
			D_n→CO_3	1.30	4.50	1.40	2.10	4.70	1.50	4.70	
			D_n→PC, PS	2.30	7.00	2.50	3.80	7.20	2.60	7.20	
			CI_{n-2}, CI_1→CO_2	0.90	3.20	1.00	1.50	3.40	1.10	3.40	
			CI_{n-2}, CI_1→PC, PS	1.40	4.20	1.50	2.15	4.45	1.60	4.45	
			CI_2, CI_3→PC, PS	0.80	3.00	0.80	1.45	3.20	0.90	3.20	
Transition Time	t_{TLH} t_{THL}			0.45	1.60	0.45	0.75	1.60	0.45	1.60	ns

●HD100182F

Item	Symbol	Test Condition		0℃ min	0℃ max	25℃ min	25℃ typ	25℃ max	85℃ min	85℃ max	Unit
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveform	D_n→CO_{n-2}	1.20	4.10	1.40	2.10	4.30	1.50	4.30	ns
			D_n→CO_1	1.20	4.20	1.30	2.10	4.50	1.40	4.50	
			D_n→CO_2	2.10	5.60	2.20	2.90	5.90	2.30	5.90	
			D_n→CO_3	1.30	4.30	1.40	2.00	4.50	1.50	4.50	
			D_n→PC, PS	2.40	6.80	2.50	3.70	7.00	2.60	7.00	
			CI_{n-2}, CI_1→CO_2	0.90	3.00	1.00	1.40	3.20	1.10	3.20	
			CI_{n-2}, CI_1→PC, PS	1.40	4.00	1.50	2.05	4.25	1.60	4.25	
			CI_2, CI_3→PC, PS	0.70	2.80	0.80	1.35	3.00	0.90	3.00	
Transition Time	t_{TLH} t_{THL}			0.45	1.50	0.45	0.70	1.50	0.45	1.50	ns

Note) The circuit in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m s⁻¹ (500 linear fpm) is maintained.